

RELIABILITY REPORT FOR MAX11628EEE+T

PLASTIC ENCAPSULATED DEVICES

September 30, 2012

MAXIM INTEGRATED

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Approved by		
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Conclusion

The MAX11628EE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

- I.Device Description
- II.Manufacturing Information
- IV.Die Information
- V.Quality Assurance Information
- III.Packaging Information
- VI.Reliability Evaluation

I. Device Description

A. General

.....Attachments

The MAX11626-MAX11632/MAX11632/MAX11633 are serial 12-bit analog-to-digital converters (ADCs) with an internal reference. These devices feature on-chip FIFO, scan mode, internal clock mode, internal averaging, and AutoShutdown(tm). The maximum sampling rate is 300ksps using an external clock. The MAX11632/MAX11633 have 16 input channels; the MAX11628/MAX11629 have 8 input channels; and the MAX11626/MAX11627 have 4 input channels. These six devices operate from either a +3V supply or a +5V supply, and contain a 10MHz SPI-/QSPI(tm)-/MICROWIRE®- compatible serial port. The MAX11626-MAX11629 are available in 16-pin QSOP packages. The MAX11632/MAX11633 are available in 24-pin QSOP packages. All six devices are specified over the extended -40°C to +85°C temperature range.



II. Manufacturing Information

- A. Description/Function:12-Bit, 300ksps ADCs with FIFO and Internal ReferenceB. Process:C6C. Number of Device Transistors:31874D. Fabrication Location:Japan or USA
- E. Assembly Location: Philippines and Thailand
- F. Date of Initial Production: August 20, 2010

III. Packaging Information

A. Package Type:	16-pin QSOP		
B. Lead Frame:	Copper		
C. Lead Finish:	100% matte Tin		
D. Die Attach:	Conductive		
E. Bondwire:	Au (0.8 mil dia.)		
F. Mold Material:	Epoxy with silica filler		
G. Assembly Diagram:	#05-9000-4058		
H. Flammability Rating:	Class UL94-V0		
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1		
J. Single Layer Theta Ja:	120°C/W		
K. Single Layer Theta Jc:	37°C/W		
L. Multi Layer Theta Ja:	105°C/W		
M. Multi Layer Theta Jc:	37°C/W		

IV. Die Information

A. Dimensions:	90 X 130 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	AI with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.9 microns (as drawn)
F. Minimum Metal Spacing:	0.9 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)	
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet.0.1% For all Visual Defects.	
C. Observed Outgoing Defect Rate:	< 50 ppm	
D. Sampling Plan:	Mil-Std-105D	

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 127 \times 2}$$
 (Chi square value for MTTF upper limit)
(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)
$$\lambda = 8.7 \times 10^{-9}$$

𝔅 = 8.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.2 @ 25C and 0.4 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EF4ZAQ001J, D/C 1012)

The AC88 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 1200V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101
ESD-MM:	+/- 250V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX11628EEE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS	
Static Life Test (Note 1)						
	Ta = 135C	DC Parameters	48	0	EF4ZAQ001B, D/C1001	
	Biased Time = 192 hrs.	& functionality	79	0	EF4ZAQ002X, D/C 1104	

Note 1: Life Test Data may represent plastic DIP qualification lots.