RELIABILITY REPORT

FOR

MAX11410ATI+T

PLASTIC ENCAPSULATED DEVICES

November 9, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX11410ATI+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11410 is a low-power, multi-channel, 24-bit delta-sigma ADC with features and specifications that are optimized for precision sensor measurement. The input section includes a low-noise programmable gain amplifier (PGA) with very high input impedance and available gains from 1x to 128x to optimize the overall dynamic range. Input buffers provide isolation of the signal inputs from the switched-capacitor sampling network when the PGA is not in use, making the ADC easy to drive even with high-impedance sources. Several integrated features simplify precision sensor applications. The programmable matched current sources provide excitation for resistive sensors. An additional current sink and current source aid in detecting broken sensor wires. The 10-channel input multiplexer provides the flexibility needed for complex, multi-sensor measurements. GPIOs reduce isolation components and ease control of switches or other circuitry. When used in single-cycle mode, the digital filter settles within a single conversion cycle. The available FIR digital filter allows single-cycle settling in 16ms while providing more than 90dB simultaneous rejection of 50Hz and 60Hz line noise. The integrated on-chip oscillator requires no external components. If needed, an external clock source may be used instead. Control registers and conversion data are accessed through the SPI-compatible serial interface.

II. Manufacturing Information

A. Description/Function:	24-Bit Multi-Channel Low-Power 1.9ksps Delta-Sigma ADC with PGA
B. Process:	TS18
C. Number of Device Transistors:	396736
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	June 24, 2016

III. Packaging Information

A. Package Type:	28-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5977
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	35°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	99.5433X99.5433 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AZ08-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11410ATI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.