

RELIABILITY REPORT FOR MAX1123EGK+ PLASTIC ENCAPSULATED DEVICES

September 12, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by Sokhom Chum Quality Assurance Reliability Engineer



Conclusion

The MAX1123EGK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1123 is a monolithic 10-bit, 210Msps analogto- digital converter (ADC) optimized for outstanding dynamic performance at high IF frequencies up to 500MHz. The product operates with conversion rates of up to 210Msps while consuming only 460mW. At 210Msps and an input frequency of 100MHz, the MAX1123 achieves a spurious-free dynamic range (SFDR) of 74.5dBc. Its excellent signal-to-noise ratio (SNR) of 57.4dB at 10MHz remains flat (within 1.5dB) for input tones up to 500MHz. This makes the MAX1123 ideal for wideband applications such as digital predistortion in cellular base-station transceiver systems. The MAX1123 requires a single 1.8V supply. The analog input is designed for either differential or singleended operation and can be AC- or DC-coupled. The ADC also features a selectable on-chip divide-by-2 clock circuit, which allows the user to apply clock frequencies as high as 420MHz. This helps to reduce the phase noise of the input clock source. A differential LVDS sampling clock is recommended for best performance. The converter's digital outputs are LVDS compatible, and the data format can be selected to be either two''s complement or offset binary. The MAX1123 is available in a 68-pin QFN with exposed pad (EP) and is specified over the industrial (-40°C to +85°C) temperature range. For pin-compatible, lower and higher speed versions of the MAX1123, refer to the MAX1122 (170Msps) and the MAX1124 (250Msps) data sheets. For a higher speed, pin-compatible 8-bit version of the MAX1123, refer to the MAX1121 data sheet.



E. Assembly Location:

F. Date of Initial Production:

II. Manufacturing Information

A. Description/Function:	1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications
B. Process:	TS18
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan

Korea

October 24, 2003

III. Packaging Information

A. Package Type:	QFN 10x10 68L
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0587 / B
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

Α.	Dimensions:	132 X 132 mils
В.	Passivation:	$Si_3N_4/SiO_2\;$ (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D.	Backside Metallization:	None
E.	Minimum Metal Width:	0.18µm
F.	Minimum Metal Spacing:	0.18µm
G.	Bondpad Dimensions:	
н.	Isolation Dielectric:	SiO ₂
Ι.	Die Separation Method:	Wafer Saw



V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering)
		Don Lipps (Manager, Reliability Engineering)
		Bryan Preeshl (Vice President of QA)
В.	Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C.	Observed Outgoing Defect Rate:	< 50 ppm
D.	Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{1000 \times 4340 \times 48 \times 2}$ (Chi square value for MTTF upper limit) $\lambda = 4.4 \times 10^{-9}$ $\lambda = 4.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QFL0EQ001D D/C 0340)

The CA08 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.



Table 1 Reliability Evaluation Test Results

MAX1123EGK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	e 1) Ta = 135℃ Biased Time = 1000 hrs.	DC Parameters & functionality	48	0	QFL0EQ001C, D/C 0340

Note 1: Life Test Data may represent plastic DIP qualification lots.