RELIABILITY REPORT

FOR

MAX11192ATE+T

PLASTIC ENCAPSULATED DEVICES

August 23, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Eric Wright Reliability Engineer	Brian Standley Manager, Reliability

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Conclusion

The MAX11192ATE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11192/MAX11195/MAX11198 is a dual-channel SAR ADCs with simultaneous sampling at 2Msps, 12-/14-/16-bit resolution, and differential inputs. Available in a tiny 16-pin, 3mm x 2mm ultra TDFN package, this ADC delivers excellent static and dynamic performance while operating from a supply voltage over the range of 3.0V to 5.25V. An integrated reference further reduces board area and component count. The MAX11192/MAX11195/MAX11198 output conversion data using an SPI-compatible serial interface with a dual DOUT bus. Specifications apply over the extended industrial temperature range of -40°C to +125°C.

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II. Manufacturing Information

A. Description/Function:	12-/14-/16-Bit, 2Msps, Dual Simultaneous Sampling SAR ADCs with Internal Reference
B. Process:	TS18
C. Number of Device Transistors:	107112
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	June 20, 2017

III. Packaging Information

A. Package Type:	16-pin TDFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	8006ns
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5973
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	60°C/W
K. Single Layer Theta Jc:	11°C/W
L. Multi Layer Theta Ja:	60°C/W
M. Multi Layer Theta Jc:	11°C/W

IV. Die Information

A. Dimensions:	94.4882X55.1181 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.64 \times 10^{-9}$

λ = 2.64 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AZ11-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX11192ATE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 1000 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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