RELIABILITY REPORT

FOR

MAX11100EUB+

PLASTIC ENCAPSULATED DEVICES

September 16, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The MAX11100EUB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11100 low-power, 16-bit analog-to-digital converter (ADC) features a successive-approximation ADC, automatic power-down, fast 1.1µs wake-up, and a high-speed SPI/QSPI(tm)/MICROWIRE®-compatible interface. The MAX11000 operates with a single +5V analog supply and features a separate digital supply, allowing direct interfacing with 2.7V to 5.25V digital logic. At the maximum sampling rate of 200ksps, the MAX11100 typically consumes 2.45mA. Power consumption is typically 12.25mW (VAVDD = VDVDD = +5V) at a 200ksps (max) sampling rate. AutoShutdown(tm) reduces supply current to 140µA at 10ksps and to less than 10µA at reduced sampling rates. Excellent dynamic performance and low power, combined with ease of use and small package size (10-pin µMAX® and 12-bump WLP), make the MAX11100 ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

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II. Manufacturing Information

A. Description/Function:	16-Bit, +5V, 200ksps ADC with 10µA Shutdown
B. Process:	C6Y
C. Number of Device Transistors:	12275
D. Fabrication Location:	Japan
E. Assembly Location:	Philippines, Thailand, or Malaysia
F. Date of Initial Production:	September 23, 2011

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4279
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W K.
Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	62 X 87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

λ = 13.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the C6Y Process results in a FIT Rate of 0.04 @ 25C and 0.73 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot E1A0IQ001C, D/C 1110)

The AC23 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of+/- 100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX11100EUB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	E1A0IQ002C, D/C 1126

Note 1: Life Test Data may represent plastic DIP qualification lots.

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