RELIABILITY REPORT

FOR

MAX11040KGUU+

PLASTIC ENCAPSULATED DEVICES

May 18, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX11040KGUU+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX11040K/MAX11060 are 24-/16-bit, 4-channel, simultaneous-sampling, sigma-delta analog-to-digital converters (ADCs). The devices allow simultaneous sampling of as many as 32 channels using a built-in cascade feature to synchronize as many as eight devices. The serial interface of the devices allows reading data from all the cascaded devices using a single command. Four modulators simultaneously convert each fully differential analog input with a programmable data output rate ranging from 0.25ksps to 64ksps. The devices achieve 106dB SNR at 16ksps and 117dB SNR at 1ksps (MAX11040K). The devices operate from a single +3V supply. The differential analog input range is ±2.2V when using the internal reference; an external reference is optional. Each input is overvoltage protected up to ±6V without damage. The devices use an internal crystal oscillator or an external source for clock. The devices are compatible with SPI(tm), QSPI(tm), MICROWIRE(tm), and DSP-compatible 4-wire serial interfaces. An on-board interface logic allows one serial interface (with a single chip select) to control up to eight cascaded devices or 32 simultaneous sampling analog input channels. The devices are ideally suited for power-management systems. Each channel includes an adjustable sampling phase enabling internal compensation for phase shift due to external dividers, transformers, or filters at the inputs. The output data rate is adjustable with a 0.065% resolution (at 16ksps or below) to track the varying frequency of a periodic input. A SYNC input allows periodic alignment of the conversion timing of multiple devices with a remote timing source. The ICs are available in a 38-pin TSSOP package specified over the -40°C to +105°C industrial temperature range. *Introduction to the MAX11040K, a 24-bit, simultaneous-sampling, sigma-delta converter. Accurate simultaneous sampling with the MAX11046 and MAX11040K sigma-delta converters.*

II. Manufacturing Information

A. Description/Function:	24-/16-Bit, 4-Channel, Simultaneous-Sampling, Cascadable, Sigma-Delta ADCs
B. Process:	S45
C. Number of Device Transistors:	360321
D. Fabrication Location:	California
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	March 1, 2011

III. Packaging Information

A. Package Type:	TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1917
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	3
J. Single Layer Theta Ja:	73°C/W
K. Single Layer Theta Jc:	11°C/W
L. Multi Layer Theta Ja:	62.5°C/W
M. Multi Layer Theta Jc:	11°C/W

IV. Die Information

A. Dimensions:	108 X 288 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot ST0ZBQ001H D/C 1105)

The AC89 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000 per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11040KGUU+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	ST0ZBQ001H, D/C 1105

Note 1: Life Test Data may represent plastic DIP qualification lots.