RELIABILITY REPORT

FOR

MAX109EHF+

PLASTIC ENCAPSULATED DEVICES

April 9, 2009

MAXIM INTEGRATED PRODUCTS

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SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX109EHF+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX109, 2.2Gsps, 8-bit, analog-to-digital converter (ADC) enables the accurate digitizing of analog signals with frequencies up to 2.5GHz. Fabricated on an advanced SiGe process, the MAX109 integrates a high-performance track/hold (T/H) amplifier, a quantizer, and a 1:4 demultiplexer on a single monolithic die. The MAX109 also features adjustable offset, full-scale voltage (via REFIN), and sampling instance allowing multiple ADCs to be interleaved in time.

The innovative design of the internal T/H amplifier, which has a wide 2.8GHz full-power bandwidth, enables a flat-frequency response through the second Nyquist region. This results in excellent ENOB performance of 6.9 bits. A fully differential comparator design and decoding circuitry reduce out-of-sequence code errors (thermometer bubbles or sparkle codes) and provide excellent metastability performance (1014 clock cycles). This design guarantees no missing codes.

The analog input is designed for both differential and single-ended use with a 500mVP-P input-voltage range. The output data is in standard LVDS format, and is demultiplexed by an internal 1:4 demultiplexer. The LVDS outputs operate from a supply-voltage range of 3V to 3.6V for compatibility with single 3V-reference systems. Control inputs are provided for interleaving additional MAX109 devices to increase the effective system-sampling rate.

The MAX109 is offered in a 256-pin Super Ball-Grid Array (SBGA) package and is specified over the extended industrial temperature range (-40°C to +85°C).

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II. Manufacturing Information

A. Description/Function:	8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs
B. Process:	GST3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	ATP Philippines
F. Date of Initial Production:	May 23, 2007

III. Packaging Information

A. Package Type:	256-pin SBGA
B. Lead Frame:	PCB Substrate
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Multi Layer Theta Ja:	13.5°C/W
K. Multi Layer Theta Jc:	1.5°C/W

IV. Die Information

A. Dimensions:	275 X 281 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 9.6 \times 10^{-9}$

λ = 9.6 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim"s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-7245) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1N). Current monitor data for the S4 Process results in a FIT Rate of 0.14 @ 25C and 2.34 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA17 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

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Table 1

Reliability Evaluation Test Results

MAX109EHF+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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