

RELIABILITY REPORT
FOR
MAX1069xxUD
PLASTIC ENCAPSULATED DEVICES

July 25, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX1069 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1069 is a low-power, 14-bit successive-approximation analog-to-digital converter (ADC). The device features automatic power-down, an on-chip 4MHz clock, a +4.096V internal reference, and an I2C-compatible 2-wire serial interface capable of both fast and high-speed modes.

The MAX1069 operates from a single supply and consumes 5mW at the maximum conversion rate of 58.6ksps. AutoShutdown™ powers down the device between conversions, reducing supply current to less than 50µA at a 1ksps throughput rate. The option of a separate digital supply voltage allows direct interfacing with +2.7V to +5.5V digital logic.

The MAX1069 performs a unipolar conversion on its single analog input using its internal 4MHz clock. The full-scale analog input range is determined by the internal reference or by an externally applied reference voltage ranging from 1V to AVDD.

The four address select inputs (ADD0-ADD3) allow up to sixteen MAX1069 devices on the same bus. The MAX1069 is packaged in a 14-pin TSSOP and offers both commercial and extended temperature ranges. Refer to the MAX1169 for a 16-bit device in a pin-compatible package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
AVDD to AGND	-0.3V to +6V
DVDD to DGND	-0.3V to +6V
AGND to DGND	-0.3V to +0.3V
AGNDS to AGND	-0.3V to +0.3V
AIN, REF, REFADJ to AGND	-0.3V to (AVDD + 0.3V)
SCL, SDA, ADD_ to DGND	-0.3V to +6V
Maximum Current into Any Pin	50mA
Operating Temperature Ranges:	
MAX1069_CUD	0°C to +70°C
MAX1069_EUD	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin TSSOP	727mW
Derates above +70°C	
14-Pin TSSOP	9.1mW/°C

II. Manufacturing Information

A. Description/Function:	58.6ksps, 14-Bit, 2-Wire Serial ADC in a 14-Pin TSSOP
B. Process:	S6 (0.6 micron CMOS)
C. Number of Device Transistors:	18,269
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Thailand, or USA
F. Date of Initial Production:	October, 2002

III. Packaging Information

A. Package Type:	14-Pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-2101-0057
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	87 x 105 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si (Aluminum/ Silicon)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-5964) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AC06Z die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1069xxUD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. ^{1/} ^{2/}

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} ^{3/}	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

^{1/} Table II is restated in narrative form in 3.4 below.

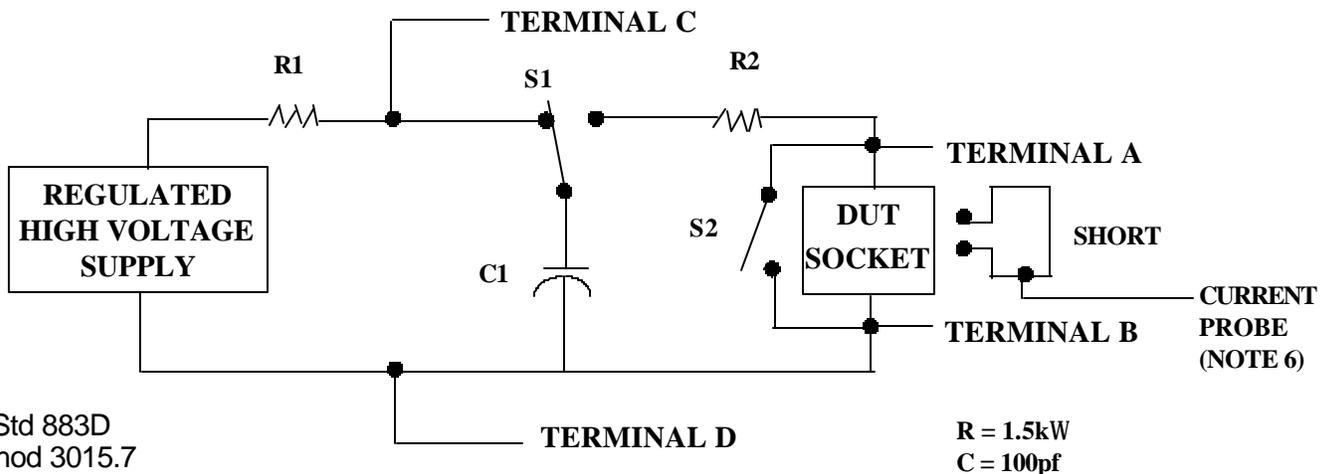
^{2/} No connects are not to be tested.

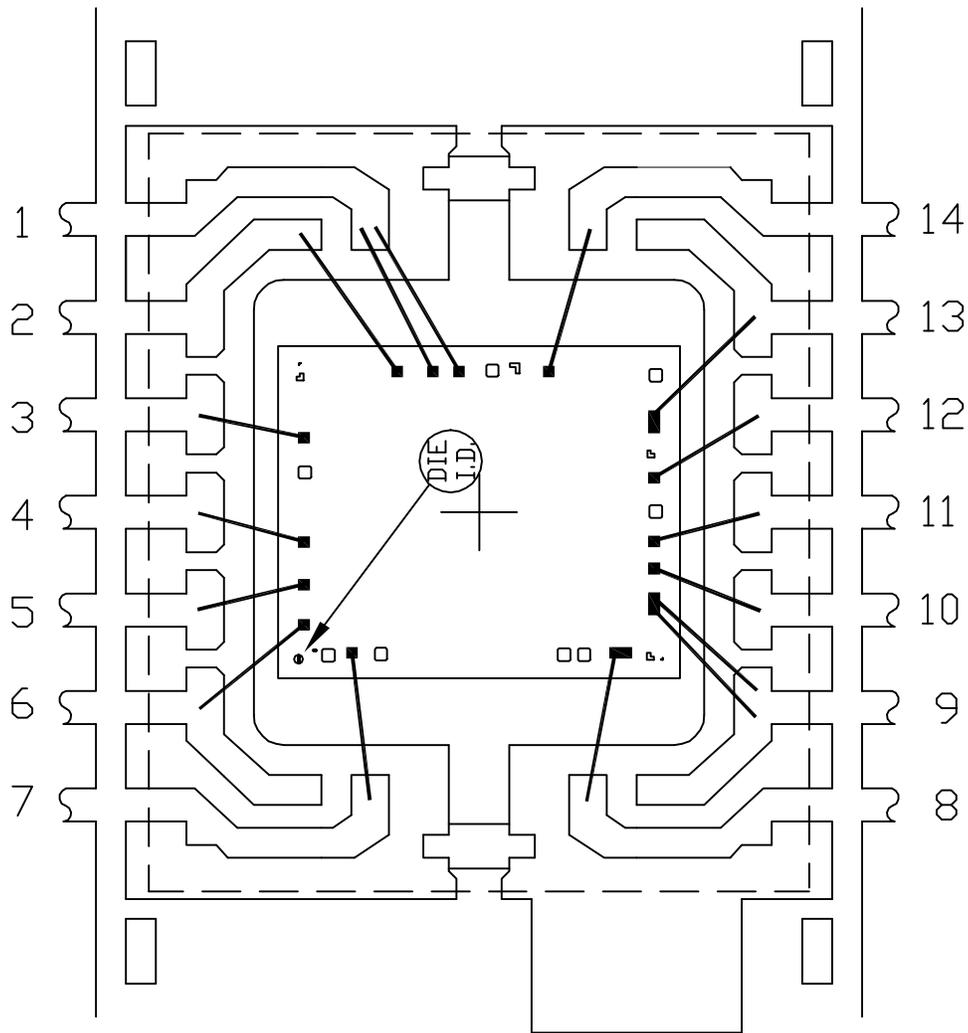
^{3/} Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

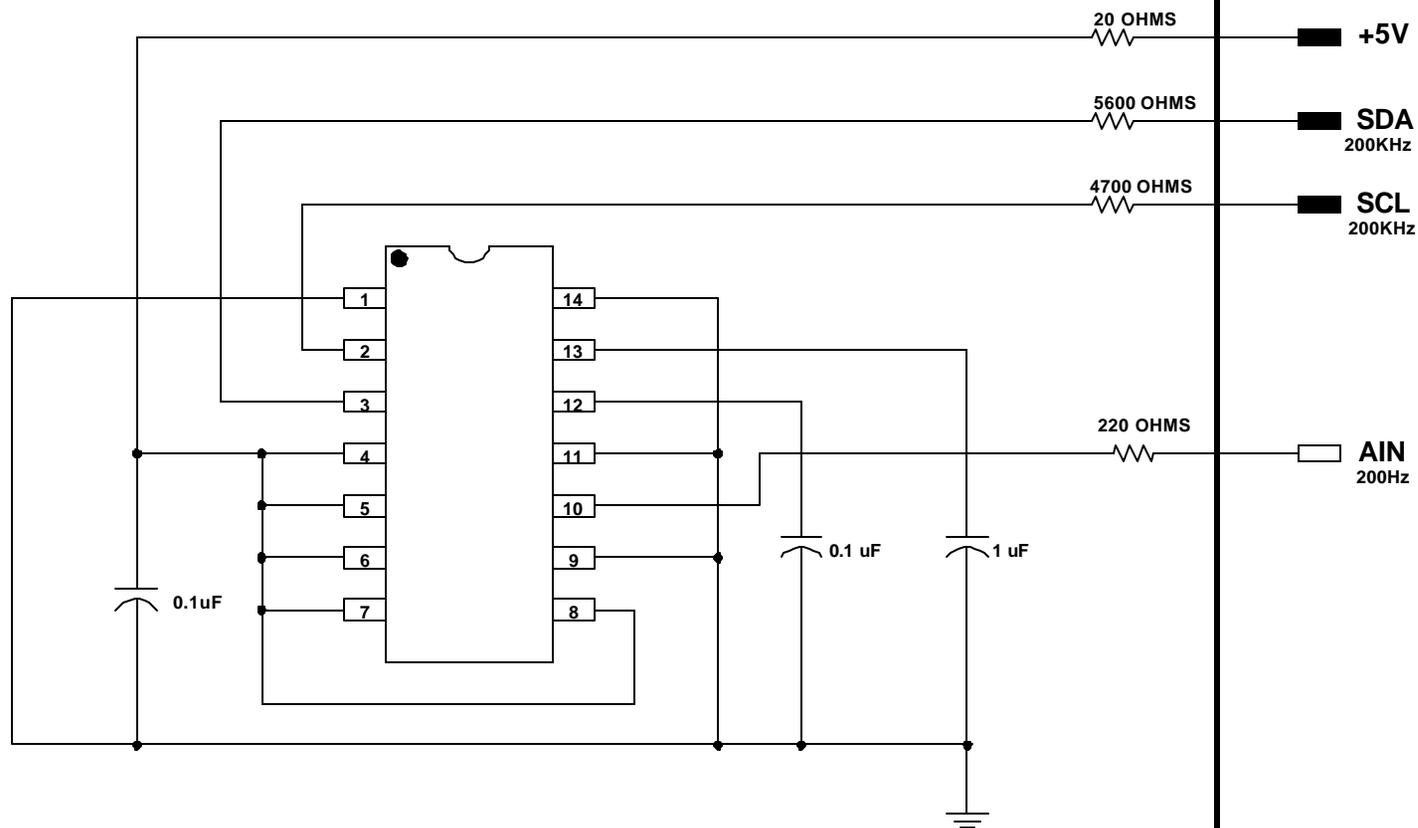




PKG. CODE: U14-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x122	PKG. DESIGN			BOND DIAGRAM #: 05-2101-0057	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX1069/1169
PACKAGE: 14-TSSOP (U14-1)
MAX. EXPECTED CURRENT = 4mA

DRAWN BY: TEK TAN/ JIM CITTADINO

NOTES: SCL and SDA will provide wake up signal sequence from outside. Clock signal waveform provided by design to be programmed in oven by B/I manager.