

RELIABILITY REPORT
FOR
MAX1003CAX+
PLASTIC ENCAPSULATED DEVICES

February 13, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX1003CAX+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX1003 is a dual, 6-bit analog-to-digital converter (ADC) that combines high-speed, low-power operation with a user-selectable input range, an internal reference, and a clock oscillator. The dual parallel ADCs are designed to convert in-phase (I) and quadrature (Q) analog signals into two 6-bit, offset-binary-coded digital outputs at sampling rates up to 90MSPS. The ability to directly interface with baseband I and Q signals makes the MAX1003 ideal for use in direct-broadcast satellite, VSAT, and QAM16 demodulation applications. The MAX1003 input amplifiers feature true differential inputs, a -0.5dB analog bandwidth of 55MHz, and user-programmable input full-scale ranges of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled input signal, matching performance between input channels is typically better than 0.1dB gain, 1/4LSB offset, and 0.5° phase. Dynamic performance is 5.85 effective number of bits (ENOB) with a 20MHz analog input signal, or 5.7 ENOB with a 50MHz signal. The MAX1003 operates with +5V analog and +3.3V digital supplies for easy interfacing to +3.3V-logic-compatible digital signal processors and microprocessors. It comes in a 36-pin SSOP package.

II. Manufacturing Information

A. Description/Function:	Low-Power, 90Msps, Dual 6-Bit ADC
B. Process:	GST2
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Malaysia
F. Date of Initial Production:	June 17, 1997

III. Packaging Information

A. Package Type:	36-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-7001-0212
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	84.7457627119°C/W
K. Single Layer Theta Jc:	19.3°C/W
L. Multi Layer Theta Ja:	58°C/W
M. Multi Layer Theta Jc:	19.5°C/W

IV. Die Information

A. Dimensions:	66 X 98 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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|-----------------------------------|--|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.06 @ 25C and 1.10 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AD84-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-750V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX1003CAX+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.