RELIABILITY REPORT

FOR

LM4041xIx3-1.2

PLASTIC ENCAPSULATED DEVICES

March 20, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The LM4041 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The LM4041 is a precision two-terminal shunt mode, bandgap voltage reference with a fixed reverse breakdown voltage of 1.225V. Ideal for space-critical applications, the LM4041 is offered in the subminiature 3-pin SC70 surface-mount package (1.8mm 5 1.8mm), 50% smaller than comparable devices in SOT23 surface-mount packages (SOT23 versions are also available).

Laser-trimmed resistors ensure precise initial accuracy. With a 100ppm/°C temperature coefficient, the device is offered in four grades of initial accuracy ranging from 0.1% to 1%. The LM4041 has a 60µA to 12mA shunt current capability with low dynamic impedance, ensuring stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

The LM4041 does not require an external stabilizing capacitor while ensuring stability with any capacitive load.

B. Absolute Maximum Ratings

Item	Rating
Reverse Current (Cathode to Anode)	20mA
Forward Current (Anode to Cathode)	10mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
3-Pin SC70	174mW
3-Pin SOT23	320mW
Derates above +70°C	
3-Pin SC70	2.17mW/°C
3-Pin SOT23	4.01mW/°C

II. Manufacturing Information

A. Description/Function:	Improved Precision MicroPower Shunt Reference
B. Process:	S12
C. Number of Device Transistors:	60
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	April, 2000

III. Packaging Information

	3 Lead SC70	**3 Lead SOT23**
A. Package Type:		
B. Lead Frame:	Alloy 42	Alloy 42
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Non-Conductive Exposy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0901-0157	Buildsheet # 05-0901-0156
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	30 x 31 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 75 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 14.48 \times 10^{-9}$ $\lambda = 14.48$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (#06-5672) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RF25 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

LM4041xIx3-1.2

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		75	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23 SC-70	320 97	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

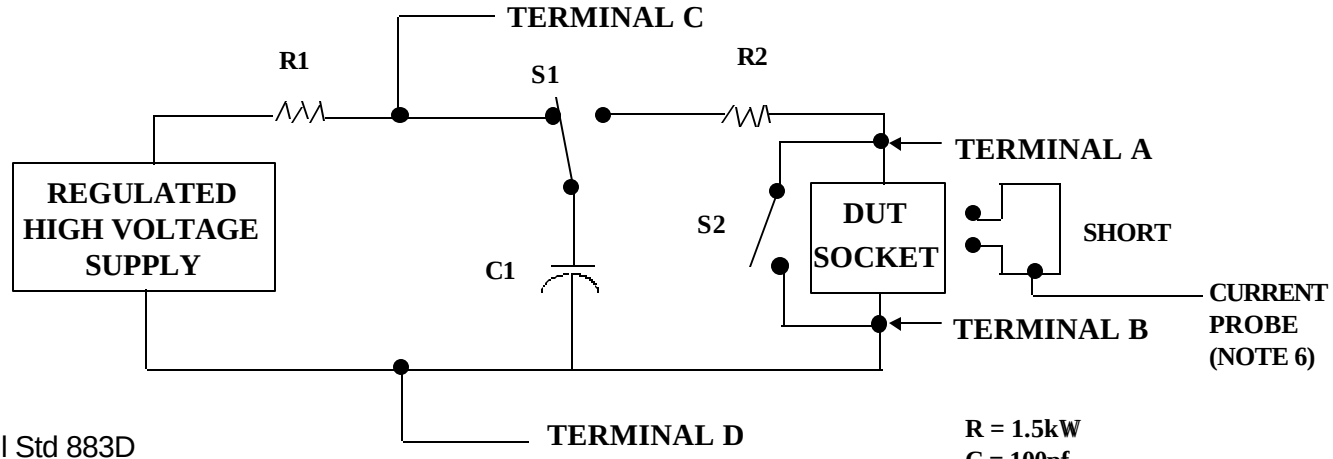
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

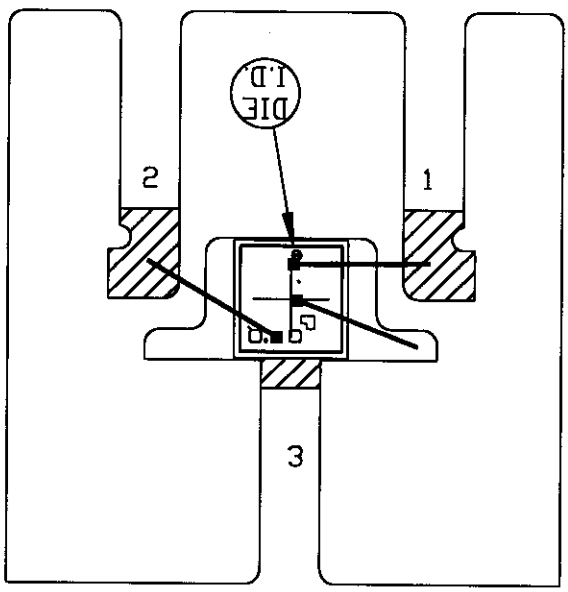
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

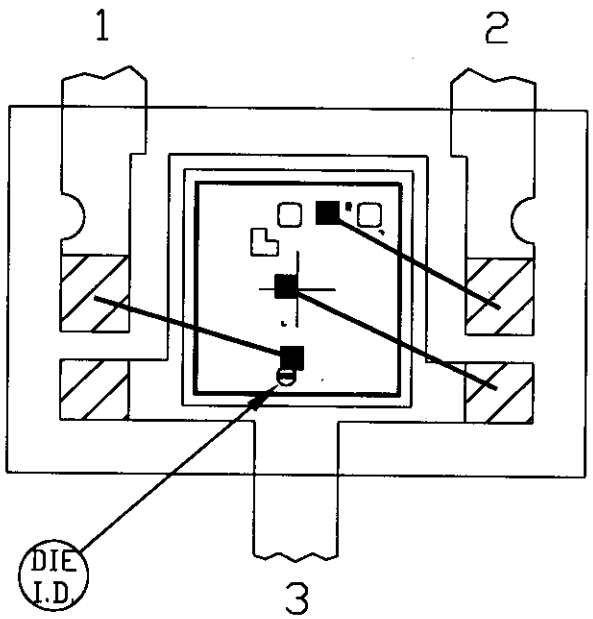


Mil Std 883D
Method 3015.7
Notice 8



USE NON-CONDUCTIVE EPOXY

PKG. CODE: U3-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 45X32	PKG. DESIGN			BOND DIAGRAM #: 05-0901-0156	REV: B



USE NON-CONDUCTIVE EPOXY

SCALE: 40x

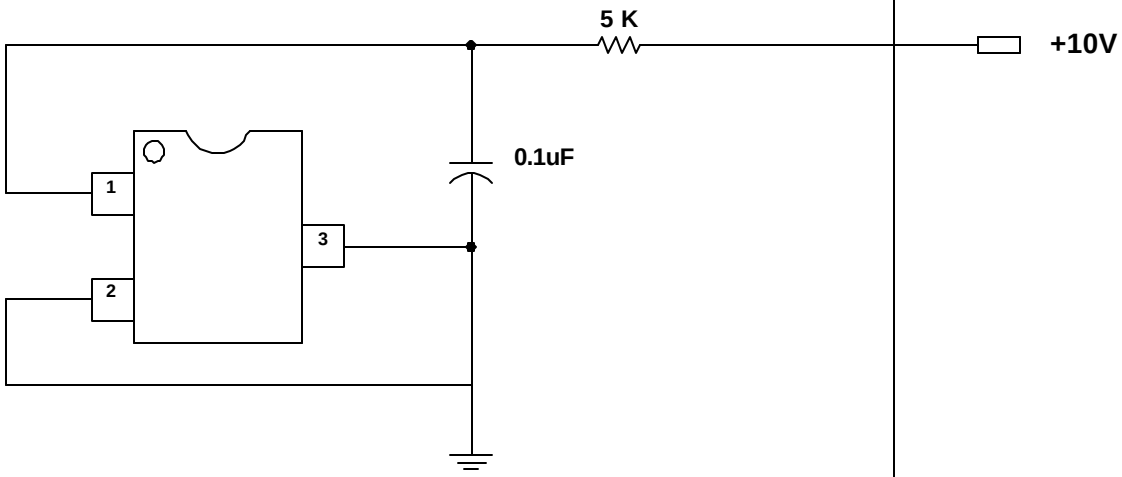
CAVITY DOWN

BONDABLE AREA

PKG. CODE: X3-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 34x35	PKG. DESIGN			BOND DIAGRAM #: 05-0901-0157 / REV: B

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: LM 4040 / 4041/MAX6138
MAX. EXPECTED CURRENT = 1.75 mA
PACKAGE: 3-SC70

DRAWN BY:
NOTES: