RELIABILITY REPORT

FOR

DS2477Q+T, DS2477Q+U

April 2, 2020

MAXIM INTEGRATED

160 RIO ROBLES

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Conclusion

The DS2477 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The DS2477 secure I2C coprocessor with built-in 1-Wire® master combines FIPS202-compliant secure hash algorithm (SHA-3) challenge and response authentication with Maxim's patented ChipDNA™ feature, a physically unclonable technology (PUF) to provide a cost-effective solution with the ultimate protection against security attacks. The ChipDNA implementation utilizes the random variation of semiconductor device characteristics that naturally occur during wafer fabrication. The ChipDNA circuit generates a unique output value that is repeatable over time, temperature, and operating voltage. Attempts to probe or observe ChipDNA operation modifies the underlying circuit characteristics thus preventing discovery of the unique value used by the chip cryptographic functions. The DS2477 utilizes the ChipDNA output as key content to cryptographically secure all device-stored data. With ChipDNA capability, the device provides a core set of cryptographic tools derived from integrated blocks including a SHA-3 engine, a FIPS/NIST compliant true random number generator (TRNG), 2Kb of secured EEPROM, and a unique 64-bit ROM identification number (ROM ID). The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. The DS2477 provides the SHA-3 and memory functionality required by a host system to communicate with and operate a 1-Wire SHA-3 slave. In addition, it performs protocol conversion between the I2C master and any attached 1-Wire SHA-3 slaves. For 1-Wire line driving, internal user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. The 1-Wire line can be powered down under software control. Strong pullup features support 1-Wire power delivery for commands that require higher current consumption.

II. Manufacturing Information

A. Description/Function:	DeepCover Secure SHA-3 Coprocessor with ChipDNA PUF Protection
B. Process:	TS18
C. Device Count:	599981
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 16, 2019

III. Packaging Information

A. Package Type:	6L TDFN
B. Lead Frame:	CU194
C. Lead Finish:	Matte Tin
D. Die Attach:	AB8200T
E. Bondwire:	0.8 mil Au
F. Mold Material:	G770HCD
G. Flammability Rating:	N/A
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	55 °C/W
J. Single Layer Theta Jc:	9 °C/W
K. Multi Layer Theta Ja:	42 °C/W
L. Multi Layer Theta Jc:	9 °C/W

IV. Die Information

A. Dimensions:	70X88.937 mils
B. Passivation:	SiN/SiO2

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ryan Wall (Manager, Reliability) Michael Cairnes (Executive Director, Reliability) Bryan Preeshl (SVP of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate λ is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192\ x\ 2454\ x\ 80\ x\ 2}$$ (Chi square value for MTTF upper limit)

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 24.3\ x\ 10^{-9}$$

$$\lambda = 24.3\ FITs\ (60\%\ confidence\ level\ @25°C)$$

Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at https://www.maximintegrated.com/en/support/qa-reliability/reliability/reliability-monitor-program.html.

TS18 cumulative process data

$$\lambda = 0.03\ FITs\ (60\%\ confidence\ level\ @25°C)$$
$$\lambda = 0.35\ FITs\ (60\%\ confidence\ level\ @55°C)$$

B. ESD and Latch-Up Testing

The DS2477 has been found to have all pins able to withstand an HBM transient pulse of ±2500 V per JEDEC / ESDA JS-001. Latch-Up testing has shown that this device withstands ±250 mA current injection and supply overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

DS2477

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 125°C Biased Time = 192 hrs.	DC parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.