RELIABILITY REPORT

FOR

DG419DY+T

PLASTIC ENCAPSULATED DEVICES

September 14, 2012

MAXIM INTEGRATED PRODUCTS

160 Rio Robles

San Jose, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The DG419DY+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

Maxim's redesigned DG417/DG418/DG419 precision, CMOS, monolithic analog switches now feature guaranteed on-resistance matching (3 max) between switches and guaranteed on-resistance flatness over the signal range (4 max). These switches conduct equally well in either direction and guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers low off-leakage current over temperature (less than 5nA at +85°C). The DG417/DG418 are single-pole/single-throw (SPST) switches. The DG417 is normally closed, and the DG418 is normally open. The DG419 is single-pole/double-throw (SPDT) with one normally closed switch and one normally open switch. Switching times are less than 175ns max for tON and less than 145ns max for tOFF. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. The improved DG417/DG418/DG419 are fabricated with a 44V silicon-gate process.

II. Manufacturing Information

A. Description/Function:	Improved, SPST/SPDT Analog Switches
B. Process:	S5HV
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Thailand, Philippines
F. Date of Initial Production:	October 27, 2001

III. Packaging Information

A. Package Type:	150 mil 8L SOIC
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0301-0611 / B
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	170°C/W
K. Single Layer Theta Jc:	40°C/W
L. Multi Layer Theta Ja:	132°C/W
M. Multi Layer Theta Jc:	38°C/W

IV. Die Information

A. Dimensions:	76 X 58 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S5HV Process results in a FIT Rate of 0.09 @ 25C and 1.55 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot N7J0AQ001S, Latch-up lot N7J0AQ001G D/C 0134)

The AG55 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

DG419DY+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	N7J0AQ001G, D/C 0134

Note 1: Life Test Data may represent plastic DIP qualification lots.