A Clean 12-Bit, 10Msps ADC

by Richard Reay and Dave Thomas

Introduction

As data conversion rates increase, it becomes difficult to find ADCs that have both good dynamic performance and clean linearity. An exception is the LTC1420, a 12-bit ADC that has excellent dynamics and linearity at sampling rates up to 10Msps, making it ideal for communications, scanners and high speed data acquisition. The versatile LTC1420 operates from either single 5V or ±5V supplies, making it easy to interface to single- or dual-supply systems. A programmable on-chip reference and a PGA input circuit give the user a wide selection of input ranges.

LTC1420 Features

❑ 10Msps sample rate

❑ Single 5 or ±5V supplies (250mW)

❑ 0.35LSB INL typical (1LSB max)

❑ 0.25LSB DNL typical (1LSB max)

❑ 71dB S/(N+D) and 83dB SFDR at 5MHz input

❑ 100MHz full-power-bandwidth sampling

❑ Input programmable gain amplifier
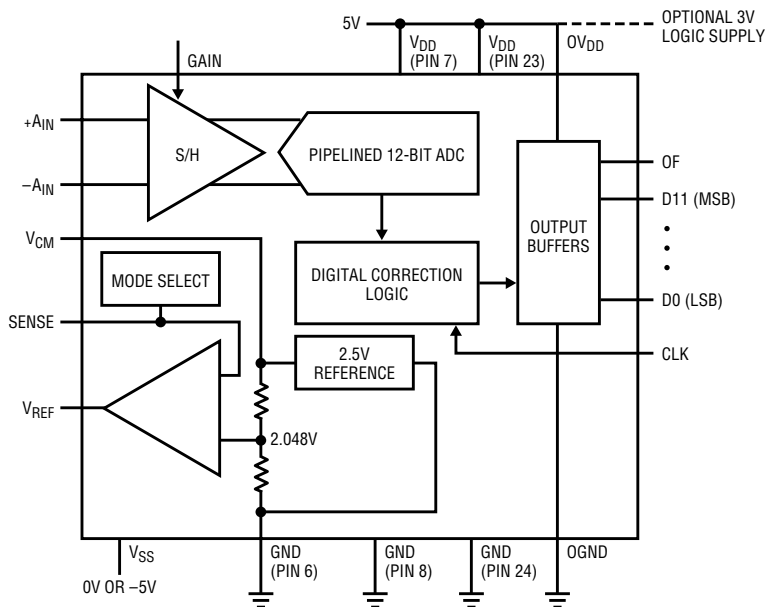
❑ Out-of-range indicator

❑ Small package: 28-pin narrow SSOP

Figure 1. The LTC1420 block diagram shows the 12-bit pipelined ADC core, programmable reference, input PGA and on-chip sample-and-hold.

Issue Highlights

The subject of our cover article this issue is the LTC1420, a 12-bit ADC with excellent dynamics and linearity at sampling rates up to 10Msps, making it ideal for communications, scanners and high speed data acquisition. The versatile LTC1420 operates from single 5V or ±5V supplies, making it easy to interface to single- or dual-supply systems. The LTC1420 features 0.35LSB INL, 0.25LSB DNL, 71dB S/(N+D) and 82dB SFDR at 5MHz input.

This issue also introduces another new ADC, the LTC1417. This 14-bit ADC samples at up to 400ksps while consuming just 20mW from a single 5V supply. It is easy to use, requiring little or no support circuitry in a wide variety of applications. Some of its key features include 400ksps throughput, 82dB SINAD and –95dB THD at Nyquist, 1.25LSB INL max and 1LSB DNL max.

This issue also debuts several new power products, including a low dropout linear regulator and two switchers.

The LT1761 is a new micropower low dropout regulator in a SOT-23 package with the lowest noise available from any LDO regulator. Designed to deliver 100mA of output current at a dropout of 300mV, the LT1761 fits well in many portable designs. The input voltage can range from 2V to 20V, allowing for a wide range of input supplies. Its low 20µA operating quiescent current is ideal for battery-powered applications.

The LTC1628 is the newest member of Linear Technology's third generation of DC/DC controllers. It uses a constant frequency, current mode architecture and Burst Mode™ operation similar to that of previous-generation LTC controllers, but with improved features. A key feature is control circuitry that drives the two top switches 180 degrees out of phase to minimize the input capacitance requirement *and* reduce conducted and radiated EMI. The resultant input ripple is effectively half the amplitude and double the frequency of nonphased

controllers, significantly reducing the input capacitance requirement. OPTI-LOOP™ compensation, 5V and 3.3V standby regulators, new protection circuitry, tighter load regulation and strong MOSFET drivers make these controllers ideal for current and future generations of CPU and/or system power applications.

The LT1576 is an improved version of the LT1376 constant frequency, current mode buck converter. With its 200kHz switching frequency and integral switch, only a few external, surface mount components are required to produce a complete switching regulator.

In the filter arena, we premier a pair of new monolithic linear-phase, DC-accurate, 10th order lowpass filter ICs: the LTC1569-6/LTC1569-7 are the first monolithic filters in the industry to provide accurate control of the cutoff frequency without the need for an external clock. A single external resistor programs internal precision circuitry, enabling the user to vary the filter cutoff frequency over eight octaves with a typical accuracy of ±3% or better.

Two new additions to LTC's interface product line are the LT1785 and LT1791 RS485/RS422 transceivers with ±60V fault tolerance. The high voltage fault tolerance of the LT1785 and LT1791 provides a highly reliable solution for data networking in high-risk environments.

Also included in this issue is a new special purpose device: the LT1684 ring-tone generator. This device is an isolated, pulse width modulated DAC with internal reference, output filtering and amplification, designed to ring telephones. Utilizing the robustness and voltage handling capability of two external MOSFETs, the LT1684 provides the precision voltage and current control required to fill the gap between microprocessors and phone lines. Ring frequency, amplitude, cadence and starting and stopping voltage points are controlled by the digital controller connected to the LT1684's input.

This issue includes a variety of Design Ideas, including three battery-related circuits, a single-supply application circuit for the LT1167 IA, a buck/boost converter based on the LTC1625 No R$_{SENSE}$ controller and two differential bridge digitizers for the LTC2400 delta-sigma converter. The issue concludes with a trio of New Device Cameos. *LT*

Flexible, Yet Easy to Use

The LTC1420 is a complete solution, with an on-chip sample-and-hold, a 12-bit pipelined ADC and a 15ppm programmable reference (Figure 1). The wideband sample-and-hold circuit can sample analog inputs beyond the Nyquist rate up to its 100MHz bandwidth. The sample-and-hold can operate with single-ended inputs or differential inputs with an outstanding CMRR of 75dB. A low impedance, 2.5V reference output is provided (V_{CM}); it can be used as the negative analog input for single-supply applications. The on-chip programmable reference can be set to 2.048V or 4.096V, or turned off so an external reference can be used.

The LTC1420 has the cleanest linearity of any ADC at this speed. Figures 2 shows typical linearity plots, with better than 0.35LSB INL and 0.25LSB DNL. The INL and DNL errors are guaranteed to be less than 1LSB over temperature for both single supply- and dual-supply applications.

The dynamic performance of the LTC1420 is exceptional, with typical values of 71dB S/(N+D) (signal-to-noise and distortion ratio) and 83dB SFDR (spurious free dynamic range) at Nyquist. The smooth linearity also gives clean dynamic performance with low level input signals, where performance can be degraded by the INL jumps and wobbles found in competitors' products (Figure 3). Figure 4 shows a 2048-point FFT plot of the LTC1420 with a 5MHz input signal.
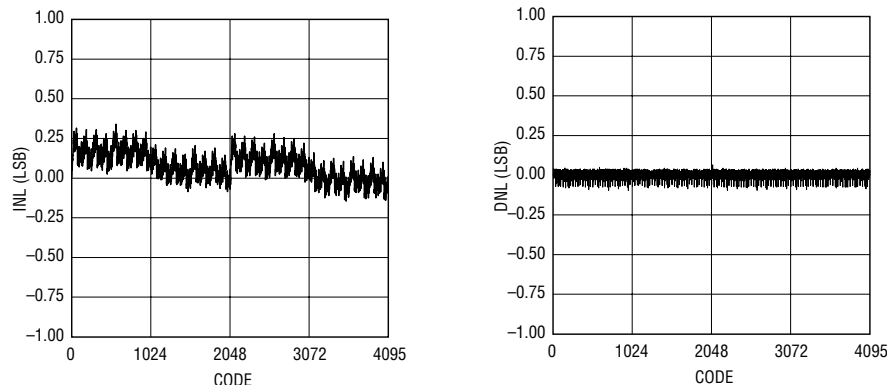
Single-Supply or Dual-Supply Operation

A single-supply ADC can be cumbersome to work within a dual-supply system. A signal with a common mode of zero volts has to be shifted up to the common mode of the ADC. Shifting the common mode voltage can be accomplished with AC coupling, but DC information is lost. Alternatively, an op amp level shifter can be used but this adds circuit complexity and additional errors. The LTC1420 can operate with dual supplies, allowing direct coupling to the input.

If a single supply is used, the dynamic performance of most ADCs is optimal when the common mode voltage of the input signal is at midsupply (2.5V). To generate this voltage, competitors' products require an external voltage reference or external resistors and capacitors. The LTC1420 is much easier to use: simply connect A_{IN}^- to the 2.5V V_{CM} pin. In dual-supply applications, A_{IN}^- can be connected directly to ground. AC coupling signals to the LTC1420 is also easy. All of these modes are shown in Figure 5.

Programmable On-Chip Reference

The LTC1420 has two reference pins, V_{CM} and V_{REF}, and a reference programming pin, SENSE. V_{CM} is a low impedance 2.5V pin that can be used as the common mode input voltage. The voltage at the V_{REF} pin sets the input span of the ADC to $\pm V_{REF}/2$. If the SENSE pin is connected to V_{REF} or
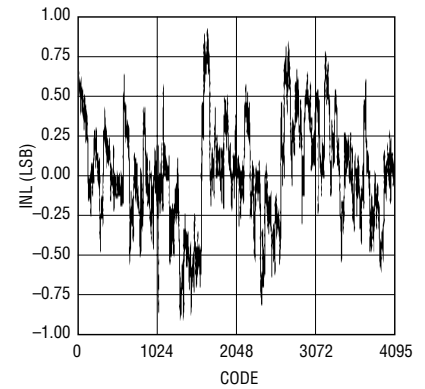
Figure 3. Typical INL for a competitor's 12-bit, 10Msps ADC; Small input signals near the large jumps and wobbles in the INL will have poor dynamic performance. The clean INL of the LTC1420 prevents this problem.

ground, internal circuitry converts the 2.5V reference to either 2.048V or 4.096V at the V_{REF} pin. With a temperature coefficient of 15ppm/°C, both V_{CM} and V_{REF} are suited to serve as the master reference of the system. However, if an external reference is required, tie SENSE to V_{DD} and the on-chip reference amplifier will be turned off and V_{REF} can be directly driven by an external reference.

Pipelined Architecture for High Speed

A/D converters with the cleanest performance are usually made with nonpipelined successive approximation (SAR) based architectures. This is because pipelined converters usually have errors that occur when information is passed from stage to stage in the pipeline. Despite this drawback, pipelining is necessary to obtain high conversion rates. The LTC1420 solves this problem by using a proprietary pipelined architecture that is fast but has accuracy similar to that of slower SAR-type converters. With the LTC1420 you get fast, clean performance without the headache of complicated, time-consuming self-calibration.

Figure 6 shows the timing diagram for the LTC1420. The rising edge of CLK begins a conversion and the digital outputs are updated 70ns later. As with all pipelined ADCs, there is latency in the output data. Output data is updated from the LTC1420 two clock cycles plus 70ns after the

Figure 2. Typical INL (left) and DNL (right) of the LTC1420; the INL/DNL are 0.35LSB/0.25LSB typical and 1LSB max over temperature.
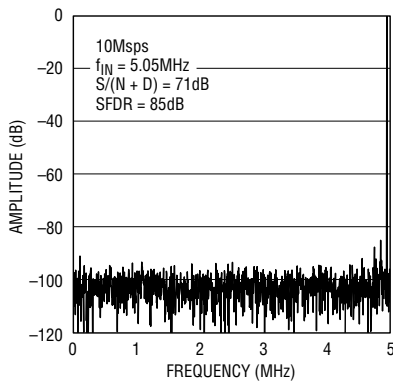
Figure 4. A 2048-point FFT plot of the LTC1420 at 10Msps for a 5.05MHz input signal; the SNR is 71.2dB, SFDR is 85.1dB, THD is –82.4dB and S/(N + D) is 70.9dB.

input is sampled, so data can be correctly latched on the third rising edge after the conversion starts.

Easy Interface to 5V or 3V Systems

Another nice feature of the LTC1420 is its dedicated pin for the digital output supply (OV$_{DD}$). This supply can be set to 5V or 3V, allowing direct interface to 3V systems. Some competitors' parts support only 5V digital outputs, requiring level-shifting circuitry when interfacing to a 3V system. If 5V digital outputs are desired, OV$_{DD}$ can simply be shorted to V$_{DD}$ to save a bypass capacitor.

Small Footprint

A tiny package and minimal external components make the LTC1420 the smallest 12-bit 10Msps solution on the market. Its 28-pin narrow SSOP package is just 0.09in^2, and only four to five 1μF ceramic chip bypass capacitors are needed. Competitors' parts come in larger packages and can require ten to fifteen bypass capacitors, resistor dividers, external voltage references and op amp level shifters.
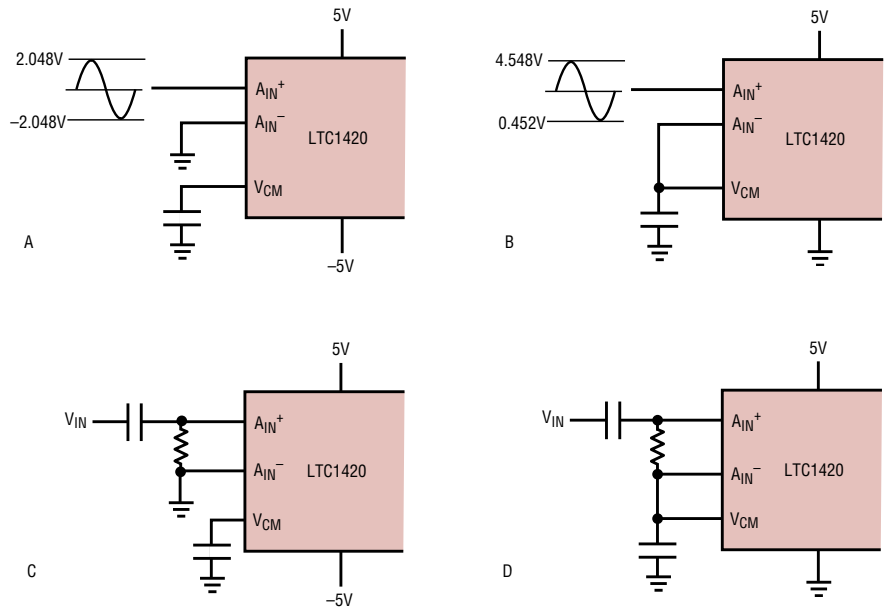
Figure 5. It is simple to directly connect a single-ended signal for a dual-supply (A) or single-supply (B) system (V$_{REF}$ = 4.096V). AC coupling the LTC1420 is also straightforward (C, D).

	MIN	TYP	UNITS
t$_{CLOCK}$	100	—	ns
t$_H$	20	50	ns
t$_L$	20	50	ns
t$_{CONV}$	—	70	ns
t$_{ACQ}$	—	30	ns
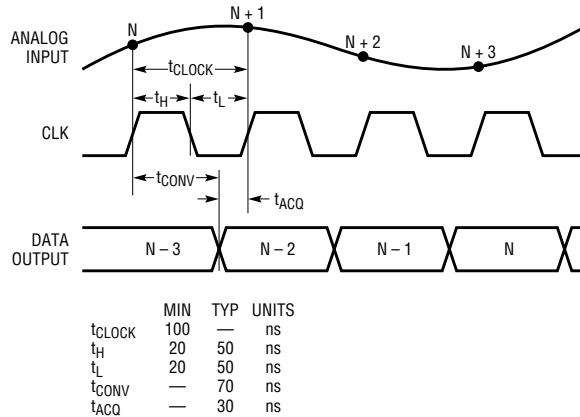
Figure 6. This timing diagram shows two cycles of pipeline delay. The sample is taken on the rising clock edge. Data is available on the third following rising edge.

Conclusion

The LTC1420 is a simple, flexible 12-bit 10Msps ADC that is easy to use. It has the clean linearity and dynamic performance of a SAR-type ADC at the conversion speed of a pipelined converter. With its high performance and tiny footprint, it is a clear solution for high speed data acquisition. *LT*

Micropower LDO Has the Lowest Noise and Quiescent Current in SOT-23

by Todd Owen

Introduction

A cell phone rings, a pager beeps. Wireless communications devices are everywhere. These RF circuits have a myriad of power supply requirements. Most important in many applications is low noise operation, to prevent unwanted sidebands on RF amplifiers. Second is low power operation, which translates directly to extended operating time in battery-powered devices. In addition, portability requires small size, which makes small packages for regulators and stability with small surface mount ceramic capacitors a plus. Another factor that can weigh in is low voltage operation, both for the input and output. Satisfying all of these needs at once can be a difficult challenge.

New LDO Makes a Quiet Entrance

Figure 1 shows a typical application for the LT1761, a new micropower low dropout regulator in a 5-lead SOT-23 package with the lowest noise available from any LDO regulator. Designed into the regulator are many other features that make it useful in a variety of applications. It is stable with a wide range of output capacitors. Small ceramic capacitors can be used without the necessary addition of series resistance as is common with other regulators. The output capacitor can be as low as 1µF, with an ESR in the range from milliohms up to 3 ohms. For low noise operation, the addition of a small bypass capacitor from the output to the BY-

Table 1. Evaluation of available SOT-23 low noise, low dropout regulators

Part	Quiescent Operating Current	Output Voltage Noise (Specified with Bypass Cap)	Output Voltage Noise (Measured with Bypass Cap)	Output Voltage Noise (Measured, No Bypass Cap)
Competitor 1 (5V Output)	80µA	$260nV/\sqrt{Hz}$[1]	$100µV_{RMS}$	$245µV_{RMS}$
Competitor 2 (5V Output)	95µA	$30µV_{RMS}$	$55µV_{RMS}$[2]	$340µV_{RMS}$
Competitor 3 (3.3V Output)	85µA	$30µV_{RMS}$	$30µV_{RMS}$	$265µV_{RMS}$
Linear Technology LT1761	20µA	$20µV_{RMS}$ (1.22V)	$15µV_{RMS}$ (1.22V)	$56µV_{RMS}$ (1.22V)
		$20µV_{RMS}$ (3.3V)	$16µV_{RMS}$ (3.3V)	$110µV_{RMS}$ (3.3V)
		$20µV_{RMS}$ (5V)	$18µV_{RMS}$ (5V)	$135µV_{RMS}$ (5V)

1. The data sheet specification is $260nV/\sqrt{Hz}$, with no spot frequency given.
2. Measurement on the bench is over the 10Hz–100kHz frequency range, where $30µV_{RMS}$ is specified in the data sheet over the 300Hz–50kHz frequency range.

PASS pin can reduce output voltage noise to $20µV_{RMS}$ over the 10Hz to 100kHz frequency range. However, when using a noise bypass capacitor, it is recommended that a minimum output capacitor of 3.3µF be used.

Designed to deliver 100mA of output current at a dropout of 300mV, the LT1761 fits well in many portable designs. The input voltage can range from 2V to 20V, allowing for a wide range of input supplies. Its low 20µA operating quiescent current is ideal for battery-powered applications. This quiescent current is well controlled; it does not rise excessively in dropout as happens with many competing regulators. The part also has a low power shutdown state: with the shutdown pin pulled high, the LT1761 will

provide a regulated output; when the shutdown pin is pulled to ground, all quiescent current from the input and shutdown pins is reduced to the leakage currents of the internal transistors. This leakage current, typically a few nanoamperes at room temperature, stays below 1µA over the operating temperature range. Competing devices may be able to match the shutdown quiescent current, but operating quiescent current is improved by a factor of four.

The LT1761 has a number of protection features to safeguard itself and sensitive load circuits. The device is protected against reverse input voltages, which is useful in situations where a battery might be connected backwards. No external protection diodes are needed when using the LT1761. With a reverse voltage from output to input, the LT1761 acts as if it has a diode in series with its output and prevents reverse current flow. In dual-supply applications where the regulator load is returned to a nega-
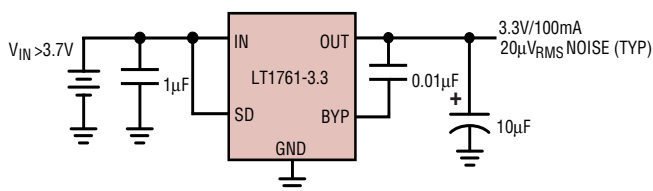
Figure 1. New low noise, low dropout, micropower regulator

E_{NOISE}
100µV/DIV

1ms/DIV
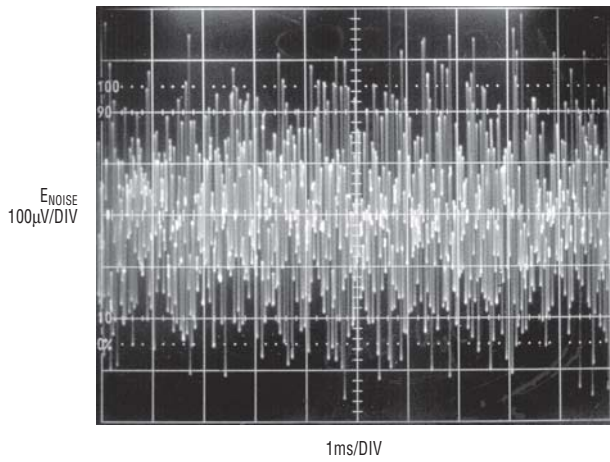
Figure 2. Competitor #1's peak-to-peak output voltage noise (5V output)

E_{NOISE}
100µV/DIV

1ms/DIV
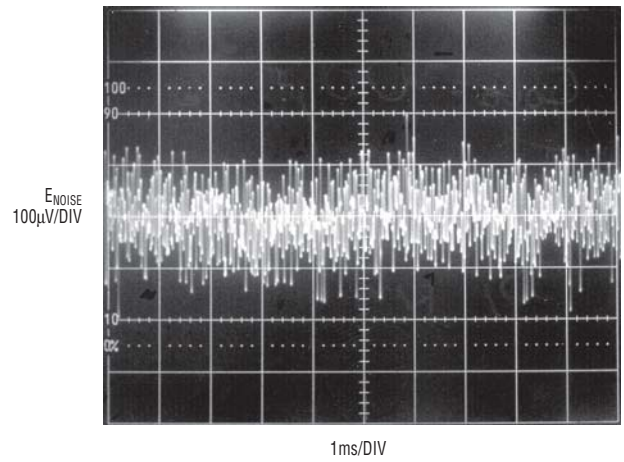
Figure 3. Competitor #2's peak-to-peak output voltage noise (5V output)

E_{NOISE}
100µV/DIV

1ms/DIV
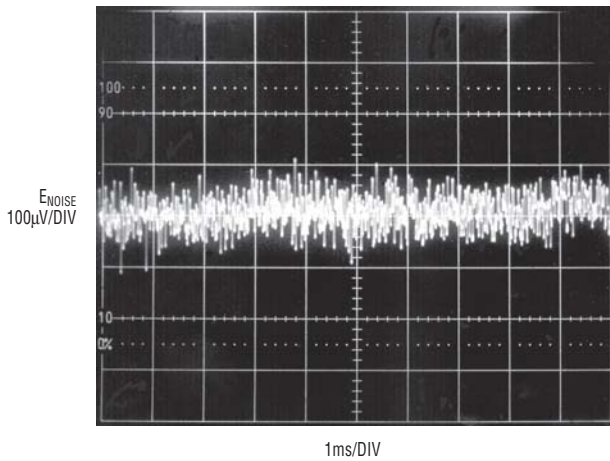
Figure 4. Competitor #3's peak-to-peak output voltage noise (5V output)

E_{NOISE}
100µV/DIV

1ms/DIV
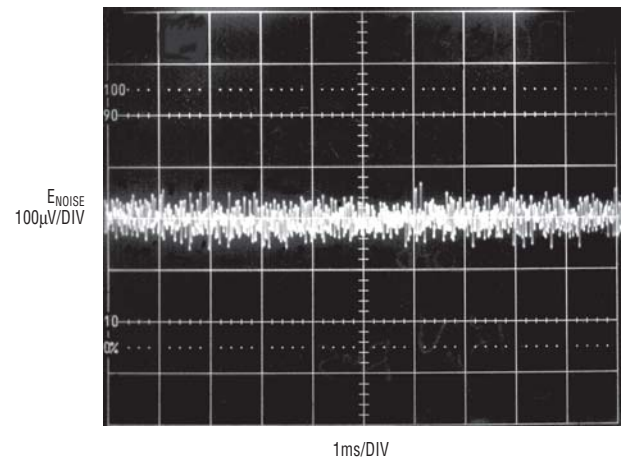
Figure 5. LT1761-5 output voltage noise

E_{NOISE}
100µV/DIV

1ms/DIV
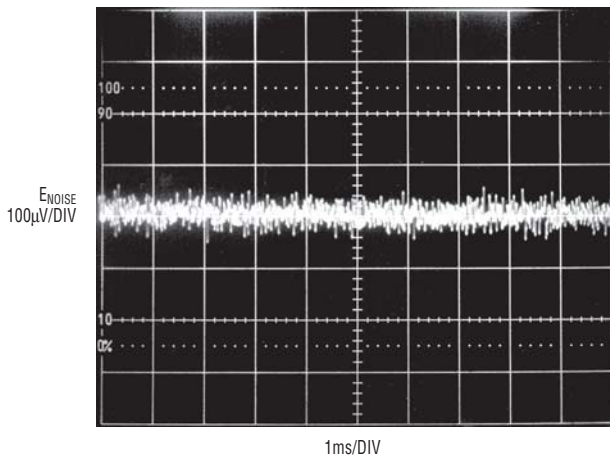
Figure 6. LT1761-3.3 output voltage noise

E_{NOISE}
100µV/DIV

1ms/DIV
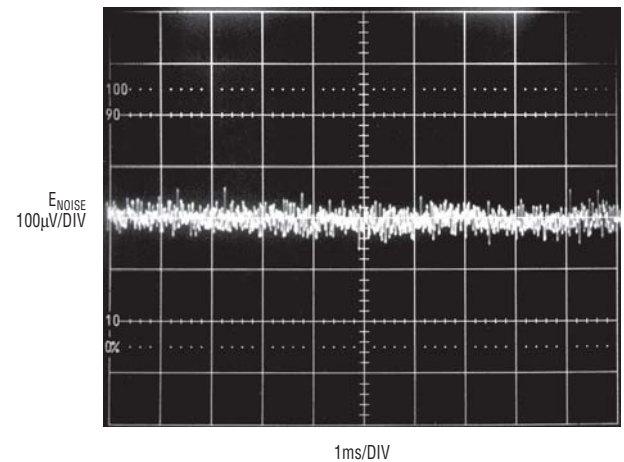
Figure 7. LT1761-BYP output voltage noise (V_{OUT} = 1.22V)

tive supply, the output can be pulled below ground by several volts and the device will still start and operate. These features are in addition to standard protection features for linear regulators, such as current limiting and thermal limiting.

The LT1761 regulators are available in several fixed voltage options as well as two different adjustable versions. Fixed voltage options include 2.5V, 3V, 3.3V and 5V. The adjustable versions of the LT1761 are available with a reference voltage of 1.22V and a mini-

mum input operating voltage of 2V. The adjustable LT1761 has to sacrifice one of the function pins to bring out the adjust pin. For the LT1761-SD, the SHUTDOWN pin remains while the BYPASS pin has been removed. This allows the regulator to be
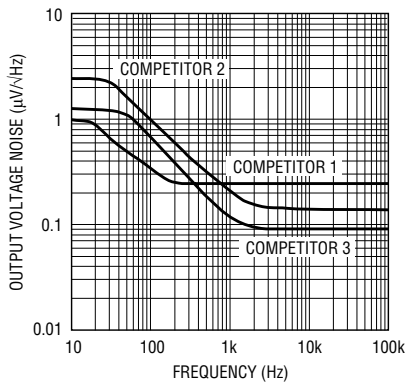
Figure 8. Competing devices' noise spectral density

operated normally, with the exception that noise reduction cannot be achieved. For the LT1761-BYP, the BYPASS pin has been brought out to allow for low noise operation with the addition of a small capacitor. The shutdown pin is internally tied to the input to ensure that the regulator will operate normally with the minimum operating voltage.

How Does It Measure Up?

There are a number of low noise, low dropout regulators in SOT-23 packages on the market. The LT1761 gives many performance advantages over the competition. Comparisons based on data sheet specifications can be difficult and confusing, since many manufacturers specify different measurement methods and frequency ranges. Table 1 summarizes the distinctions between the parts to help designers make a quick comparison.

These parts were compared on the bench side by side. This A/B comparison eliminates any variations in test equipment or measurement methods. All measurements were taken with a 50mA load, 10μF output capacitor and the manufacturer's maximum recommended noise capacitor (0.01μF). Noise was measured using a noise amplifier with a gain of 60dB (the amplifier adds $0.5\mu V_{RMS}$ of noise into the measurement, providing accuracy within 0.5% for a $20\mu V_{RMS}$ noise signal). The noise was amplified to eliminate any noise added by the instrumentation used for measurements.

Noise measurements given as RMS values over a frequency bandwidth may often not provide enough information to decide on a regulator for your design. Figures 2 through 7 show peak-to-peak noise for the regulators showcased in the article. Again, the devices were tested with identical 10μF output capacitors, the manufacturer's recommended maximum 0.01μF bypass capacitor and identical 50mA loads. The difference in performance is readily apparent.

Finally, Figures 8 and 9 show noise spectral density over the 10Hz to 100kHz range for the parts. These curves show the dramatic difference that the LT1761's unique architecture makes in reducing output voltage noise. Noise over the entire frequency range is reduced, providing an exceptionally quiet output. By any of these
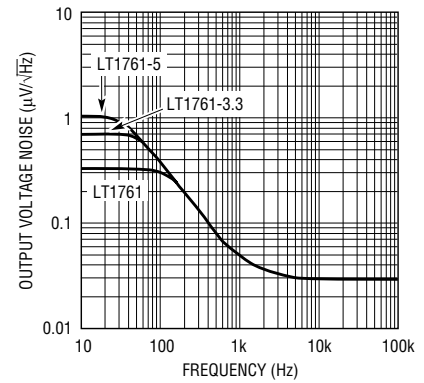
Figure 9. LT1761 noise spectral density

measurement methods, the LT1761 offers the lowest noise available.

Other Performance Advantages

The unique internal architecture of the LT1761 provides other performance advantages. For transient performance, Figure 10 shows two photos of a 10mA to 100mA transient load step on the 5V output of the LT1761. This test was done with 6V on the input and 10μF capacitors on both input and output. The only difference in test conditions between the two is the addition of a 0.01μF bypass capacitor to lower the output voltage noise. The difference in circuit response is readily apparent. The LT1761 also allows for direct connection of the output to the adjust pin, which provides a minimum 1.22V regulated output. Competing devices are either unavailable in adjustable versions or require some minimum
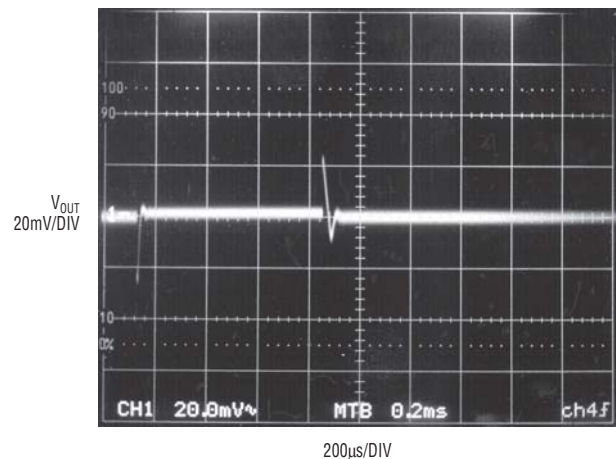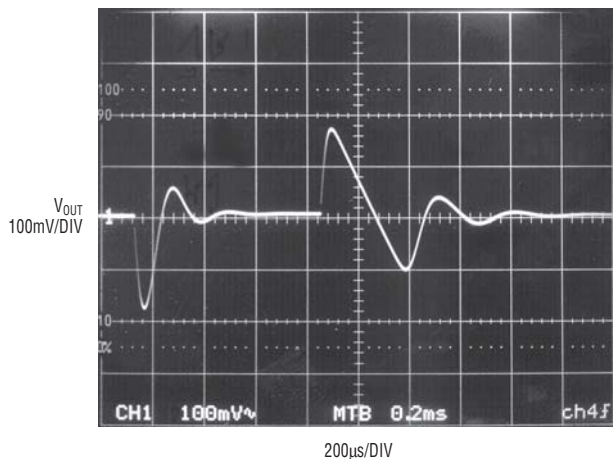
Figure 10. Before and after photos show dramatic improvement in transient response after the addition of a 0.01μF bypass capacitor. Note the change in voltage scale

The LT1576: 200kHz, 1.5A Monolithic Buck Converter

by Lenny Hsiu

Introduction

The LT1576 is an improved version of the LT1376 1.5A buck switching regulator from Linear Technology. With its 200kHz switching frequency and integral switch, only a few external, surface mount components are required to produce a complete switching regulator. All the features of the LT1376 have been retained, including current mode control, external synchronization and a low current (typically 20µA) shutdown mode. Improvements have been made to reduce the start-up input supply headroom and the switching noise. The quiescent current has been reduced by one half. The feedback voltage has been lowered from 2.42V to 1.21V for low output voltage applications. Improved power-device layout also lowers the equivalent resistance of the on-chip switch from 0.3Ω to 0.2Ω.

LT1576 Features

❏ Constant 200kHz switching frequency
❏ 0.2Ω high speed switch
❏ 20µA shutdown current
❏ Uses all surface mount components
❏ Cycle-by-cycle current limiting
❏ Easily synchronizable
❏ Available in the SO-8 package

Circuit Description

The LT1576 is a constant frequency, current mode buck converter. As shown in Figure 1, an internal clock and two feedback loops control the duty cycle of the power switch. In addition to the normal output error amplifier, a current sense amplifier monitors switch current on a cycle-by-cycle basis.

A switch cycle starts with an oscillator pulse that sets the RS flip-flop to turn the switch on. When the switch current reaches a level set by the output of the error amplifier (that is, the V_C pin), the flip-flop is reset and the switch turns off. The power stage is, in effect, turned into a programmable current source. The output current, in turn, is controlled by the error amplifier in response to changes in the output voltage.

This current mode technique means that the error amplifier controls the current delivered to the output rather than the voltage. Current mode control gives pulse-by-pulse current limiting and eases frequency com-
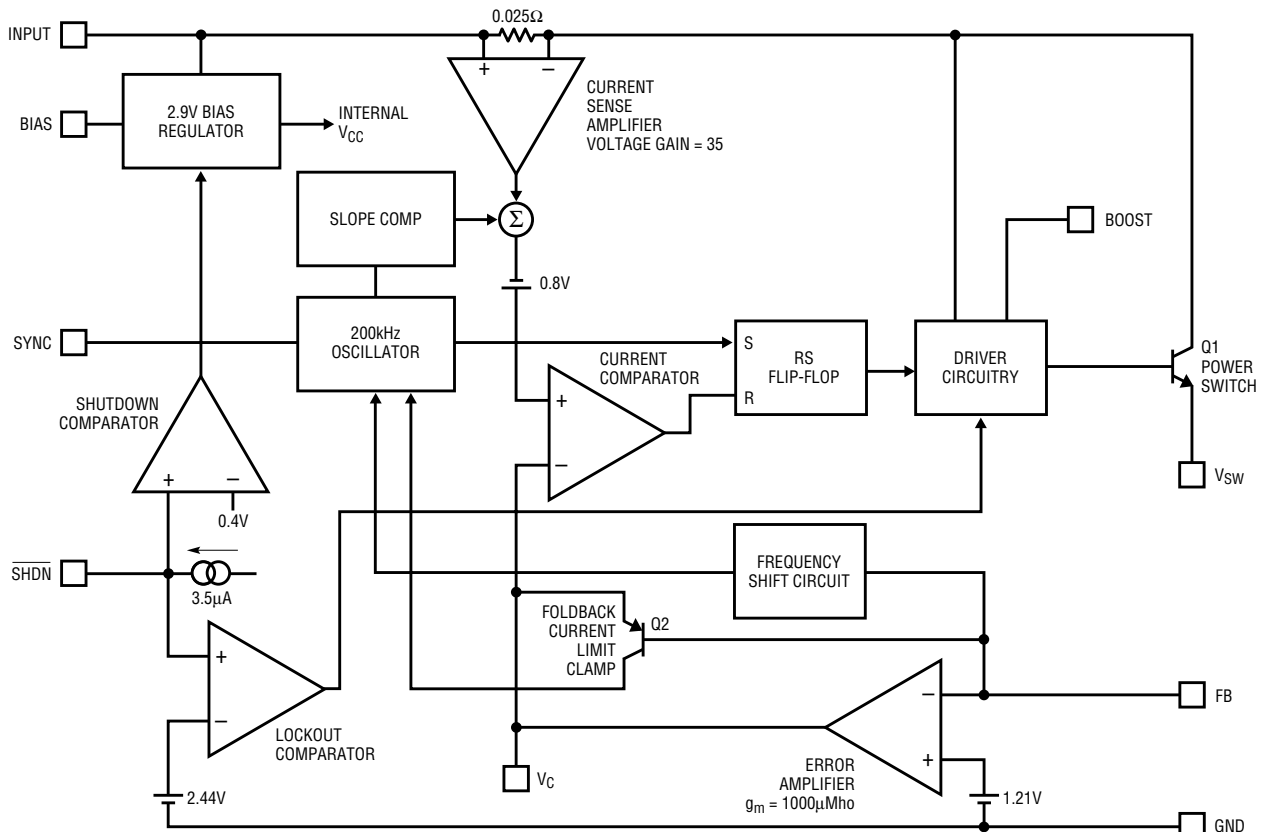
Figure 1. LT1576 block diagram
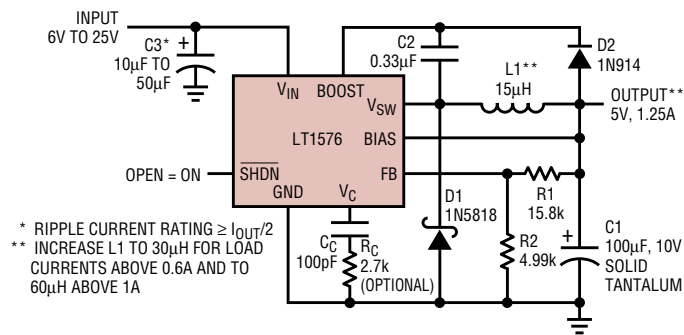
Figure 2. 5V/1.25A buck converter

pensation. A voltage mode control system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. A current mode control system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response. Nonlinear slope compensation has been added to the current sense signal to prevent the subharmonic oscillation associated with current mode control when the regulator duty cycle is greater than 50%.

In addition to providing the output voltage feedback path to the internal error amplifier, the feedback pin, FB, provides several overload-protection functions. As the feedback pin voltage drops below 0.7V a voltage clamp is gradually applied to the V_C pin, which reduces the switch current limit. Additionally, the oscillator frequency is gradually reduced to about 40kHz, which is one-fifth of the nominal 200kHz switching frequency. Because the minimum on-time for the switch remains the same, the minimum duty cycle is effectively reduced by a factor of five. This lowers the power dissipation for a shorted output condition in both the LT1576 and the catch diode, D1, shown in Figure 2. During power-up, the frequency foldback and current-limiting features of the FB pin provide a soft-start function.

High switch efficiency is attained by using the Boost pin to provide a voltage to the switch driver that is higher than the input voltage, allowing the switch to saturate. This boosted voltage is generated with an external capacitor, C2, and a diode, D2, as shown in Figure 2. The minimum boost voltage required to fully saturate the switch at maximum current has been reduced from 3.5V (LT1376) to 3V. Current used by the boost circuit is considered an efficiency loss. Supplying current from a lower voltage via the boost diode, D2, improves the efficiency. For most applications with outputs above 3V, the configuration shown in Figure 2 is optimal. Converters with lower output voltages should use the input or an alternate supply to power the boost diode.

Compared to the LT1376, the LT1576 has been improved by reducing the minimum start-up voltage at low output currents. At low output currents, there is not enough energy in the inductor at switch-off to drive the switch-node capacitance to ground. In this case, the minimum start-up voltage is the unboosted voltage drop across the output switch. Improvements made to the drive circuitry of the LT1576 have reduced this drop from 2.5V on the LT1376 to 1.5V.

The switch transition time for the LT1576 is increased to 60ns from the LT1376's 16ns to reduce EMI and RFI without sacrificing efficiency. First, its switching frequency has been lowered to 200kHz (that of the LT1376 is 500kHz); second, efficiency is boosted by reducing the quiescent current to 1.35mA from the LT1376's 2.5mA, and by reducing the switch on-resistance from 0.3Ω to 0.2Ω.

Most of the circuitry of the LT1576 operates from an internal 2.9V bias supply. The bias regulator normally draws power from the regulator input pin, but if the bias pin is connected to an external voltage higher than 3V, bias power is drawn from the external source (typically the regulated output voltage). This improves efficiency if the bias pin voltage is lower than regulator input voltage.

On some versions of the LT1576, an external clock signal (up to 400kHz) can be fed into the SYNC pin to increase the internal oscillator frequency or synchronize it to a system clock. The synchronization feature is defeated when the FB pin voltage is below 0.7V. This allows the frequency foldback function to work during start-up.

Two comparators are connected to the shutdown pin. The first comparator, with a threshold of 2.44V, disables the output switch and can be used as an undervoltage lockout level. The second comparator, with a threshold of 0.4V, puts the device into a low quiescent current shutdown state, where quiescent current drops to just 20μA.

Typical Application: 5V/1.25A Buck Converter

Figure 2 shows a typical buck converter using the LT1576 with a 6V to 25V input range, a 5V output and 1.25A output current capability. Due to the low on-resistance of the on-chip switch, the converter efficiency remains high over a wide range of output currents, as shown in Figure 3. To achieve high efficiency, both the BIAS pin and the boost circuit are powered from the 5V output.

The choice of the surface mount inductor, L1, is affected by several factors, including the maximum current, core and copper losses, size and cost. A high value, high current inductor gives the highest output current with the lowest ripple, at the expense of a large physical size and cost. Lower inductance values tend to be physically smaller and have higher current ratings. They are less expensive, but the output ripple current, and hence the output ripple voltage, increases.
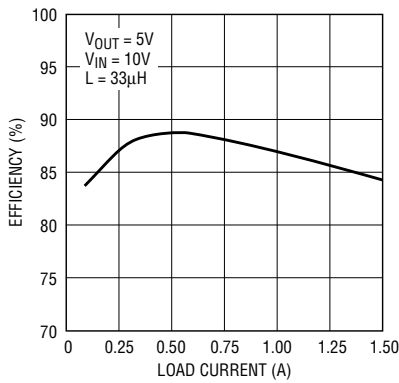
Figure 3. Efficiency of Figure 2's circuit

The input capacitor C3 must be rated to absorb all switching current ripple. The ripple current can be as high as $I_{OUT}/2$, so low ESR tantalum capacitors are needed. The ripple current rating on the input capacitor must be observed to ensure reliable operation. The ripple current at the output capacitor is lower, but its ESR still needs to be low to limit the output ripple voltage.

The voltage drop across the catch diode D1 has a significant effect on overall converter efficiency, especially at higher input voltages when the switching duty cycle is low. For good electrical performance, D1 must be placed close to the LT1576.

Loop Compensation

For most LT1576 applications, the suggested frequency compensation is a 100pF capacitor (C_C) from the V_C pin to ground. The following description of the loop frequency response characteristics is provided as an aid in optimizing loop compensation.

In an LT1576 closed-loop regulator system, two low frequency poles are formed by the output capacitor and the compensation capacitor. A high frequency zero is formed by the output capacitor and its ESR. The location of this zero varies with the type of output capacitor. To stabilize the regulator, this zero must bring the loop phase up before the phase contributed by the two low frequency poles reaches –180° at unity gain. If loop stability must be improved, another high frequency zero can be formed by adding a resistor, R_C, (typically around 3k) in series with compensation capacitor C_C (see Figure 2). The unity-gain phase margin can be adjusted by changing the value of R_C (and hence, the location of the zero). Although it solves the loop-stability problem, this added resistor occasionally causes a large-signal subharmonic problem in the control loop. The output ripple voltage feeds back through the error amplifier to the V_C pin, changing the current trip point of the next cycle. Changing the value of R_C also changes the high frequency gain of the error amplifier. If the loop frequency response gain at the switching frequency is high enough, the output ripple voltage can appear at the V_C pin with enough amplitude to interfere with the proper operation of the regulator. This sub-harmonic problem can be solved by adding a second capacitor—typically from 1nF to 3nF—directly from the V_C pin to ground to form a pole at one-fifth the switching frequency. This capacitor provides significant attenuation of the switching ripple but does not add unacceptable phase shift at the loop's unity-gain frequency.

PCB Layout

All high current, high speed circuits require careful layout to obtain optimum performance. When laying out the PCB, keep the trace length around the high frequency switching components, shown in Figure 4, as short as possible. This minimizes the EMI and RFI radiation from the loop created by this path. These traces have a parasitic inductance of approximately 20nH/inch, which can cause an additional problem at higher operating voltages. At switch-off, the current flowing in the trace inductance causes a voltage spike. This is in addition to the input voltage across the switch transistor. At higher currents, the additional voltage can potentially cause the output switching transistor to withstand more than its absolute maximum voltage rating.

Conclusion

The LT1576 makes a very compact, low parts count, 1.5A DC/DC converter without the need for separate control and power devices. Compared to the existing LT1376, this new part has been improved to reduce the start-up input supply headroom and switching noise. The quiescent current has been reduced from 2.5mA to 1.35mA. Improved power-device layout also lowers the on-chip switch on-resistance from 0.3Ω to 0.2Ω. Because of the former two factors, efficiency is greatly improved. Additionally, the feedback voltage has been lowered from 2.42V to 1.21V, which will meet the requirements for lower output voltage applications. *LT*
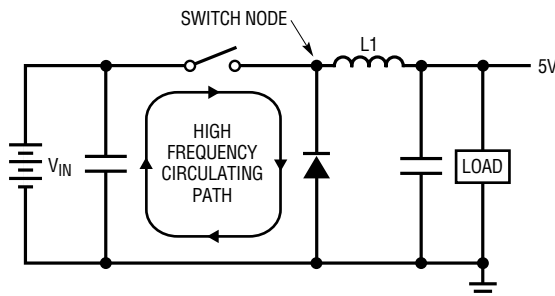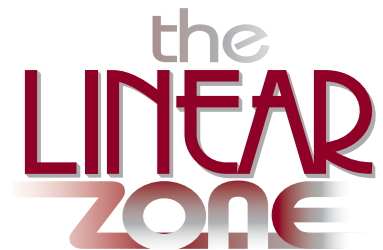

Figure 4. High speed switching path

The LT1684 Solves the Global Ringing Problem

by Dale Eagar

Ring generators are sine wave output, high voltage inverters for the express purpose of ringing telephone bells. In decades past, the phone company generated ring tones with motor generator sets, with the capacity to ring many phones simultaneously. The most common frequency used to ring telephones is 20Hz, while 16Hz and 24Hz are also widely used. The output voltage is about 90V with less than 10mA-per-bell output current capability. Since the power supplied is low, one would think that the task is minimal. However, there are several things that complicate matters:

❏ The output needs to be DC coupled to make detection of the off-hook condition possible.

❏ If the ring signal has to go out over any significant length of wire, there is potential for crosstalk and EMI if the ring signal is not low distortion and free of digital noise.

❏ The output needs to be current limited.

❏ The output needs to be robust, because lightning, static discharge and line faults impose ugly transients on a ring generator's output.

❏ If the output is to drive a FAX machine or modem, it needs to have sufficient peak voltage to trip the ring-detect circuit on the most conservative unit (a 35V square wave will ring just about any phone but hardly any modems).

❏ All but the simplest systems need isolation of the ring generator output from the digital logic initiating the ring.

❏ In designs where Caller ID is required, output noise can become an issue.

What is needed for most systems is a high voltage, robust, clean, isolated
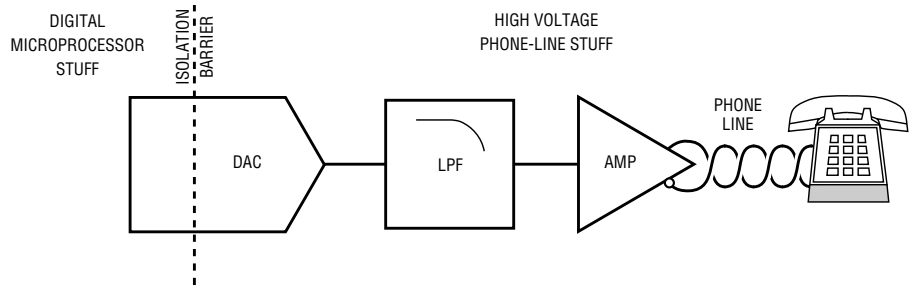
Figure 1. The LT1684 incorporates all of the functions required to go from bits to bells.

DAC that has output smoothing for harmonic suppression.

Introducing the LT1684

The LT1684 is an isolated, pulse width modulated (PWM) DAC with internal reference, output filtering and amplification (see Figure 1). Utilizing the robustness and voltage handling capability of two external MOSFETs, the LT1684 provides the precision voltage and current control required to fill the gap between microprocessor and phone line.

Ring frequency, amplitude, cadence and starting and stopping voltage points are controlled by the digital controller connected to the LT1684's input. In addition to providing the correct frequency and voltage to ring phones in systems all around the globe, this approach allows implementation of Caller ID, cadencing and the simultaneous ringing of multiple phone lines.

The Circuit Guts

The LT1684 uses several novel circuit concepts to perform its seemingly magic task. While providing precision control of the ring-signal voltage and current, the LT1684 IC doesn't need to actually handle the enormous voltages involved (Figure 2). The digital input is isolated by coupling the pulse width modulated signal differentially through RC networks (R1 and R2 and C1 and C2 in Figure 2). The input characteristics of the differential receiver allow fault-free digital isolation even while sustaining large common mode voltages across the isolation barrier.

With the input resistors and capacitors, the LT1684's digital inputs are well protected against kilovolts of static discharge. Although normally

Figure 2. The LT1684 controls its output over hundreds of volts while operating in a ±12V window.

Figure 3. LT1684 typical application

driven by CMOS inverter outputs, this circuit can be driven from a distance by an RS422/RS485 differential line driver such as the LT1785, with only a 2-wire connection.

The filter/amplifier in the LT1684 is a 2nd order multiple feedback (MFB) lowpass filter. This topology was derived from a unique inside-out circuit transformation of the standard textbook MFB filter. More details of this transformation can be found on the LT1684 data sheet and in *Linear Technology* VI:2 (May 1996).

The DAC in Figure 2 is implemented by a novel bidirectional bandgap reference that outputs either 1.25V or –1.25V depending on the state of the output of the differential receiver. This bandgap output is referenced to the output pin of the LT1684 and is available on the BG_{OUT} pin. Referring to

Figure 3, the bidirectional bandgap output is applied to the input of the 2nd order MFB lowpass filter/amplifier through R3. R3–R5 and C3–C4 set up the gain and corner frequency of the filter/amplifier. C5–C8 are compensation capacitors for the amplifier. R6, D1 and D2 are for protection from lightning. R8 and R9 subdue the high frequency MOSFET demons in Q1 and Q2.
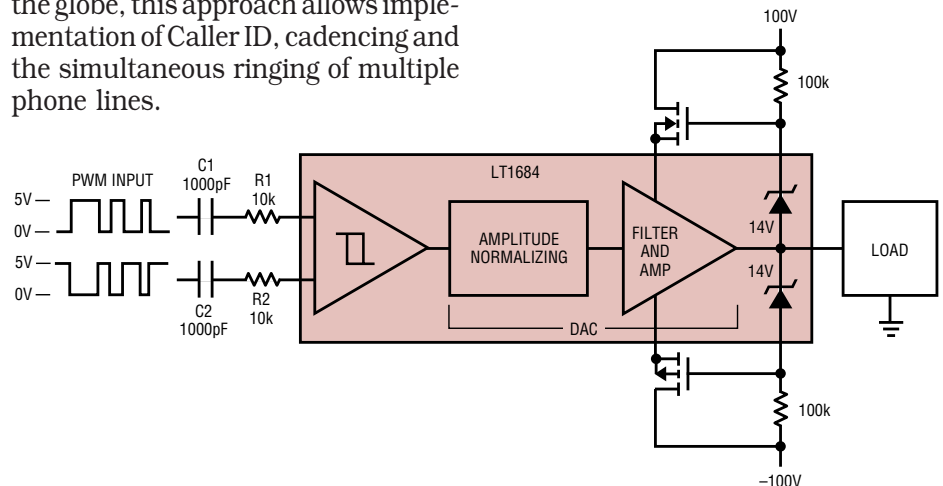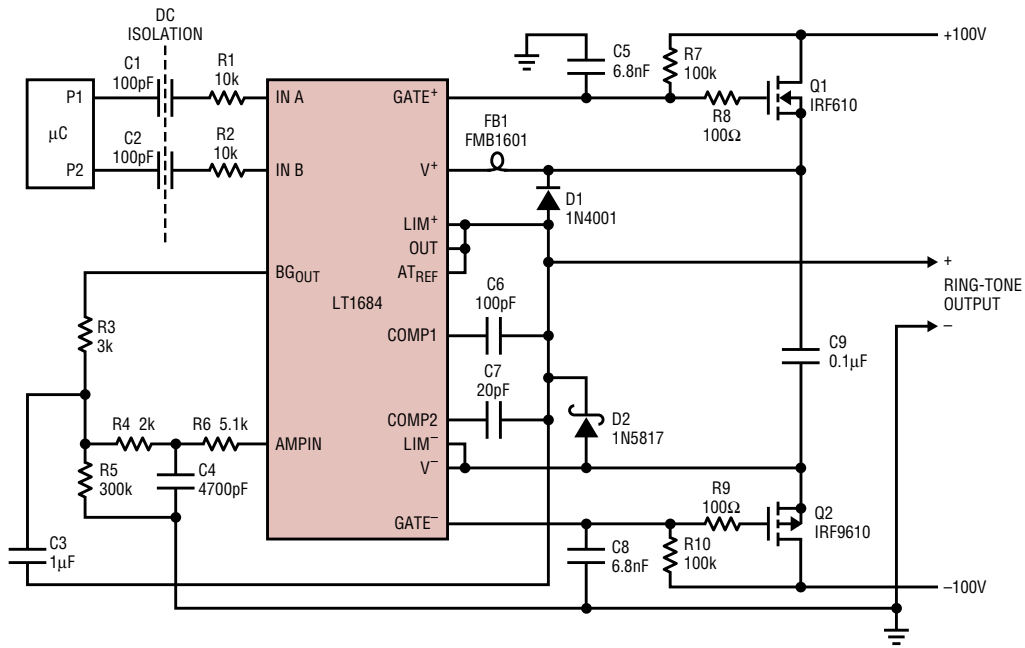

Figure 4. Ring signal from Figure 3's circuit

This circuit has the output current limit set at ±200mA, more than enough to ring ten phones. For current limits less than 200mA, two current limit resistors can be added in the Lim+ and Lim– leads, allowing the current limit to be set anywhere from 20mA to 200mA.

If additional output current is required, the LT1684 can be paired up with the LT1166 automatic bias control to provide any amount of current that is required.

Conclusion

By enabling direct software control of frequency, amplitude and cadence, the LT1684 allows a single design to be used in phone systems globally. *LT*

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output voltage above the reference, rendering them unusable in some applications.

Conclusion

The LT1761 provides excellent performance in a small package. With a maximum of 100mA output current at a dropout of 300mV, it operates

with only 20µA of quiescent current. This current drops to less than 0.1µA in shutdown, perfect for battery powered applications that need to be miserly with every joule. It is stable with a wide range of output capacitors, including small ceramics. With the addition of a small bypass capaci-

tor from the output to the reference, output voltage noise can be reduced to as low as $20\mu V_{RMS}$. Adding a bypass capacitor also realizes a benefit in improved transient response. Competing devices can't come close to the advantages that the LT1761 offers in the world of SOT-23 regulators. *LT*

LT1785 and LT1791: 60V, Fault-Tolerant RS485/RS422 Transceivers

by Gary Maulding

Introduction

The LT1785 and LT1791 RS485/RS422 transceivers with ±60V fault tolerance solve a real-world problem of field failures in RS485 interface circuits. RS485 and RS422 data networks are used in a wide variety of data-communications applications. Modems and other computer peripherals use point-to-point RS422 connections to support higher communications speeds with better noise immunity over greater distances than is possible with RS232 connections. Multipoint RS485 networks are used for LANs and industrial-control networks. These applications are vulnerable to the unknown, sometimes hostile environment outside of the controlled, shielded environment of a typical electrical-equipment chassis. Data line voltages exceeding the absolute maximum ratings of the transceiver chips can cause field failures of conventional transceiver circuits. Installation wiring faults, ground voltage faults and lightning-induced surge voltages are all common causes of overvoltage conditions that can damage conventional interface circuits. The rate of field failures in RS485 transceiver chips in some high-risk environments is so high that the transceiver chips are often DIP packages mounted in sockets to allow easy field servicing of equipment. The high voltage fault tolerance of the LT1785 and LT1791 provides a highly reliable solution for data networking in high-risk environments.

In addition to enhancing network-system fault tolerance, the electrical performance of the LT1785 and LT1791 matches or exceeds the best performing standard RS485/RS422 transceivers available, at data rates of up to 250kbaud. The LT1785 and LT1791 transceivers feature high input impedance for extended data networks, slew controlled outputs for EMI control, low impedance cable-drive capability, fail-safe receiver design and on-chip ±15kV ESD protection. With industry standard pinouts, systems can be easily upgraded for improved environmental fault tolerance.

Inherently Safe Up to ±60V

The electrical standards for RS422 and RS485 requires receivers and unpowered transmitters to operate with input common mode voltages from –7V to 12V, even though transmit voltages are limited to a voltage range between ground and 6V. This extra common mode range allows some tolerance for the real-world problem of ground voltage differences across a network. Unfortunately for most transceivers, voltages far in excess of the –7V to 12V range may occur in an actual network.

The RS485 and RS422 transceivers commonly available from several vendors are all vulnerable to damage from fault voltages only slightly outside the –7V to 12V operating envelope. One vendor's RS485 transceivers have absolute maximum voltage ratings of –8V to 12.5V on the data I/O pins. Such narrow margins above the required –7V to 12V operating conditions makes such circuits very fragile in a real-world environment. In addition, external protection circuitry is ineffective at protecting these circuits without interfering with normal operating signal levels.

The LT1785 and LT1791, with ±60V ratings on the driver output and receiver input pins, are inherently safe in environments that will destroy other interface circuits. Whether the circuit is transmitting, receiving, in standby or powered off, any voltage within ±60V will be tolerated by the chip without damage. Data communication will be interrupted during the fault condition, but the circuit will live to talk another day. The I-V curves shown in Figures 1–3 illustrate this.

The LT1785 and LT1791 receiver inputs maintain high impedance, typically 120kΩ, from –60V to 60V (see Figure 1). This benign characteristic is present under all operating conditions. Data signals are properly

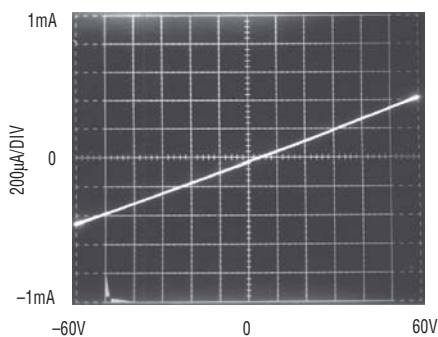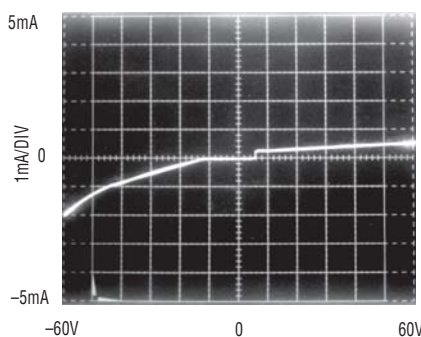Figure 1. I–V curve of LT1791 receiver input: –60V to 60V

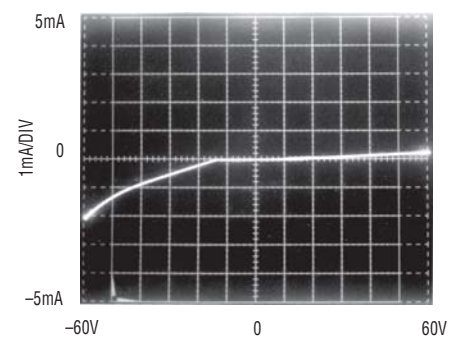Figure 2. I–V curve of LT1791 driver output: V_{CC} = 5V, DE = 0V, –60V < V_{OUT} < 60V

Figure 3. I–V curve of LT1791 driver output: V_{CC} = 0V, DE = 0V, –60V < V_{OUT} < 60V
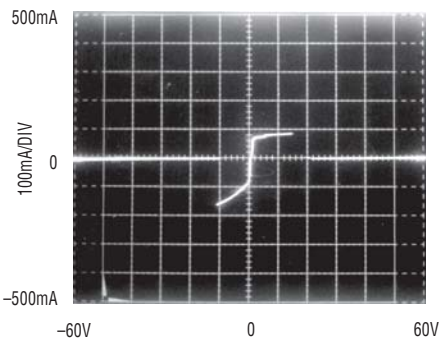
Figure 4. Driver fault current for output low (DE = V_{CC} = 5V)

received only in the –7V to 12V common mode range of RS485, but no damage to the LT1785/LT1791 will result over the entire ±60V range.

The driver behavior of the LT1785/ LT1791 is more involved than the receiver inputs and must be discussed separately for each operating mode. Figure 2 shows the I-V characteristic of the LT1791 driver outputs with the drivers in high impedance mode. Below –12V, some leakage current flows, but this only reaches a 2mA magnitude at –60V. With $V_{OUT} > V_{CC}$ (5V in this case), a small (100µA) current is conducted, which stays virtually constant as V_{OUT} increases up to 60V. With V_{CC} = 0V, the driver I-V curve is the same for negative voltages, but the 100µA current with positive voltages is not present (Figure 3).

Fault conditions while the circuit is transmitting cause the driver to enter current limit. For large magnitude faults, the current limit folds back to near zero. If short-circuit fault conditions are sustained, a thermal shutdown circuit will turn the drivers off. Figures 4 and 5 show the driver I-V curves for the outputs in low and high states.

Extending Beyond ±60V

Although ±60V fault tolerance forgives a great number of sins, higher voltage demons may still be lurking. ESD is one such demon, with voltage spikes of thousands of volts. The LT1785 and LT1791 have on-chip ESD protection to prevent damage from ESD transients of up to ±15kV. The ESD protection devices shunt the ESD energy away from active circuitry to the ground and V_{CC} supply pins. For the ESD protection to function properly, the user must ensure that low ESR supply-decoupling capacitors are located close to the V_{CC} and ground pins of the circuit. 0.1µF ceramic chip capacitors work well.

Other high voltage faults, such as lightning induced surge voltages, industrial environment ground loops or shorts to the AC line, are not as limited in energy as ESD transients. For such high energy faults, external protection must be used to protect the circuits. Typical protection networks use voltage clamping combined with current limiting networks. In concept, such networks could be used with most RS485 circuits to afford extended protection, but in practice, the addition of protection networks interferes with normal operation of the data network. Voltage clamping Zeners or TransZorbs® are not available in tight voltage tolerances and in addition, their internal impedances create several volts of additional potential above their nominal breakdown voltage to appear at the protected device's pins when fault currents flow. To protect a circuit with a –8V to 12.5V absolute maximum voltage rating would require the

TransZorb is a registered trademark of General Instruments, Inc. PolySwitch is a trademark of Raychem Corp.
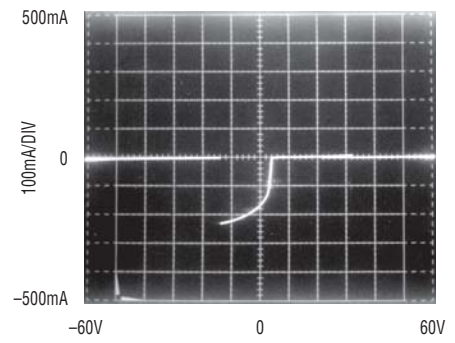
Figure 5. Driver fault current for output high (DE = V_{CC} = 5V)

use of protection devices with voltage ratings much below the required common mode range of RS485 networks. The triggering of the protection diodes would interrupt normal data transmission. The huge margin between operating voltages and the ±60V absolute maximum limits makes external protection a viable option with the LT1785 and LT1791.

Figure 6 shows an example of the use of external clamping and limiting components to extend the LT1785's ±60V inherent tolerance to much higher ±170V levels, the peak 120VAC line voltage in this example. 36V TransZorbs are used to clamp the transceiver line pins below the 60V rating of the transceiver. During a short to the 120VAC line, peak surge currents of nearly 3A will flow through the 47Ω resistors and the PolySwitch™ limiters. The peak current rating and series resistance of the TransZorbs must be considered during selection to ensure that the clamp limiter can withstand the surge and that the peak voltage will remain below the ±60V rating of the LT1785. At 3A, even high current TransZorbs will exceed their nominal breakdown voltage by several volts, making this protection method ineffective with transceiver circuits with only 1V to 4V absolute maximum margin above their operating ranges. The PolySwitch limiters are thermally activated and increase in resistance by many orders of magnitude in about 10ms. After the PolySwitch transition, fault currents are only a few milliamperes. Carbon composite resistors must be used for limiting the initial surge cur-
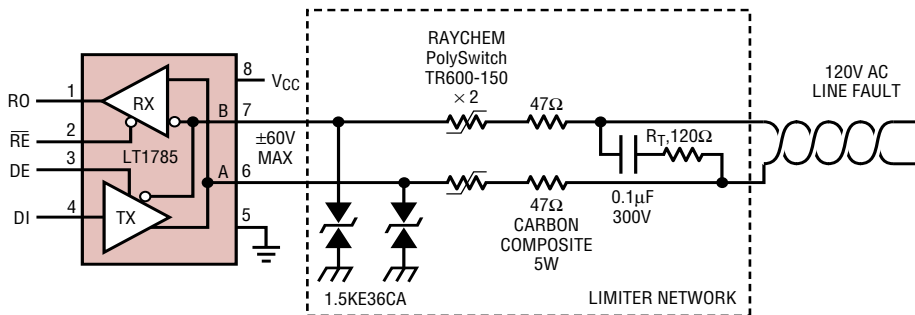
Figure 6. Fault tolerance extended to 120VAC line voltage

rent before the PolySwitch transition point. Metal film resistors do not have effective surge overload ratings and will fail before the PolySwitch transition drops the currents to sustainable levels.

Electrical Features Enhance Large Network Data Integrity

In addition to their unique fault tolerance capabilities, these transceivers provide electrical performance features that maximize the integrity of data transmission over long-line, distributed networks. Controlled-slew-rate outputs minimize EMI and cable reflection problems. Limited slew rates restrict data rates up to a maximum of 250kbaud (Figure 7), but this is not a limitation in most networks. RS485 standards allow data rates faster than 250kbaud only on small networks, less than 1000 feet in length. Controlled slew rates reduce cable reflections caused by connection stubs, imperfect terminations and cable splices, improving data transmission integrity on most networks.

LT1785 and LT1791 driver outputs have extra drive capability compared to most competing transceivers. Output levels are guaranteed when driving low impedance loads—as low as 36Ω. The extra current drive

allows inexpensive telephone cable, with characteristic impedance as low as 72Ω, to be used for the networking cable. This can result in significant cost savings in large networks and allows the use of existing wiring in many buildings.

A-grade devices are available that ensure fail-safe receiver outputs when the inputs are opened or shorted or no signal is present. The receiver thresholds on the LT1785A and LT1791A are guaranteed to be between 0.01V and 0.200V. This is tighter than the RS485/RS422-standard –0.200V to 0.200V thresholds. The guaranteed positive voltage thresholds eliminate ambiguous received signals during system fault or standby conditions. Open cables, shorted cables or all drivers in high impedance mode result in a zero volt differential at the receiver. The fail-safe receiver feature simplifies the design of software to detect these conditions. Any receiver-output low condition will be reliably interpreted as valid data.

The LT1785 and LT1791 feature extra high receiver input impedance, 85kΩ minimum, to minimize data-line loading and allow up to 128 connections on a data network. Standard RS232 networks are limited to
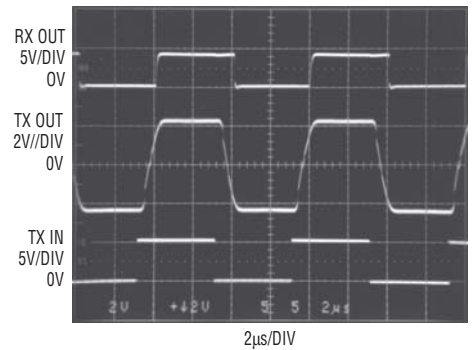
Figure 7. Normal operational waveforms at 250kbaud

32 receivers, where each receiver is considered to be one "unit load." Each LT1785 or LT1791 may be counted as 1/4 unit load and mixed with other 1-unit-load transceivers in a network. Maximum network size is reached at a total of 32 unit loads.

These electrical features, combined with rugged overvoltage tolerance, make the LT1785 and LT1791 excellent choices for extended data networks in less-than-benign electrical environments (Figure 8). Any data network operating in industrial environments, subject to installation errors or any other wiring faults, will benefit from using these transceivers for trouble-free, reliable data networking.
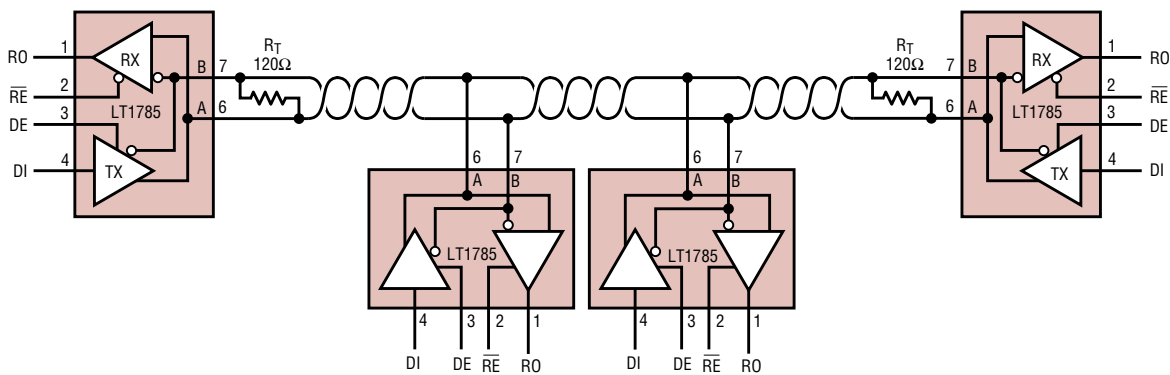
Figure 8. Half-duplex RS485 network operation

For more information on parts featured in this issue, see
http://www.linear-tech.com/go/ltmag

A Third Generation Dual, Opposing-Phase Switching Regulator Controller

by Steve Hobrecht

Introduction

The LTC1628 is the newest member of Linear Technology's third generation of DC/DC controllers. (The latest single-output members include the LTC1735, LTC1735-1 and the 5-bit VID controlled LTC1736.) These controllers use a similar constant frequency, current mode architecture and Burst Mode operation as the previous generation LTC1435–LTC1439 controllers but with improved features. A key new feature is control circuitry that drives the two top switches 180 degrees out of phase to minimize the input capacitance requirement *and* reduce conducted and radiated EMI. The resultant input ripple is effectively half the amplitude and double the frequency of nonphased controllers, significantly reducing the input capacitance requirement. OPTI-LOOP™ compensation, 5V and 3.3V standby regulators, new protection circuitry, tighter load regulation and strong MOSFET drivers make these controllers ideal for current and future generations of CPU and/or system power applications.

New Features of LTC's Third Generation of DC/DC Controllers

❏ Dual controllers have opposing-phase top MOSFET turn-on timing.
❏ OPTI-LOOP compensation and Burst Mode operation reduce the output capacitance requirement while optimizing transient response and minimizing peak-to-peak output voltage ripple at all output current levels.
❏ A 0.8V, 1% reference allows lower output voltage operation (down to 0.8V).
❏ 0.2% load and line regulation
❏ The maximum current sense voltage has been reduced from 150mV to 75mV. This reduces

the power lost in the sense resistor by a factor of two.
❏ The gate drivers are three to four times the strength of those in the previous generation of products, the LTC1435–39. This equates to faster rise and fall times when driving the same MOSFETs plus the capability to drive larger MOSFETs with less transition loss and higher efficiency.
❏ Overvoltage "soft latch"
❏ Undervoltage lockout at 3.5V
❏ Foldback current limiting and defeatable overcurrent latch-off
❏ The current comparators' common mode range includes ground. This allows operation of the switching regulator controller in a grounded sense resistor application while retaining full operation of all controller features.
❏ Three operating modes (the third item is new)
—Forced PWM: inefficient but can be low noise
—Burst Mode: very efficient but can generate noise, depending upon the load
—Burst disable: reasonably efficient and low noise due to constant frequency operation down to approximately 1% of maximum designed load current.
❏ Minimum on-time < 200ns allows high V_{IN} to V_{OUT} ratios and high frequency operation without skipping cycles.
❏ Logical-control of fault coupling on the LTC1628 between the two controllers
—Both controllers can be forced into continuous mode
—A normally operating controller can be shut down when a short-circuit fault is sensed on the other controller (both are shut down and latched off).

❏ A standby mode on the LTC1628 provides two functions:
—A common pin to pull down both RUN/SS pins for reset
—A control pin that, when pulled high, turns on both the 5V and 3.3V standby regulators even when neither controller is turned on.

2-Phase Operation

The LTC1628 dual, high efficiency DC/DC controller brings the considerable benefits of 2-phase operation to portable applications for the first time. Notebook computers, PDAs, handheld terminals and automotive electronics will all benefit from the lower input filtering requirement, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

Why the need for 2-phase operation? Up until the LTC1628, constant frequency dual switching regulators operated both channels in phase (1-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two channels of the dual switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses coming from the switches, greatly reducing the overlap time where they add together. The result is a significant reduction in total RMS input current, which, in turn, allows less expensive input capacitors to be used, reduces
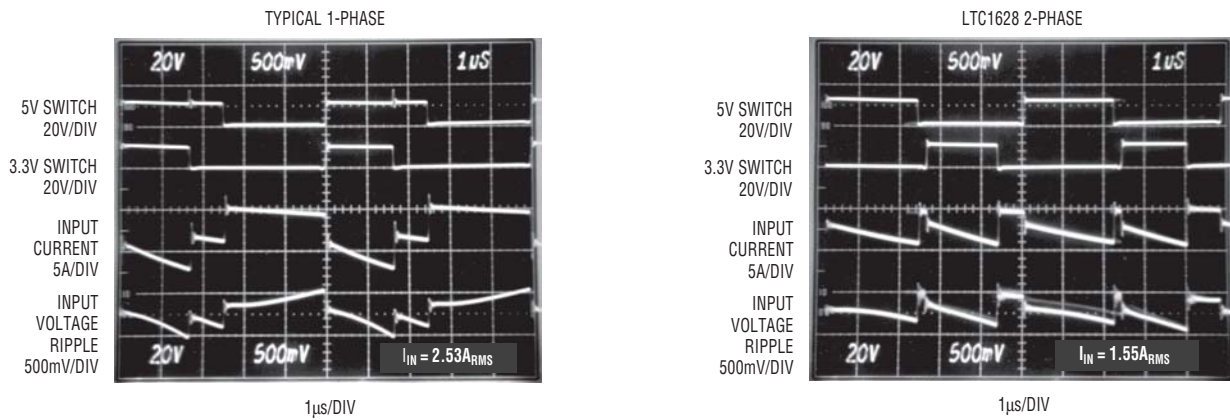
TYPICAL 1-PHASE

LTC1628 2-PHASE

Figure 1. Input waveforms, comparing 1-phase and 2-phase operation for dual switching regulators converting 12V to 5V and 3.3V at 3A each: the reduced input ripple with the LTC1628 2-phase regulator allows the use of less expensive input capacitors, reduces shielding requirements for EMI and improves efficiency.

shielding requirements for EMI and improves overall operating efficiency.

Figure 1 compares the input waveforms for a representative 1-phase dual switching regulator to the LTC1628 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase operation decreases the input current from $2.53A_{RMS}$ to $1.55A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I^2_{RMS}, meaning that the actual power wasted is reduced by a factor of 2.66. The reduced input ripple voltage also means less power lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.
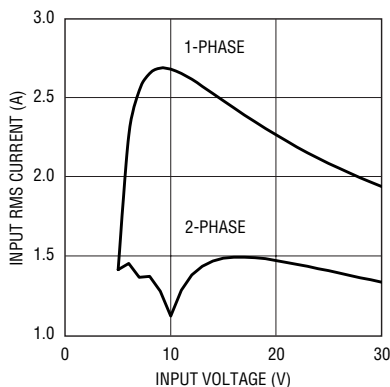

Figure 2. RMS input current vs input voltage; V_{O1} = 5V/3A; V_{O2} = 3.3V/3A

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles, which in turn are dependent upon the input voltage, V_{IN} (duty cycle = V_{OUT}/V_{IN}). Figure 2 shows how the RMS input current varies for 1-phase and 2-phase operation for 3.3V and 5V regulators, each with a 3A constant load, over a wide input voltage range. It can be readily seen that the advantages of 2-phase operation are not limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb is that, in most applications, 2-phase operation will require the same input capacitance as one channel of a single-phase circuit operating at maximum current and 50% duty cycle.

Now, a final question: if 2-phase operation offers such an advantage over 1-phase operation for dual switching regulators, why hasn't it been done before? The answer is that, while simple in concept, it is hard to implement. Constant frequency, current-mode switching regulators require an oscillator-derived slope compensation signal to allow stable operation of each regulator at over 50% duty cycle. This signal is relatively easy to derive in 1-phase dual switching regulators, but required the development of a new proprietary technique to allow 2-phase operation. In addition, isolation between the two channels becomes more critical with 2-phase operation because switch transitions in one channel could po-

tentially disrupt the operation of the other channel.

The LTC1628 is proof that these hurdles have been surmounted. The new device offers unique advantages for the ever-expanding number of high efficiency power supplies required in portable electronics.

Additional Features

The LTC1628 contains two synchronous step-down switching regulator controllers to drive external N-channel power MOSFETs using a programmable, fixed frequency OPTI-LOOP architecture. OPTI-LOOP compensation effectively removes the constraints placed on C_{OUT} by other controllers for proper operation. A maximum duty cycle limit of 99% provides low dropout operation, which extends operating time in battery-operated systems. A forced-continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling Burst Mode when the main output is lightly loaded. Soft-start is provided for each controller by an external capacitor that can be used to properly sequence supplies. The operating output current levels are set by external current sense resistors. A wide input-supply range allows operation from 3.5V to 30V (36V maximum).

Protection

New internal protection features in the LTC1628 controllers (also included in the single-output ver-

sions) include foldback current limiting, short-circuit detection, optional short-circuit latch-off and overvoltage protection. These features protect the PC board, the MOSFETs and the load itself against faults.

Fault Protection: Overcurrent Latch-Off

The RUN/SS pins, in addition to providing soft-start capability, also provide the ability to shut off the controller and latch off when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS} (refer to Figure 5), is used initially to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge the output capacitor and provide full load current, C_{SS} is used as a short-circuit timer. If the output voltage falls to less than 70% of its nominal output voltage after C_{SS} reaches 4.2V, it is assumed that the output is in a severe overcurrent and/or short-circuit condition and C_{SS} begins discharging. If the condition lasts for a long enough period, as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled.

This built-in latch-off can be overridden by providing >5µA at a compliance of 4V to the RUN/SS pin (refer to the LTC1628 data sheet for details). This external current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition.

Why should you defeat overcurrent latch-off? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will allow easy troubleshooting of the circuit and PC board layout. The internal short-circuit detection and foldback current limiting still remain active, thereby protecting the power supply system from failure. After the design is complete, you can decide whether to enable the latch-off feature.

A logic input pin, FLTCPL, can direct the internal control circuitry to

Table 1. Overvoltage protection comparison		
Operating Condition	Soft Latch	Hard Latch
Fast Transients	Controls Overshoot	Latches Off
Output Shorted to 5V	Output Clamped at OVP	Latches Off
VID Voltage Decrease	Regulates New Voltage	Latches Off
Noise	Controls Output	Latches Off
Shorted Top MOSFET	Bottom MOSFET Overloads	Bottom MOSFET Overloads
Output Voltage Can Reverse	No	Yes
When Overload is Removed	Resumes Normal Operation	Remains Latched Off
Troubleshooting Faults	Easy DC Measurements	Difficult; May Require Digital Oscilloscopes

shut down a normally operating controller when a fault results in the shutdown of either controller. In addition, this pin can direct both channels to operate in a forced continuous (PWM) mode when the FCB pin falls below a 0.8V threshold.

Fault Protection: Current Limit and Current Foldback

The LTC1628 current comparators have a maximum sense voltage of 75mV, resulting in a maximum inductor current of 75mV/R_{SENSE}. The LTC1628 includes current foldback to help further limit load current when the output is shorted to ground. If the nominal output voltage falls by more than 30%, the maximum sense voltage is progressively lowered from 75mV to 30mV. Under short-circuit conditions with very low duty cycle, the LTC1628 will begin cycle skipping in order to limit the short-circuit current. In this situation, the bottom MOSFET will be on most of the time, conducting the current. The average short-circuit current will be approximately 30mV/R_{SENSE}. Note that this function is always active and is independent of the short circuit latch-off.

Fault Protection: Output Overvoltage Protection (OVP)

An output overvoltage crowbar turns on the synchronous MOSFET to either force a protected-wall-adapter power source into a current/power limiting mode or blow a system fuse in the input lead when the output of the regulator rises much higher than

nominal levels. The crowbar can cause huge currents to flow, greater than in normal operation. This feature is designed to protect the load against a shorted top MOSFET or shorts to higher supply rails.

Previous latching crowbar schemes for overvoltage protection have a number of problems (see Table 1). One of the most obvious, not to mention most annoying, is nuisance trips caused by noise or transients momentarily exceeding the OVP threshold. Each time this occurs with latching OVP, a manual reset is required to restart the regulator. Far more subtle is the resulting output voltage reversal. When the synchronous MOSFET latches on, a large reverse current is loaded into the inductor while the output capacitor is discharging. When the output voltage reaches zero, it does not stop there, but rather continues to go negative until the reverse inductor current is depleted. This requires a sizable Schottky diode across the output to prevent excessive negative voltage on the output capacitor and load.

A further problem on the horizon for latching OVP circuits is their incompatibility with on-the-fly CPU core voltage changes. If an output voltage is reprogrammed from a higher voltage to a lower voltage, the OVP will temporarily indicate a fault, since the output capacitor will momentarily hold the previous, higher output voltage. With latching OVP, the result will be another latch-off, with a manual reset required to attain the new out-

Table 2. FCB possible states

FCB Pin	Condition
DC Voltage: 0V–0.7V	Burst Disabled/ Forced Continuous, Current Reversal Enabled
3.5V >DC Voltage > 0.9V	Burst Mode, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
DC Voltage = 5V	Burst Mode Disabled, No Current Reversal

put voltage. To prevent this problem, the OVP threshold must be set above the maximum programmable output voltage, which would do little good when the output voltage was programmed near the bottom of its range.

In order to avoid these problems with traditional latching OVP circuits, the LTC1628 uses a new "soft-latch" OVP circuit. Regardless of operating mode, the synchronous MOSFET is forced on whenever the output voltage exceeds the regulation point by more than 7.5%. However, if the voltage then returns to a safe level, normal operation is allowed to resume, thereby preventing latch-off caused by noise or voltage reprogramming. Only if a true fault, such as a shorted top MOSFET, exists will the synchronous MOSFET remain latched on until the input voltage collapses or the system fuse blows.

The new soft-latch OVP also provides protection and easy diagnosis of other overvoltage faults, such as a lower supply rail shorted to a higher
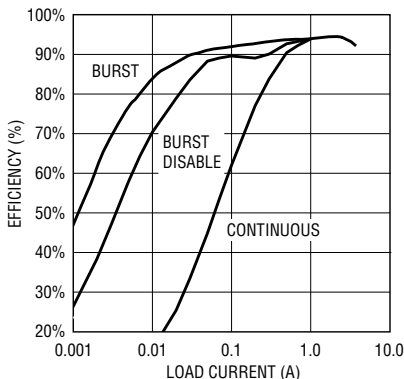

Figure 3. Efficiency vs load current for three modes of operation (V_{IN} = 15V, V_{OUT} = 5V)

voltage. In this scenario, the output voltage of the higher regulator is pulled down to the OVP voltage of the soft-latched regulator, allowing the problem to be easily diagnosed with DC measurements. On the other hand, latching OVP provides only a transient glimpse of the fault as it latches off, forcing the use of expensive digital oscilloscopes for troubleshooting.

Three Operating Modes/ One Pin: Forced PWM, Burst and Burst Disable

The FCB pin is a multifunction pin that controls the operating mode of the LTC1628. When the FCB pin drops below a 0.8V threshold (or is grounded), continuous mode operation is forced on the first controller if V_{FLTCPL} = 0V or on both controllers if V_{FLTCPL} = 5V. In continuous mode, the top and bottom MOSFETs continue to be driven synchronously regardless of the load on the output. The inductor current is allowed to go negative at low load currents in order to maintain a secondary output voltage. The voltage derived from a secondary winding can be resistively divided down and fed into the FCB pin to force continuous operation momentarily or continuously as required to regulate the secondary output voltage. This allows a secondary output voltage to be regulated, regardless of the load on the primary output.

When the FCB pin is left open, Burst Mode operation is enabled. Burst Mode operation allows intermittent on/off PWM operation of the output MOSFETs, as required to keep the output in regulation. This maximizes efficiency at the expense of a slight increase in output voltage ripple (20mV–30mV).

The burst disable mode is selected by tying the FCB pin to the INTV$_{CC}$ pin. The burst disable mode uses a constant frequency, discontinuous inductor current method. This mode is not as efficient as Burst Mode, but allows low noise, constant frequency operation down to approximately 1% of the maximum designed load cur-

rent and does not allow the inductor current to reverse. At very low currents, cycles are skipped to maintain proper output voltage.

Table 2 summarizes the possible states available on the FCB pin.

Figure 3 gives a comparison of efficiencies in a regulator for the three operating modes: forced continuous operation, burst disable (pulse-skipping) mode and Burst Mode operation.

Speed

The LTC1628 is designed to be used in higher current applications than the LTC1435–39 family. Stronger gate drive allows paralleling multiple MOSFETs or higher operating frequencies. The LTC1628 has been optimized for low output voltage operation by reducing the minimum on-time to less than 200ns. Remember, though, that transition losses can still impose significant efficiency penalties at high input voltages and high frequencies. The LTC1628 can operate at 300kHz but that doesn't mean it should be used there in every application. Figure 4 shows a plot of MOSFET charge current versus frequency.

Linear Current Comparator Operation

Since the trend in the marketplace has forced output voltages to lower and lower values, the current sense inputs have been optimized for low voltage operation. The current sense comparator has a linear response characteristic, without discontinuities, for output voltages from 0V to 6V. In the LTC1435–LTC1439, two input stages are used to cover this
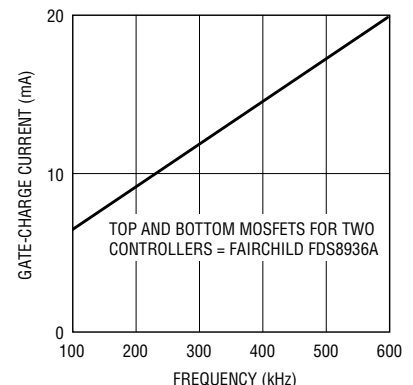

Figure 4. Gate-charge current vs frequency (V_{IN} = 15V, V_{GATE} = 5V$_{P-P}$)
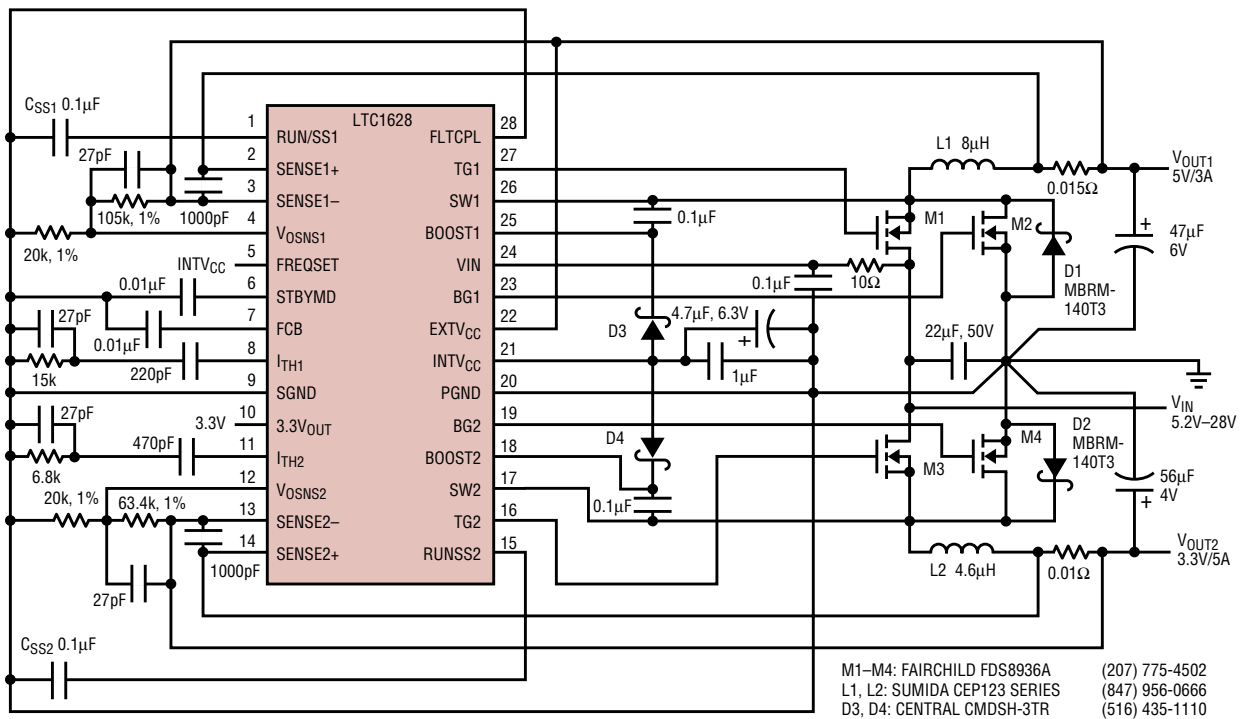
Figure 5. High efficiency 5V/3A, 3.3V/5A, small-footprint system power design

range, so an overlap (with a transition region) exists. All third-generation products, including the LTC1628 uses only one input stage and includes slope compensation that operates over the full output voltage range. This allows the third generation controllers to be operated in grounded R_{SENSE} applications.

Remote Output Voltage Sensing

The LTC1628 also has remote sense capability. A resistive divider is connected between the output load and SGND. The SGND pin can be tied to the load return, allowing a Kelvin connection for remotely sensing the output voltage directly across the load, eliminating any PC board–trace resistance errors.

Applications

Figure 5 shows a 5V/3A, 3.3V/5A application using the LTC1628. The input voltage can range from 5V to 28V. Table 3 compares the third-generation LTC1628 with LTC's second generation LTC1438/ LTC1439 dual controllers.

Conclusion

The LTC1628 is the latest member of Linear Technology's third generation family of constant frequency, N-channel, high efficiency controllers. With opposing phase, new protection features, OPTI-LOOP compensation and strong MOSFET drivers, the LTC1628 is an ideal choice for many system power applications. The third generation controllers have been designed specifically to minimize both the overall power system cost and the physical size and number of the external components in order to meet the size/ performance requirements of new products. The high performance of these controllers, with their wide input voltage range, 1% output voltage accuracy and tight line and load regulation, makes them ideal for next generation designs. *LT*

Table 3. Comparison of LTC1628 controller with LTC1438/LTC1439 controllers

Parameter	LTC1628	LTC1438/LTC1439
Reference	0.8V, 1%	1.19V, 1%
Load Regulation	0.05% Typ, 0.3% Max	0.5% Typ, 0.8% Max
Max Current Sense	75mV	150mV
Minimum On-Time	200ns	400ns
Opposing Phase	Yes	No
Standby Voltages	5V, 3.3V	5V
Undervoltage Lockout	3.5V	No
Current Foldback	Internal	External
Overvoltage Protection	Yes	No
Overcurrent Latch-Off	Optional	No
Fault Coupling	Overcurrent Latch-Off	No
MOSFET Drivers	3×	1×

LTC1569-X, 10th Order, Linear-Phase Lowpass Filter Family is Tunable with a Single External Resistor

by Michael Kultgen

The new LTC1569-6/LTC1569-7 are the first monolithic filters in the industry to provide accurate control of the cutoff frequency without the need for an external clock. A single external resistor programs internal precision circuitry, enabling the user to vary the filter cutoff frequency over eight octaves with a typical accuracy of ±3% or better. Figure 1 shows a simplified block diagram of the LTC1569-6/ LTC1569-7.

The internal filter circuitry uses sampled-data techniques with a ratio of sampling frequency to filter cutoff frequency of 64:1 and 128:1 for the LTC1569-7 and LTC1569-6, respectively. This technology allows the realization of complex and accurate filter functions in a relatively small space.

Ease of tuning is just one of the many features of this linear-phase, DC-accurate, 10th order lowpass filter. Other features include:

❏ Up to 300kHz cutoff frequency operating on a single 5V supply or 150kHz cutoff frequency operating on a single 3V supply (LTC1569-7)
❏ Root raised cosine response (alpha = 0.5) with linear phase and steep selectivity
❏ DC accurate with a maximum offset of 5mV when powered with a 3V supply
❏ Differential or single-ended inputs
❏ Power consumption as low as 8mW (LTC1569-6, f_C = 4kHz)
❏ Small SO-8 package Operates from 3V to ±5V Supplies

An Outstanding Response

The frequency response of the LTC1569-6/LTC1569-7 is a 10th order approximation of the classical "root raised cosine" function with phase linearization. The result is an outstanding lowpass characteristic, ideal for data communications or data acquisition systems. This combination of precision and selectivity is *practically impossible to achieve with discrete filters.*

The filter attenuation is 50dB at 1.5 times the filter cutoff (f_C), 60dB at twice f_C and in excess of 80dB at six times f_C. Thus, the LTC1569-6/ LTC1569-7 are excellent choices in applications with demanding specifications for rejection of frequency components outside the passband (Figure 2). Examples include a wireless communication system using a lowpass filter to limit the amount of energy transmitted outside of the desired channel or a sensor system that measures a low frequency signal in the presence of significant interference.

In data communications, designs are optimized to transmit the maximum amount of information in the allotted bandwidth. In systems using pulse amplitude modulation, pulse shaping is an important design consideration. The linear-phase, root raised cosine response (alpha = 0.5) of the LTC1569-6/LTC1569-7 lets users build matched filters with low intersymbol interference and a high tolerance of timing jitter. Figure 3 shows the eye pattern when the data rate is equal to twice the cutoff frequency (512kbps).

Easy, Accurate Tuning

Many commercially available monolithic filters using sampled data (switched capacitor) techniques require an external clock to set the cutoff frequency. The ratio of the internal sampling rate to filter cutoff frequency is usually fixed; the desired cutoff frequency will dictate the exact frequency of the external clock. For instance, if the sampling-rate to the filter-cutoff frequency ratio is 100:1 and the input signal is sampled at both rising and falling edges of the internal clock (this is commonly called a double-sampled filter), a 3.4kHz cutoff frequency will dictate a 170kHz external or internal clock. If the system already possesses a crystal-based master clock of several MHz, the desired clock frequency for the filter can be derived by using appropriate dividers. Clock division by conventional binary or decade counters will then provide enough resolution to fit the application. The clock generation task described above may be cumbersome but it yields stable and accurate clock frequencies. Because switched capacitor filters feature quite accurate clock-to-cutoff frequency ratios, the overall filter frequency/ phase accuracy will be superior to a that of discrete filter realization with active and/or passive components. Applications requiring narrow band filtering or strict control of the filter phase at given frequencies could justify such a complex clock-generation
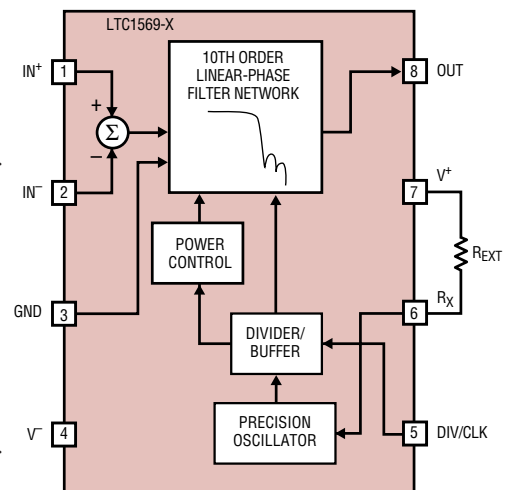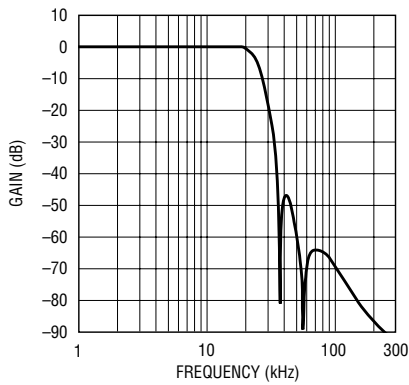

Figure 1. LTC1569-X block diagram

Figure 2. LTC1569-X frequency response characteristics

scheme, although many system designers strongly resist routing a "noisy" clock signal through an analog board.

Inexpensive and quite inaccurate clock generation (especially if the required clock frequency is below 1MHz) can also be realized with comparators or timers and discrete passive components. The clock frequency will show a tolerance of 5%–10%, especially if 5% discrete capacitors are used. This solution places the clock physically next to the sampled data filter, thus avoiding routing it throughout the PC board, but the wide tolerance of the clock can be objectionable.

Both clock generation methods above may fail if the required clock frequency is a few MHz and/or if the sampled data filter is intended to replace a discrete active filter design and there is no available clock in the system. In this case the clock generation becomes part of the filter design and the new clock/sampled-data-filter solution may be more complex than the existing discrete filter.

Clock Generation Made Easy

The LTC1569-6/LTC1569-7 solves the clock issues mentioned previously. An internal precision oscillator drives the sampled data filter. The frequency of the internal oscillator is set with an external resistor, which can have very low initial tolerance and can assume a large number of values. External capacitors or resistor-capacitor combinations are no longer required. The filter cutoff frequency is accurate to ±3% (for a given resistor value) for frequencies from 1kHz (LTC1569-6) to 256kHz (LTC1569-7); even higher cutoff frequencies are possible. Furthermore, the voltage across the external resistor is static, reducing EMI.

To set the cutoff frequency, place a resistor between pins 6 and 7 (Figure 4) and program the internal divider. The divider is programmed by tying pin 5 to pin 4 (divide by 1), floating pin 5 (divide by 4) or connecting pin 5 to pin 7 (divide by 16). These simple connections are illustrated in the application circuit of Figure 4, where the single-ended filter can have three different cutoff frequencies depending on the switch position: 8kHz, 32kHz or 128kHz.

By tying pin 6 to pin 4, the LTC1569-6/LTC1569-7 are placed in the external clock mode. The DIV/CLK pin becomes the input for an external clock signal and the LTC1569-6/LTC1569-7 can be tuned like traditional switched capacitor filters with a external-clock-frequency to filter-cutoff-frequency ratio of 64:1 (LTC1569-6) or 32:1 (LTC1569-7). Since the filter is double sampled, the effective oversampling ratio is 128:1
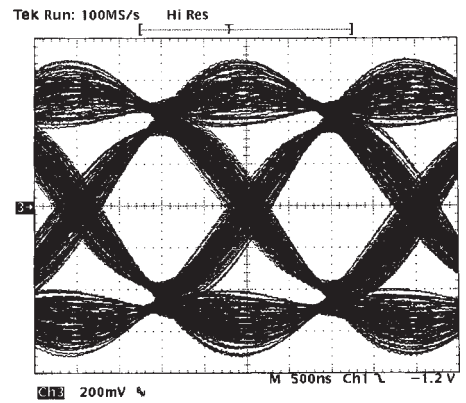

Figure 3. LTC1569-X eye diagram: data rate = 2× f_{CUTOFF} (512kbps)

(LTC1569-6) or 64:1 (LTC1569-7). External clocking is useful in applications where the cutoff frequency needs to be continuously variable or where the filter sampling needs to be synchronized to another element in the system, for example a second filter path or an A/D converter.

High Speed or Low Power

With cutoff frequencies as high as 300kHz (LTC1569-7, V_{SUPPLY} = 5V), the LTC1569-6/LTC1569-7 are the fastest switched capacitor filters on the market today, making them the ideal filtering solution for signal processing in the 200kHz to 300kHz range. Intelligent power management allows the IC to be configured for high speed or low power. For maximum cutoff frequencies, the 1569-7 typically requires 100mW when powered from a 5V supply. However, the power consumption can be reduced to as little as 8mW (LTC1569-6, V_{SUPPLY} = 3V, f_{CUTOFF} = 4kHz). In fact, there are several different power-speed combinations to choose from, allowing the user to tailor the filter to the requirements of the specific application.

Flexible Interface

Many applications require filtering a differential signal or translating the common mode voltage in a single-supply system. The flexibility of LTC1569-6/LTC1569-7's differential input solves these interfacing problems. For example, in Figure 5 the LTC1569-6/LTC1569-7 are used to pulse shape 256KB/s binary data in
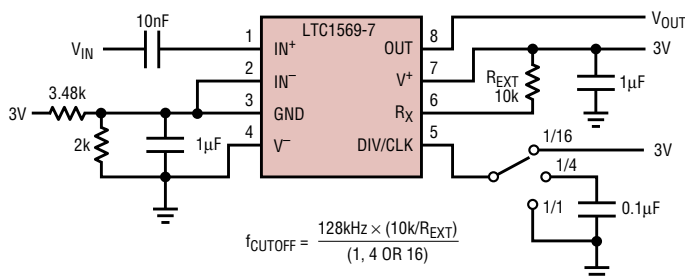
$$f_{CUTOFF} = \frac{128kHz \times (10k/R_{EXT})}{(1, 4 \text{ OR } 16)}$$

Figure 4. 3V AC-coupled, single-ended filter with multiple cutoff frequencies

Ultralow Power 14-Bit Serial ADC Samples at 400ksps

by Dave Thomas and
Kevin R. Hoskins

Introduction

The LTC1417 is a new and versatile 14-bit ADC that samples at up to 400ksps while consuming just 20mW from a single 5V supply. The LTC1417 is designed to be adaptable and easy to use, requiring little or no support circuitry in a wide variety of applications. Some of the key features of this new device include:

❏ 400ksps throughput
❏ 82dB SINAD and –95dB THD at Nyquist
❏ Low power—20mW
❏ Single 5V or ±5V supplies
❏ 1.25LSB INL max and 1LSB DNL max
❏ Differential inputs
❏ Serial data output
❏ NAP and SLEEP power shutdown modes
❏ Small package—16-pin SSOP

High Performance with Low Power

Figure 1 shows a block diagram of the LTC1417. This device includes a high performance differential sample-and-hold circuit, an ultra-efficient successive-approximation ADC, an on-chip reference and a serial digital interface that easily interfaces to microprocessors, FIFOs or DSPs. The LTC1417 is factory calibrated, so a lengthy calibration cycle is not required to achieve 14-bit performance. DC specifications include a 1LSB (max) differential linearity error (no missing codes) and ±1.25LSB max integral linearity error, both guaranteed over temperature. Typical INL and DNL curves are shown in Figures 2a and 2b. The gain of the ADC is controlled by an on-chip 10ppm/°C reference that can be easily overdriven with an external reference if required.

For AC applications, the dynamic performance of the LTC1417 is exceptional. The extremely low distortion differential sample-and-hold has a typical full-power bandwidth of 10MHz. The spurious free dynamic range is typically 95dB at the 200kHz Nyquist frequency. The part's low noise and low distortion achieve a signal-to-noise ratio (SNR) of 82dB from DC to well beyond Nyquist. Figure 3 shows the typical SINAD and ENOB versus input frequency. The FFT in Figure 4 shows the that the typical THD is composed of second and third harmonics; the higher harmonics are below the noise floor. Figure 5 shows the second and third harmonic distortion versus input frequency.
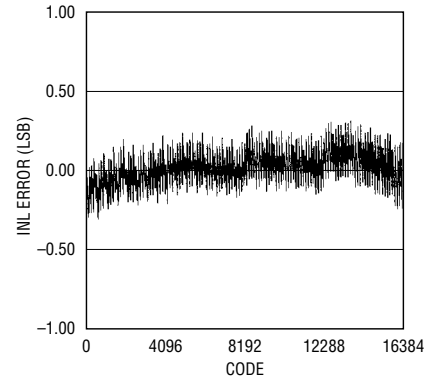

Figure 2a. The LTC1417's typical INL is less than ±0.5LSB.
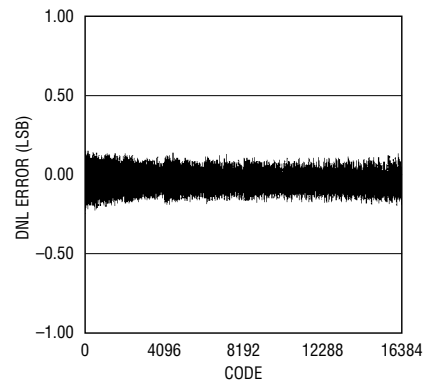

Figure 2b. With a typical DNL of less than ±0.35LSB, the LTC1417 is a true 14-bit-accurate part.
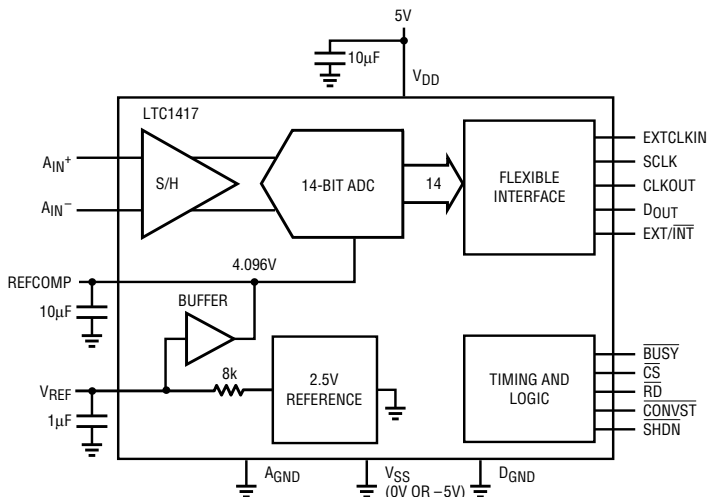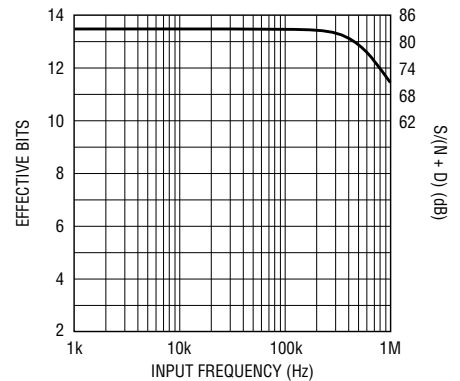

Figure 3. With a SINAD of 82dB, the LTC1417 maintains 13.4ENOB at the 200kHz Nyquist frequency.

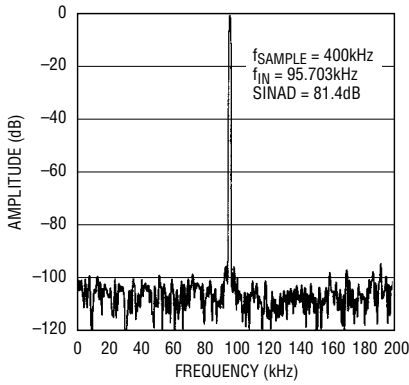

Figure 1. LTC1417 block diagram

Figure 4. The LTC1417's linearity, as shown in this FFT, helps preserve signal integrity while allowing only small amounts of second and third harmonic distortion. Any remaining distortion is below the part's noise floor.

The LTC1417's superior AC and DC performance doesn't require a lot of power. In fact, the LTC1417 is one of the lowest power 14-bit ADCs available, dissipating just 20mW at 400ksps (10mW at sample rates below 125ksps). Two shutdown modes make it possible to decrease power consumption even further as the sampling rate is reduced. This will be described in greater detail later in this article.

High Impedance Inputs

The LTC1417's high impedance inputs allow direct connection of high impedance sources without introducing errors. Many ADCs have a resistive input or input bias current that requires a low source impedance to achieve low errors. Often, ADCs with switched capacitor inputs exhibit large offset shifts when driven with a high source impedance or a large source-im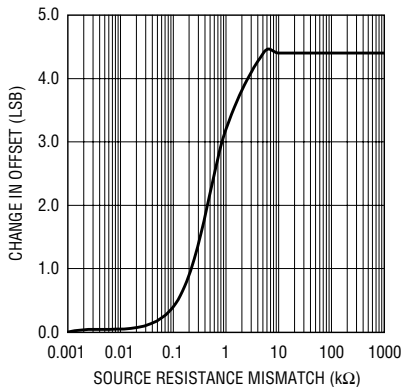pedance imbalance between their differential inputs. The LTC1417's unique sample-and-hold circuit has a low capacitance, high resistance ($10M\Omega \parallel 14pF$) switched capacitor input that has only 4.5LSB of offset shift with a source impedance imbalance between 0Ω and $1M\Omega$ (see Figure 6a). (There is no shift if $+A_{IN}$ and $-A_{IN}$ see equal source impedances.) Connecting the ADC directly to a high impedance source avoids the additional noise and offset errors that may be introduced by buffering circuitry. The only downside caused by directly connecting the ADC to a high source impedance is increased acquisition time. However, because of the LTC1417's low input capacitance (14pF), the ADC achieves full-speed operation while operating with source impedances up to $2k\Omega$. Above $3k\Omega$, the sample rate must be reduced, as shown in Figure 6b.

Differential Inputs with Wideband CMRR

Another benefit of the LTC1417's differential input is excellent common mode rejection, which eliminates the need for most input-conditioning circuitry. Op amps and instrumentation amplifiers are often used to reject common mode noise from EMI, AC power and switching noise. Although these circuits perform well at low frequencies, their rejection at high frequencies deteriorates substantially. Figure 7 shows how the LTC1417's CMRR remains strong as the frequency increases.

Figure 5. As the input signal's frequency increases, second and third harmonic distortion remain low.

Single- or Dual-Supply Operation

Single-supply ADCs can be cumbersome to use in a dual-supply system. A signal with a common mode of zero volts has to be shifted to the ADC's common mode voltage. Shifting the common mode can be accomplished with AC coupling, but DC information is lost. Alternatively, an op amp level shifter can be used, but this adds circuit complexity and additional errors. The LTC1417 overcomes these limitations because it operates with single or dual supplies, which allows input signals to be direct coupled in both cases. With a single supply, $V_{SS} = 0V$ and the ADC operates in unipolar mode with an input range of 0V to 4.096V. The ADC is equipped with circuitry that automatically detects when –5V is present on the V_{SS} pin. With a –5V supply, the ADC operates in bipolar mode and the full-scale range becomes ±2.048V for $+A_{IN}$ with respect to $-A_{IN}$.

Figure 6a. Change in offset voltage with source resistance mismatch

Figure 6b. Maximum sample rate vs unbuffered source resistance

Figure 7. Input common mode rejection vs input frequency

Figure 8. This simple 4-wire connection uses the LTC1417's internal clock to simultaneously clock the conversion and shift out the data.

On-Chip Reference

The LTC1417's on-chip reference is a standard 2.5V and is available on the V_{REF} output (pin 3). An internal amplifier increases the reference's 2.5V to 4.096V, setting the ADC's full-scale span. The 4.096V output is available on the REFCOMP output (pin 4) and may be used as a reference for other external circuitry. With a temperature coefficient of 10ppm/°C, both V_{REF} and REFCOMP are well suited to function as a system's master reference. However, if an external reference circuit is required, it can easily overdrive either reference output. The 2.5V reference output is resistive (8k) and can be easily overdriven by any r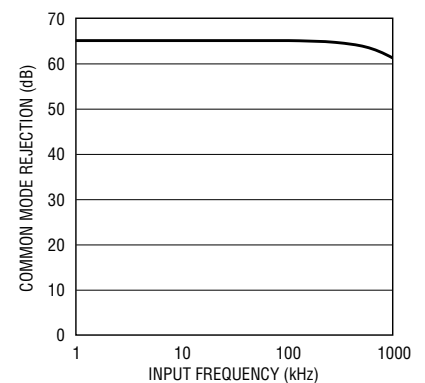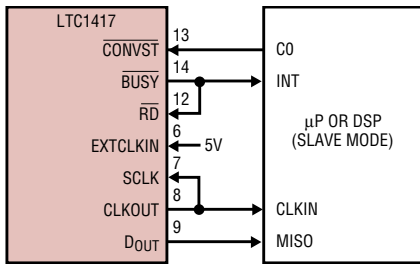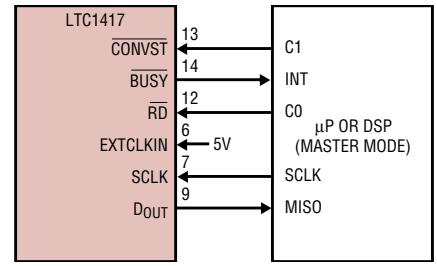eference with low output impedance by directly connecting the external reference to the REF pin. When overdriving the REFCOMP (the 4.096V reference) output, tie the V_{REF} pin to ground. This disables the output drive of the REFCOMP amplifier, allowing it to be easily overdriven.

Simple, Versatile Serial Interface

While simple, the LTC1417's four-mode serial interface does not sacrifice flexibility. Serial data can be clocked with the internal shift clock for minimal hardware or with an external shift clock for synchronization. Additionally, data can be clocked out during the conversion for the highest throughput rate or after the conversion for maximum noise immunity. Its simplest mode uses just three pins for data transfer: a data-out pin, a serial clock pin and a control pin. With more connections, the conversion and the output data can be clocked at different rates, optimized for a given controller or processor and application.

Figure 8 shows a simple, basic 4-wire connection between a host processor and the LTC1417. This interface consists of a convert-start signal, serial shift clock, serial data and an end-of-conversion signal. The conversion is started by applying a logic low to the LTC1417's $\overline{CONVST}$ pin. The conversion is completed using the internal clock. This same clock is present on the CLKOUT pin and is used by the processor to latch the data that is generated and read during the conversion. The $\overline{BUSY}$ output changes to a logic low at the start of conversion, remains low during conversion, framing the data, and returns to a logic high at the end of conversion.

Figure 9 shows a more complex, but more versatile, interface. This configuration uses the LTC1417's internal clock to step through the

Figure 9. This connection uses the LTC1417's internal clock to clock the conversion. The data is held internally until the processor asserts $\overline{RD}$, applies an external clock and retrieves the data.

conversion and an externally supplied clock to retrieve the data after the conversion's completion. This configuration allows the ADC to complete the conversion and store the data in the background, after which the processor, when it is ready, asserts $\overline{RD}$ and retrieves the data.

Perfect for Telecom: Wide Dynamic Range

With its low noise and low distortion, the LTC1417 offers extremely wide dynamic range over its entire Nyquist bandwidth. This benefit is essential to applications such as telecommunications systems. Spurious free dynamic range is typically 95dB and only starts to drop off at input frequencies above Nyquist. The ultralow $5ps_{RMS}$ jitter of the sample-and-hold keeps the SNR flat from DC to 1MHz, making this device useful for undersampling applications.

Another important requirement for telecom systems is a low error rate. In any ADC, there is a finite probability that a large conversion error (greater
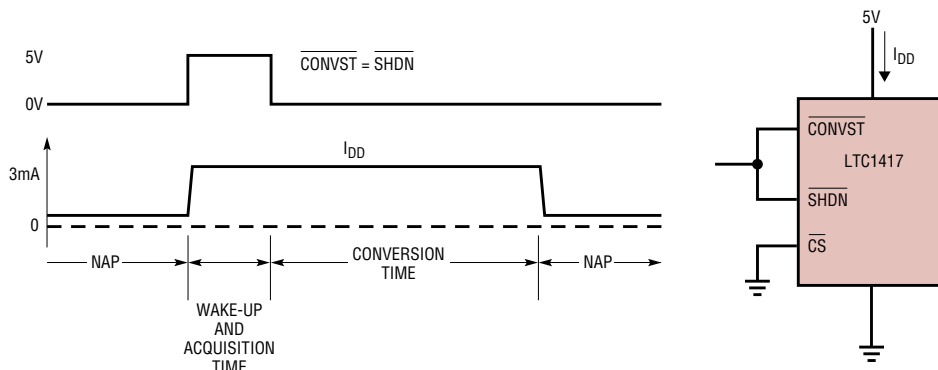

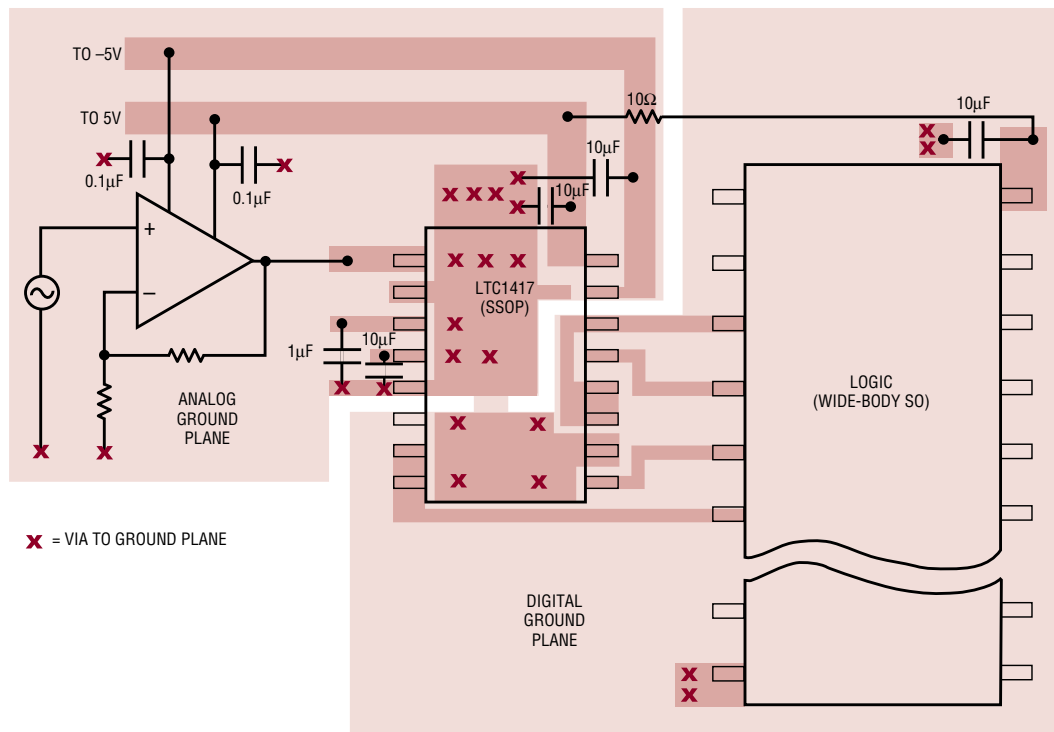**Figure 10. NAP mode between conversions**

Figure 11. This suggested layout, with analog and digital ground planes, closely positioned bypass components and multiple ground connections between the ADC's ground pin and the ground planes, maximizes the LTC1417's AC performance.

than 1% of full scale) will occur. In video or flash converters, these large errors are called "sparkle codes." Large errors are a problem in telecom systems such as ISDN, because they result in data-transmission errors. All ADCs have a rate at which errors occur, referred to as the error rate. The error rate is dependent on the ADC architecture, design and process. Error rates vary greatly and can be as low as one in ten billion to as high as one in one million. Telecom systems typically require error rates to be one in one billion or better.

A benefit of the LTC1417's design is ultralow error rates. The error rate is so low that it is difficult to measure because of the time between errors. To make measurement more practical, the error rate was measured at an elevated temperature of 150°C, because error rate increases with temperature. Even at this high temperature, the error rate was one in 100 billion. The projected error rate at room temperature is one in 2,000,000 billion or about one error every 158 years if running at the full conversion rate.

Ideal for Low Power Applications

LTC1417 is especially well suited for applications that require low power and high speed. The normal operating power is low—only 20mW. Power may be further reduced if there are extended periods of time between conversions. During these inactive periods when the ADC is not converting, the LTC1417 may be shut down. There are two power shutdown modes: NAP and SLEEP.

NAP mode shuts down 85% of the power and leaves only the reference and logic powered. The LTC1417 can wake up from NAP mode very quickly; in just 500ns it can be ready to start converting. In NAP mode, all data-output control is functional; data from the last conversion prior to starting NAP mode can be read during NAP mode. $\overline{RD}$ controls the state of the output buffers. NAP mode is useful for applications that must be ready to immediately take data after long inactive periods.

With slow sample rates, power can be saved by automatically invoking NAP mode between conversions.

Referring to Figure 10, the $\overline{SHDN}$ and $\overline{CONVST}$ pins are driven together. A conversion will be started with the falling edge of this signal; once the conversion is completed, the ADC will automatically shut down. Before the next conversion can start, the $\overline{CONVST}$ and $\overline{SHDN}$ pins must be brought high early enough to allow for the 500ns wake-up time. Power drops with the sample frequency until it approaches the power of the reference circuit, about 2mW at frequencies less than 10kHz.

The SLEEP mode is used when the NAP-mode current drain is too high or if wake-up time is not critical. In SLEEP mode, all bias currents are shut down, the reference is shut down and the logic outputs are put in a high impedance state. The only current that remains is junction leakage current, less than 1µA. Wake-up from the SLEEP mode is much slower, since the reference circuit must power up and settle to 0.01% for full accuracy. The wake-up time is also dependent on the value of the compensation capacitor used on the REFCOMP pin; with the recommended 10µF capaci-

tor, the wake-up time is 10ms. SLEEP mode is useful for long inactive periods, that is, times greater than 10ms.

Layout Considerations

As with other high resolution, high speed ADCs, the LTC1417 needs some basic attention to layout details. These include grounding, bypassing and lead inductance. The best performance is achieved when the LTC1417 is treated as an analog part, powered by an analog supply and grounded to an analog ground plane through its DGND and AGND pins. The analog and digital ground planes should be connected at only one of two places, the LTC1417's DGND pin or a PCB's

ground input. Elsewhere, the analog ground plane should never underlie or touch the digital ground plane. To ensure minimum inductance and best performance, the analog ground plane can be overlaid by analog supply traces or the power plane that feeds the LTC1417 5V or ±5V power. Figure 11 shows some suggestions for proper layout, bypassing and connections for an op amp when needed.

There are some important points to remember to achieve the best performance from the LTC1417. Use 10µF (1µF for V_{REF}) surface mount ceramic capacitors with the shortest and widest possible traces to bypass

the supply, V_{REF} and $V_{REFCOMP}$ pins. Maximizing trace area reduces inductance and maximizes bypass capacitor performance. Power, reference and ground traces should also be as wide as possible.

Conclusion

The new LTC1417 low power, 14-bit ADC will find uses in many types of applications, from industrial instrumentation to telephony. The LTC1417's adaptable analog input and serial output reduce the need for expensive support circuitry. This can result in a smaller, lower cost system. *LT*
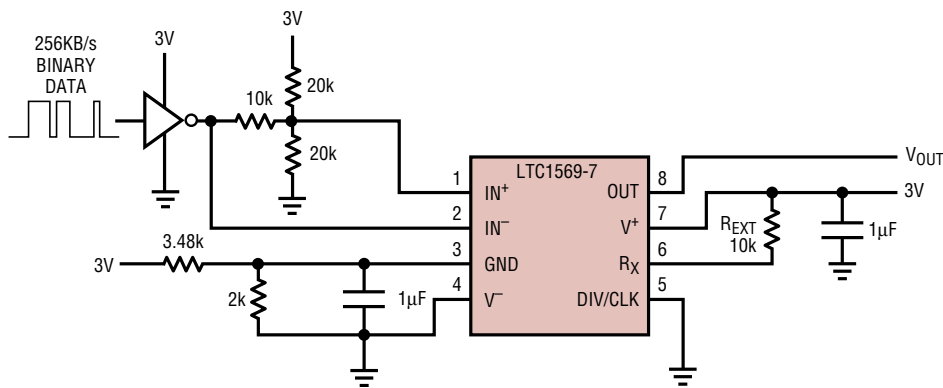

Figure 5. 3V DC-coupled, differential pulse-shaping filter

a single-supply system. For maximum dynamic range, the GND reference for the filter is set to V+/3. The CMOS input data is attenuated by 3x, filtered and appears at the output as $1V_{P-P}$ signal centered about V+/3 .

By tying the IN⁻ input to GND, the LTC1569-6/LTC1569-7 accommodate single-ended AC- or DC-coupled interfaces. The signal range of each input includes the full power supply range. The output voltage range is typically (V⁻ + 50mV) to (V⁺ – 0.8V).

DC Performance and Dynamic Range

The LTC1569-6/LTC1569-7 are well suited for systems requiring DC accuracy and dynamic range. The offset voltage is less than 5mV for 3V supplies, the DC linearity is 12 bits and

the DC common mode rejection of the differential input is 80dB. Given the total integrated noise of $95\mu V_{RMS}$ (LTC1569-6), the filter has over 80dB of dynamic range for a 5V supply. For $1V_{P-P}$ signal levels, the filter has –80dB THD.

Differences Between the LTC1569-6 and the LTC1569-7

The LTC1569-6 is a lower power, lower noise version of the LTC1569-7. The LTC1569-7 is intended for systems needing the maximum bandwidth (150kHz/300kHz on a 3V/5V supply). The LTC1569-6 has twice the oversampling ratio, resulting in a 3dB reduction in the total integrated noise. The maximum sampling rate of the LTC1569-6 was reduced to realize as much as a 50% reduction in power

consumption. The result is a high performance, low power filter suitable for 3V and 5V applications with cutoff frequencies up to 64kHz. All other features of the LTC1569-7 (response, accuracy, tunability) are retained in the LTC1569-6.

Conclusion

The LTC1569-X is the industry's first high performance monolithic filter with built-in precision tuning. The carefully chosen response is ideal for data communications or data acquisition in the 1kHz to 300kHz range. The small footprint, speed/power options, differential interface and 3V to ±5V operation make the LTC1569-6/LTC1569-7 an excellent solution for any lowpass filtering application. *LT*

Single-Inductor, Positive-Output Buck/Boost Converter Uses No R$_{SENSE}$ Controller

by Christopher B. Umminger

The LTC1625 No R$_{SENSE}$™ controller can be used in a power-converter topology that is capable of both up and down conversion and requires only a single inductor. An example of such a circuit, shown in Figure 1,

provides a 12V output with inputs that can range from 18V down to 6V. All of the circuitry to the left of the inductor is identical to that of a typical buck converter implemented with the LTC1625. However, the output (right) side of the inductor is also switched, using an additional pair of MOSFETs (M3 and M4). During the first phase of each cycle, switches M1 and M3 are on while M2 and M4 are off. The input voltage is applied across the inductor and its current increases. In the second phase, M1 and M3 are turned off while M2 and M4 are turned on. Current is then delivered to the output with V$_{OUT}$ applied across the inductor.

This type of converter has several significant differences compared to the buck topology that is usually used with the LTC1625. First, the duty cycle relationship is now equal to V$_{OUT}$/(V$_{IN}$ + V$_{OUT}$). When V$_{IN}$ is equal to V$_{OUT}$, a fifty percent duty cycle is required to balance the volt-seconds across the inductor. Second, both the

input and output capacitors must filter a square pulse current. This increases the required power handling capability of the output capacitors. Finally, the average value of the inductor current is equal to the sum of the input and output currents. Thus, the inductor is larger than that required by a pure buck or boost converter. This last point also has a bearing on the current-limit behavior.

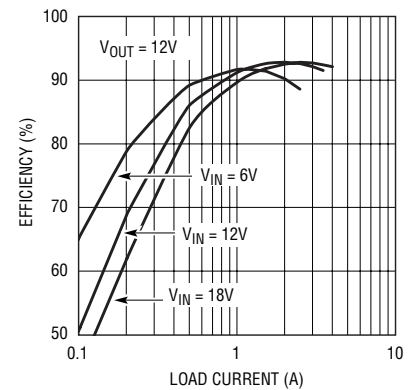**Figure 2. Efficiency vs load current for Figure 1's circuit**

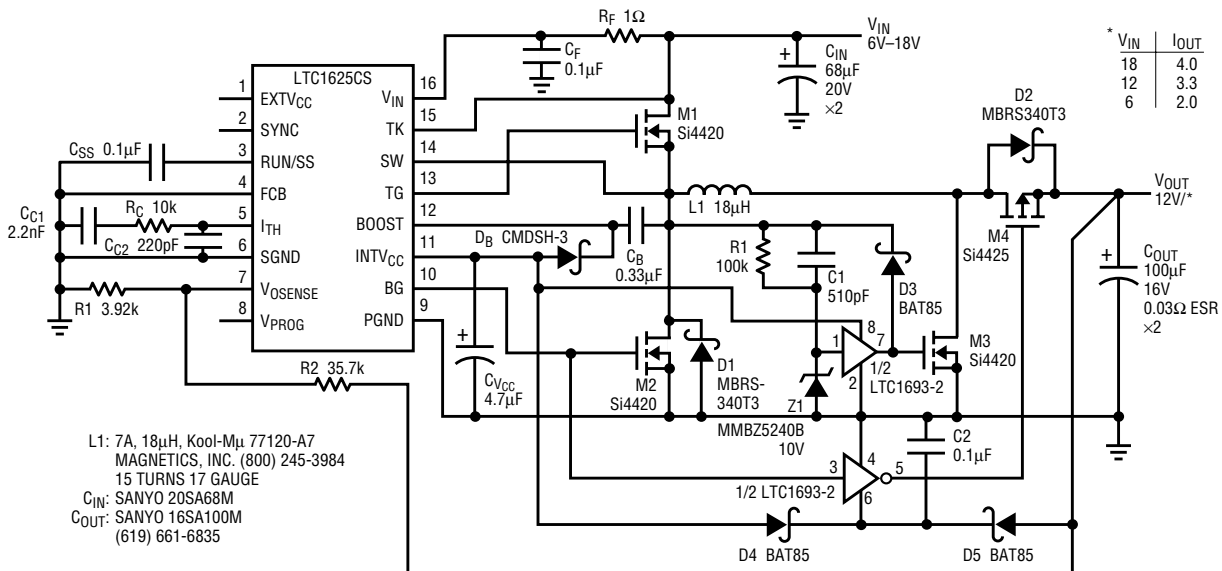**Figure 1. Single-inductor, positive-output buck-boost converter**

Designing the LT1167 Instrumentation Amplifier into a Single 5V Supply Application

by Adolfo A. Garcia

Introduction

In many single-supply applications, the need for precision amplifiers that can operate from 5V (or less) remains strong. While there are many precision, single-supply operational amplifiers currently available on the market that can be configured into 2- and 3-amplifier instrumentation circuits, these designs require great attention to detail to achieve accuracy and precision. Furthermore, although there are single-supply instrumentation amplifier devices on the market, these products trade DC and AC performance for low supply voltage/current operation. Dual-supply instrumentation amplifiers still offer the best performance.

Achieving high precision performance in a single-supply application is practical because the majority of sensor applications provide an output signal centered about the midpoint of a circuit's supply voltage or a reference voltage. Examples of such sensors include strain gauges, load cells and pressure transducers. In these applications, the signal-conditioning circuit is not required to operate near the sensor or circuit's positive supply voltage or ground (common). Even though the signal conditioning circuitry need not operate at the extremes of the supply voltage range, the output voltage swing of the circuit should be as large as possible for maximum dynamic range.

The circuit illustrated in Figure 1 achieves high precision performance while operating from a single 5V supply. The trick here is to reference the dual-supply instrumentation amplifier's inputs to a stable midpoint supply and then follow the instrumentation amplifier with a single-supply precision operational amplifier with a rail-to-rail output stage. This "composite" instrumentation amplifier uses an LT1167 (a high performance instrumentation amplifier in an SO-8 package) for the input stage and an LT1498 (a high speed, precision, rail-to-rail input/output, dual operational amplifier) for the output stage. A stable 5V supply midpoint is provided by the LT1634, a micropower 2.5V precision shunt reference.

Circuit Operation

Here's how the circuit works: The output of the LT1634 shunt reference (U3) is applied to the input of an LT1498 (U2A) configured as a voltage follower. The output of U2A provides a low impedance source required by the LT1167's output reference pin (U1-5) which exhibits a 20k input resistance and an input current of 50µA. A low impedance source is required to maintain the LT1167's high common mode rejection performance. In addition, U2A's output stage can source load currents to 20mA for biasing other external circuitry, without affecting the LT1634's accuracy. The other half of the LT1498 (U2B) is configured as a gain-of-3 inverter so that its output can swing ±2.5V "rail-to-rail" with only ±0.82V drive from the LT1167. The primary reason for choosing an inverting amplifier configuration for the output stage is to make available system DC offset adjustments. Trim networks can be connected to the inverting terminal of U2B without affecting the static or dynamic behavior of the circuit. However, the trim range should be designed so as not to adversely affect the output dynamic range of the circuit.

The LT1167's high linearity performance is maintained on a single 5V supply because its front end has been configured to operate on dual supplies and its output drive level has been relaxed. Because the entire circuit has been level shifted above ground by the LT1634, the circuit's final output voltage must be measured with respect to 2.5V, not 0V.

An expression for the gain of this composite instrumentation amplifier combines the gain equations of the LT1167 and the gain-of-3 inverter.
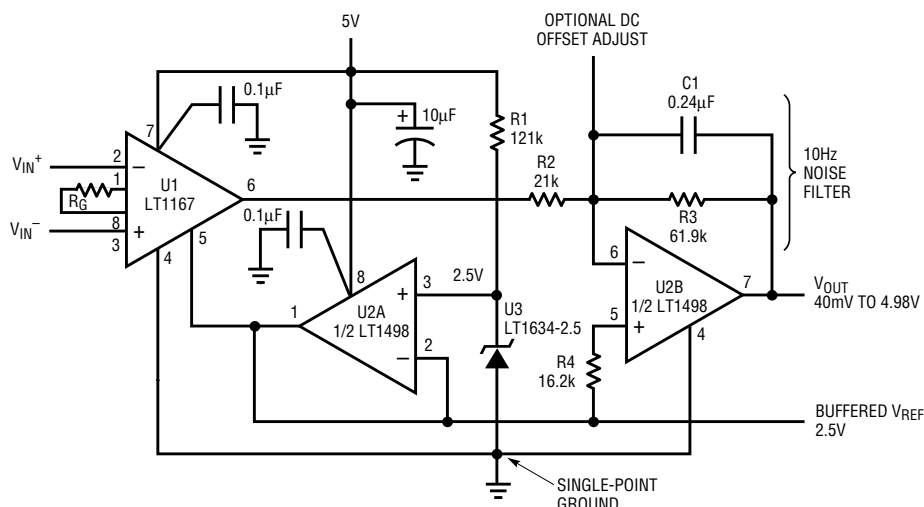

Figure 1. Single-supply instrumentation amplifier with rail-to-rail output stage

This is given by:

$$\text{GAIN} = \left[1 + \left(\frac{49.4\text{k}\Omega}{R_G}\right)\right] \times \left(\frac{R3}{R2}\right)$$

A gain-of-100 composite configuration is realized with R_G = 1.5k. Other gain settings can be realized with various values of R_G, as illustrated in Table 1.

Even though the inputs to the circuit are not required to operate at the positive rail or at ground, wide input common mode operation is always beneficial. In this configuration, the LT1167 input stage can accept signals up to 3.7V (common mode plus differential mode) with no loss of precision. In fact, at low circuit gains, the circuit's common mode input voltage range spans 2.25V to 3.45V. This wide input common mode range allows room for the full-scale differential input voltage to drive the output ±2.5V about the reference point (V_{REF}). Here's another application hint regarding this circuit: though the LT1167's input bias currents are less than 1nA, the differential input terminals still require a DC return path to ground. For more information regarding this topic, please consult the LT1167 data sheet.

The static and dynamic performance of the composite instrumentation amplifier is summarized in Table 1.

Table 1. Performance summary of 5V single-supply instrumentation amplifier with rail-to-rail outputs

Circuit Gain	R_G (Ω)	V_{OS}, RTI* (μV)	TCV_{OS}, RTI* (μV/°C)	Nonlinearity	Bandwidth (kHz) w/o C1	0.1Hz to 10Hz Noise, RTI* (μV$_{P-P}$)
10	20.5k	1300	6.5	< 0.006%	900	2
30	5.36k	450	2.3	< 0.006%	850	0.7
100	1.5k	160	0.8	< 0.006%	500	0.4
300	487	100	0.5	< 0.006%	160	0.3
1000	147	90	0.4	< 0.006%	40	0.3
*RTI is an acronym for error "referred to input."						

The transient response of the circuit as a function of gain and load is well behaved, and is attributable to the LT1498's wideband rail-to-rail output stage . Its 10MHz gain-bandwidth product and 6V/μs slew rate ensure that the small-signal performance of the circuit is dominated by the LT1167. Capacitor C1 is recommended for low frequency applications (signal bandwidths <20Hz) to eliminate or significantly reduce noise pickup. Noise can also be injected into the circuit via the input terminals of the LT1167, especially if the sensor is located remotely from the signal conditioning circuitry. This type of noise can cause a shift in the input offset voltage of the LT1167, thereby producing an error. This effect is commonly known as RFI rectification. A differential filter can be easily added to the LT1167's input terminals to reduce the effects of RFI rectification. Please consult the LT1167 data sheet for additional information on this topic.

Conclusion

As this design idea illustrates, the precision DC performance of a dual-supply instrumentation amplifier can be successfully applied to single-supply, bridge-type sensor applications using a precision rail-to-rail dual operational amplifier. The combination of the LT1167, the LT1498 and the LT1634 yields a cost-effective solution for 14-bit signal conditioning applications. **LT**

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The LTC1625 uses MOSFET V_{DS} sensing to control the inductor current peaks. Thus, the controller limits the average value of the inductor current rather than the output current in this topology. Because the input current varies as V_{IN} is changed, the limit on output current depends upon the input voltage. With V_{IN} = 12V, the maximum output current is about 3.3A. Efficiency of the circuit is shown in Figure 2.

Nonoverlapping control signals for the switches M2 and M4 are generated from the LTC1625 and buffered by an LTC1693-2 dual MOSFET driver. Note that the control signal for the PFET M4 must be able to swing between ground and V_{OUT}. Thus, the inverting half of the LTC1693-2 is powered from a diode-OR between $INTV_{CC}$ (for start-up) and V_{OUT}.

Several simplifications are possible for this circuit. The switch node can be connected directly to M3's gate, provided that V_{IN} remains below the maximum rated gate voltage. This eliminates R1, C1, Z1, D2 and the buffer portion of U2. The second stage could also be made nonsynchronous by replacing D2 with a larger diode, such as an MBRD835L, and eliminating M4, D4, D5, C2 and the inverting portion of U2. Nonsynchronous operation reduces the peak efficiency by two to three percent. **LT**

Low Voltage PowerPath Driver Switches from a 3.3V or 5V Supply to Battery Backup

by Peter Guan and
Tim Skovmand

The LTC1473L solves the problem of seamless power switching between 3.3V or 5V supplies and backup battery packs (3- or 4-cell NiMH) at high current levels. By driving two sets of back-to-back N-channel MOSFET switches, the LTC1473L routes power to the input of a low voltage (3.3V to 10V) system efficiently and inexpensively. An internal micropower boost regulator is included to fully enhance the external NMOS switches, even at low operating voltages. An external 1mH inductor and 1µF capacitor charge V_{GG} to approximately 8.5V above V^+, providing ample drive for the external MOSFETs. The LTC1473L includes inrush-current limiting during supply switchover to produce smooth transitions between the DC supply and the battery backup and to ensure that the load capacitors are always charged and discharged in a controlled fashion.

During start-up or under abnormal operating conditions, when voltages are varying, current can still pass to the output load from the higher input source if the $\overline{\text{Diode}}$ pin is enabled. Enabling the $\overline{\text{Diode}}$ pin essentially converts the two external MOSFETs into diodes. This "2-diode mode" is defeated when V^+ drops below 2.5V.

Continuous short-circuit protection is also provided by a programmable timer that limits the amount of time the switches are allowed to be in current limit. When the time limit is reached, the LTC1473L removes the gate drive and then retries the offending switch, with a very small duty cycle, until the short circuit is removed, thus limiting all power dissipation to safe levels. The LTC1473L is housed in a space-efficient 16-pin narrow SSOP package and drives a wide range of N-channel MOSFET switches.

Figure 1 is a schematic diagram of an automatic PowerPath™ switch for 3.3V applications. The LTC1442 micropower, low voltage, dual comparator monitors the DC supply rail with its internal 1.182V reference and

an external resistor divider. As soon as the supply falls below 3V, the two comparator outputs change state and invert the two logic inputs (IN1 and IN2) of the LTC1473L. This action smoothly switches the load from the DC supply to the backup battery pack. For hysteresis on the comparator's trip point, an additional resistor divider can be added between the REF (6), HYST (5), and V^- (2) pins of the LTC1442 (refer to the LTC1442 data sheet for details).

Figure 2 is a schematic showing the LTC1473L switch controller in conjunction with an LT1512 battery charger. In this application, the 4-cell NiMH battery is fully charged by the 3.3VDC supply through the LT1512 buck-boost converter to ensure that it is always "topped off" and ready to provide backup power. R3 is set at 1Ω to charge the NiMH battery pack at a constant 100mA rate.

In both applications, the value of C_{TIMER} determines the amount of time
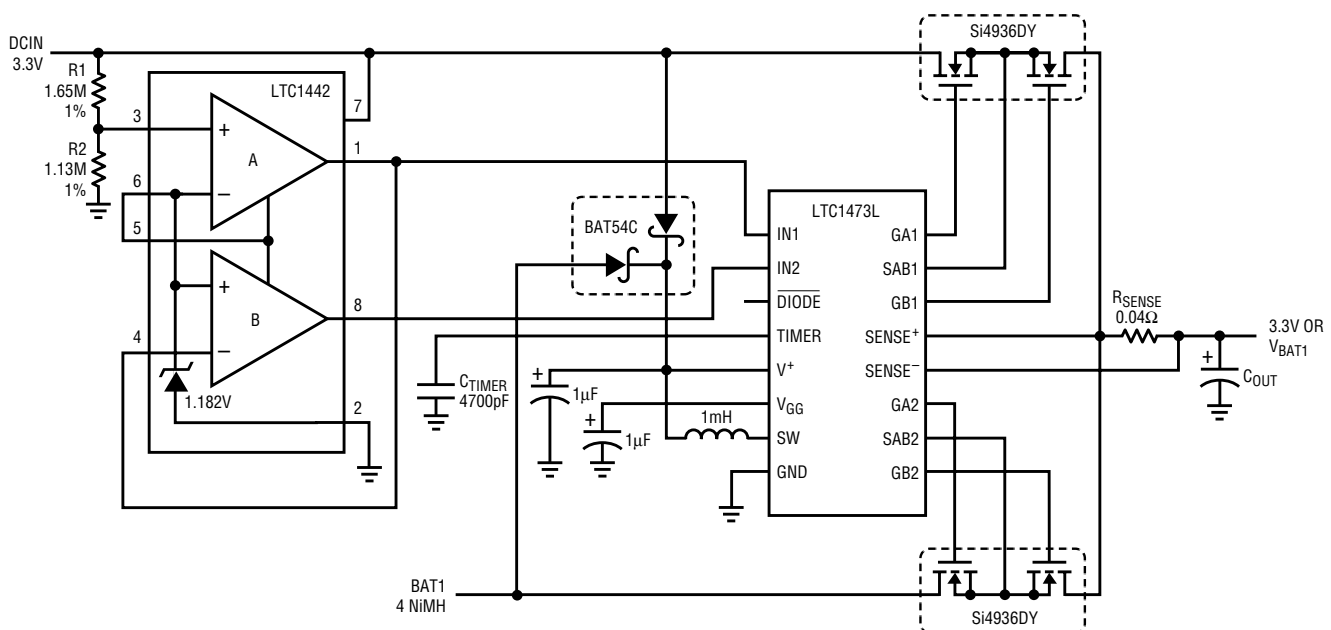
Figure 1. Automatic PowerPath switching for 3.3V applications

20A Constant Current Source/Battery Charger is 95% Efficient

by Goran Perica

Introduction

Generating precise, high DC currents presents a challenge due to the need for a current sensor that is sufficiently precise and low in cost and power dissipation. A current sense resistor is the most common type of current sensor. Current sense resistors can be very low in cost and are easy to use. Unfortunately, current sense resistors dissipate some power. Just how much power a current sense resistor will dissipate depends on the control circuit used for current sensing and the required precision of the output current. Another type of current sensor is based on Hall-effect devices. Although Hall-effect sensors meet the low power requirement, they are more difficult to use and are more expensive. Also, Hall-effect sensors

have a limited bandwidth of 20kHz to 50kHz; as a result, a current regulator based on such a sensor has a slow transient response. As far as the cost and simplicity are concerned, current sense resistors are the better choice, as long as power dissipation is within the acceptable limits. The power dissipation in a current sense resistor depends on the current and the voltage across the resistor. Hence, keeping the voltage drop across the current sense resistor low is very important. The circuit in Figure 1 is a constant-current (CC), constant-voltage (CV) DC/DC converter that generates 20A of output current and maintains efficiency greater than 95% with a 24V input and 12.6V output.

Circuit Description

To achieve high efficiency, the circuit in Figure 1 employs the LTC1625 No R$_{SENSE}$™ current mode DC/DC controller and LT1620 rail-to-rail current sense amplifier. The LTC1625 current mode controller does not require a current sense resistor to obtain the instantaneous current feedback for current mode operation. The instantaneous current value is obtained by sensing the voltage drop across power MOSFETs M1 and M2. Also, the LTC1625 provides overcurrent protection with current foldback that is based on the voltage drop across the MOSFETs. Unfortunately, the R$_{DS(ON)}$ of MOSFETs is a poorly controlled parameter that yields an overcurrent protection variation of more than 30%.
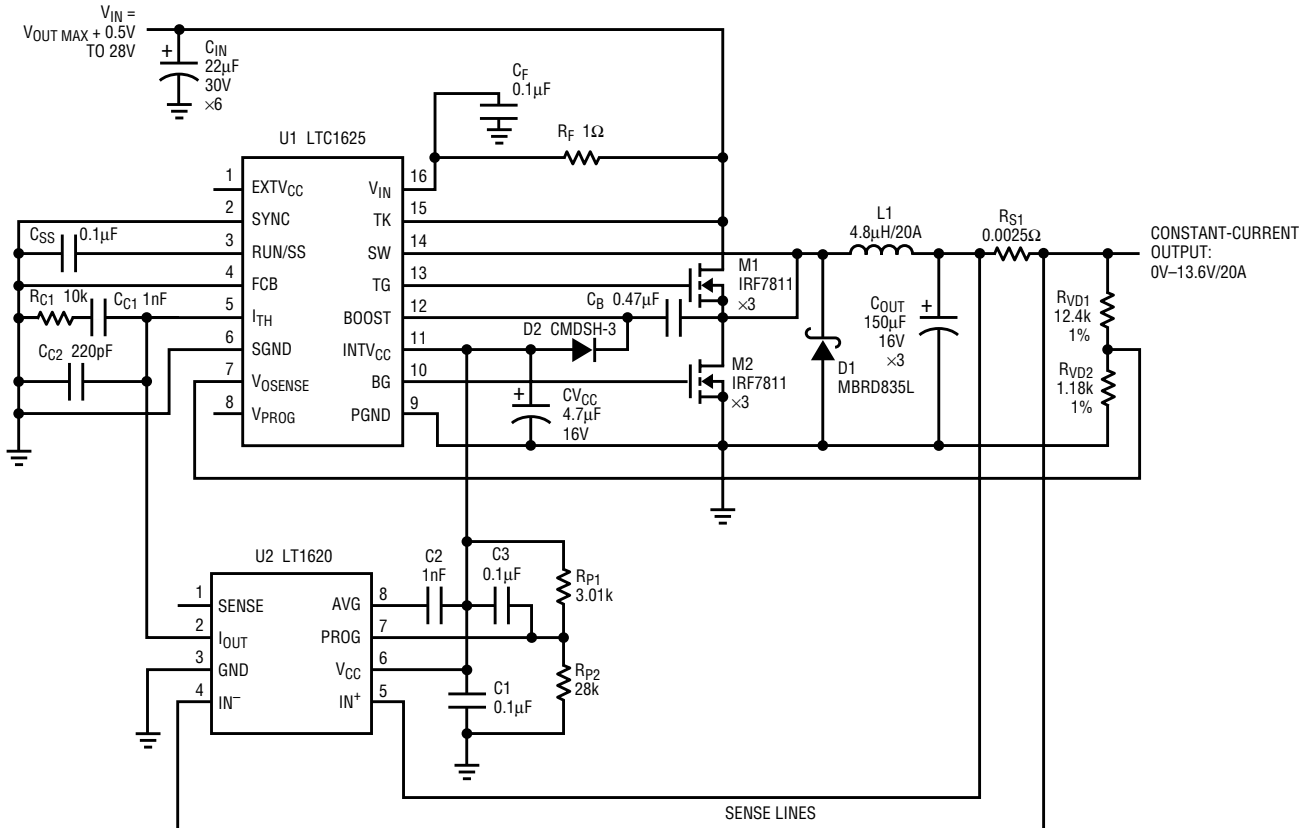

Figure 1. Constant-current (CC), constant-voltage (CV) DC/DC converter generates 20A of output current and maintains efficiency greater than 95% at a 24V input and 12.6V output.

The LT1620 achieves precise output current control. The minimum current limit of LTC1625 circuit must be set above the desired output current controlled by LT1620. The LT1620 current sense amplifier controls the LTC1625 via the I_{TH} control pin. When the LT1620 does not pull down on the LTC1625's I_{TH} pin, the circuit operates in constant voltage (CV) mode.

Constant-Voltage Operation

When the output of the circuit in Figure 1 is left open or the load draws less than the programmed output current, the circuit operates in constant voltage mode (CV). In this condition, the LT1620 does not control the feedback loop. For a load current of less than 20A, the output voltage is set to the value controlled by output voltage divider R_{VD1} and R_{VD2}. In the case of the circuit in Figure 1, the open-circuit output voltage is set to 13.6V, which is adequate for charging lead-acid batteries at room temperature. This voltage should have temperature compensation if the batteries are exposed to wide temperature variations. Temperature compensation is beyond the scope of this article—see AN51, Figure 16 for a simple compensation scheme, or consult the battery manufacturer for information.

Constant-Current Operation

The output current is set by the voltage (V_{PROG}) across the resistor R_{P1} and by the value of output current sense resistor R_{S1}. The LT1620 has a current sense amplifier with a gain of 10, which sets the actual current sense voltage to $V_{PROG}/10$. Therefore, the output current (I_{OUT}) will be:

$$I_{OUT} = (0.1 \cdot V_{PROG})/R_{S1}$$

where R_{S1} is the value of the output current sense resistor.

To obtain the highest possible precision, resistor R_{S1} should have separate voltage sense terminals (Kelvin, 4-terminal). The circuit in
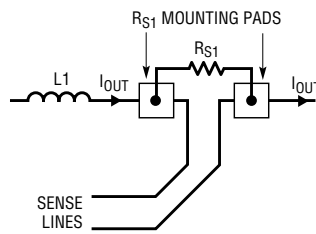

Figure 2. Detailed view of connection to R_{S1}

Figure 1 has V_{PROG} set to 0.5V, resulting in 50mV of sense voltage across R_{S1} at the constant-current threshold. The resulting power dissipation in resistor R_{S1} at 20A of output current is only 1W. If the circuit in Figure 1 is used as a 12V, 20A battery charger, the efficiency loss in R_{S1} is only 0.4%.

If a 2-terminal resistor is used, attention should be paid to connecting the current sense amplifier inputs (IN– and IN+) as close to the body of R_{S1} as possible. Connect the sense lines to the R_{S1} mounting pads as shown in Figure 2. By connecting the sense lines on the opposite sides of the output current flow (I_{OUT}) as shown, the current sense error will be minimized. In any case, some error will result from using 2-terminal resistors for R_{S1}. The output current error can be further minimized by increasing the program voltage, V_{PROG}, by an amount proportional to the increase of resistance R_{S1} due to termination resistance of R_{S1}. Because the value of R_{S1} is on the order of a few mΩ, termination resistance may be affected by such things as the type of solder used, size of component mounting holes, amount of copper on the PCB and whether the sense pins are connected on the side of R_{S1} or on the opposite side of printed circuit board.

The circuit in Figure 1 can be extended to even higher currents. To achieve the higher output currents, more MOSFETs can be used in parallel. An additional PNP/NPN gate drive buffer is also recommended. Integrated MOSFET drivers are not recommended because of the time

delays that prevent proper operation of the LTC1625.

PCB Layout

The LTC1625 relies on the $R_{DS(ON)}$ of MOSFETs M1 and M2 for overcurrent protection. Because MOSFET $R_{DS(ON)}$ is highly dependent on junction temperature, it is very important to keep the junction temperature as low as possible by selecting MOSFETs with low $R_{DS(ON)}$ values. This also improves efficiency due to lower voltage drops across M1 and M2. If surface mount MOSFETs are used (SO-8, D-Pak or D^2-Pak), good thermal management is required.

Best results can be obtained by using a multilayer printed circuit board with one or two of the inner layers used for a solid ground plane and/or a solid V_{CC} plane. These planes serve as heat spreaders. The solid inner planes (GND, V_{CC} or both) should be right next to the PCB layer where the MOSFETs are mounted. The thermal resistance between the MOSFETs package and solid inner plane depends on the distance between the two layers. Minimizing the distance between the heat spreading layer and the layer on which the MOSFETs are mounted will ensure the smallest temperature rise due to heat dissipation in the MOSFETs.

Conclusion

The circuit in Figure 1 presents a simple and efficient solution for battery charging and other applications requiring constant-current DC output. The new LTC1625 current mode controller makes it possible to achieve high output currents while maintaining high efficiency, due to its novel approach of sensing the voltage dropped across the on-resistance of the switching MOSFETs. The addition of the LT1620 as the output current controller allows the circuit to achieve high output-current precision. *LT*

LTC2400 Differential Bridge Digitizers

by Kevin R. Hoskins and Derek Redmayne

This Design Idea covers two circuits that convert differential signals to single-ended, ground referred signals for input to the LTC2400 delta-sigma ADC. These circuits were designed to have a minimal effect on the LTC2400's 1ppm typical accuracy. The circuit in Figure 1 is ideal for low level differential bridge outputs in applications that have ±5V supplies. The circuit in Figure 2 is ideal for low level differential bridge outputs, typically 2mV/V, in single-supply applications, and features "live at zero" operation. ("Live at zero" refers to a topology with an elevated ground, allowing the amplifier to drive signals below the LTC2400's negative rail.) Both circuits were tested using the LTC2400 demonstration board. The V_{CC} and V_{REF} for the LTC2400 in Figure 1's circuit are generated by an LT1236-5.

The circuit in Figure 2 uses a simple voltage reference (the Schottky diode and NPN transistor) to bias the single-ended signal approximately 270mV above ground. For single-supply applications, this bias voltage and "live at zero" operation allows the LTC1050 and the LTC2400 to amplify and convert signals that include inputs below ground.

Both circuits combine an LTC1043 precision switched capacitor block and an LTC1050 chopper stabilized op amp, creating a differential input, single-ended output bridge amplifier that has a rail-to-rail common mode input range. The LTC1043 samples a differential input voltage, holds it on C_S and transfers it to a ground-referred capacitor, C_H. The voltage on C_H is applied to the LTC1050's noninverting input and amplified by the gain set by resistors R1 and R2 (101 for the values shown). The amplifier's output is then converted to a digital value by the LTC2400.

The LTC1043 achieves its best differential to single-ended conversion when its internal switching frequency is set by a 0.01µF capacitor, C1, and when 1µF capacitors are used for C_S and C_H. Using any other value will compromise the accuracy. For example, a C1 value of 0.1µF will typically increase the circuit's overall nonlinearity tenfold. C_S and C_H should be a film type such as mylar or polypropylene. Conversion accuracy is enhanced by placing a guard shield around C_S and connecting the shield to pin 10 of the LTC1043. This mini-mizes nonlinearity that results from stray capacitance transfer errors associated with C_S. Consult the LTC1043 data sheet for more information. As is good practice in all high precision circuits, keep all lead lengths as short as possible to minimize stray capacitance and noise pickup.

The LTC1050's closed-loop gain accuracy is affected by the tolerance of the ratio of the gain-setting resistors. If cost considerations preclude using low tolerance resistors (0.02% or better), the processor to which the LTC2400 is connected can be used to perform software correction. Operated as a follower, the LTC1050's gain and linearity errors are less than 0.001%.

The circuit in Figure 1 shows an optional resistor, R_S. This resistor can be placed in series with the LTC2400's input to limit current if the input goes below –300mV. The resistor does not degrade the converter's performance.

The circuit in Figure 2 receives a very low level output from a bridge excited by only 2.5V. It uses bandwidth limiting and an attenuator after the amplifier to reduce input referred noise and autozero commutating noise
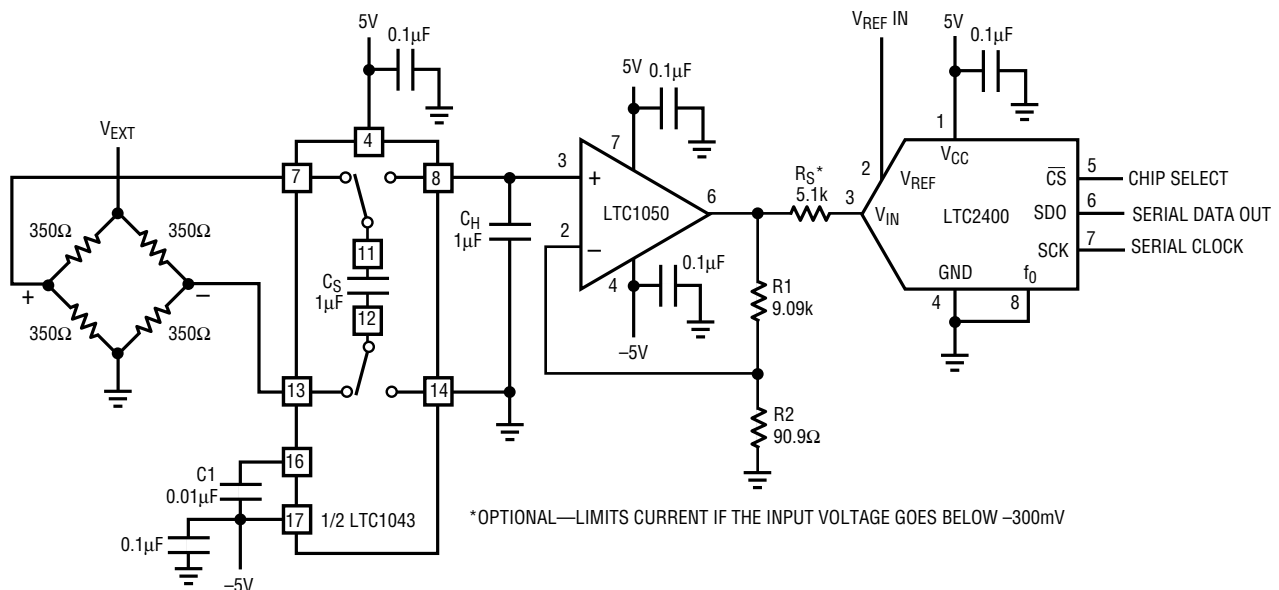

Figure 1. LTC2400 bridge digitizer for ±5V supplies

Table 1. Performance specifications for the circuits in Figures 1 and 2

Parameter	Figure 1	Figure 2	LTC2400	Units
Input Voltage Range	−3 to 40	−0.5 to 5		mV
Zero Error	12.7	2	1.5	µV
Input Current	(See Text)	(See Text)		
Nonlinearity	±1	±5	4	ppm
Noise (without Averaging)	0.3*	0.21*	1.5	µV$_{RMS}$
Noise (Averaged 64 Readings)	0.05*	0.026*		µV$_{RMS}$
Resolution (with Averaged Readings)	19.6	17.2		Bits
Overall Accuracy (uncalibrated)	20**	17.6**		Bits
Supply Voltage	±5	5	5	V
Supply Current	1.6	2.6	0.2	mA
CMRR	120	120		dB
Common Mode Range	±5	0 to 5		V

Specifications: $V_{CC} = V_{REF}$ = LTC1236-5 for Figure 1, LT1019-2.5 for Figure 2; V_{FS} = 40mV; R_{SOURCE} = 175Ω(Balanced)

  *Input-referred noise with a gain of 101
**Offset and gain error removed

as much as possible. The noise gain shown (101) allows adequate headroom for the expected signal; the attenuator reduces the overall gain to 16.8. This is approximately the point, when using the LTC1050 and the LTC2400, where additional gain produces no additional reduction in input-referred noise.

Another source of error is thermocouple effects that occur in soldered connections. These effects are most pronounced in the circuit's low level portion, before the LTC1050's output. Any temperature changes in any of the low level circuitry's connections will effect linearity in the final conversion result. These effects can be minimized by balancing the thermocouple connections with reversed redundant connections and by sealing the circuit against moving air.

Each circuit's input current is dependent on the input signal's common mode voltage. The circuit in Figure 1 has an input current of approximately –100nA and 100nA respectively, relative to the limits of the common mode range, dropping to zero at 0V common mode. The circuit in Figure 2 has an input current of approximately 100nA at a common mode input of 5V, dropping to zero at 0V common mode. The input-current values may vary from part to part. The input of each circuit is analogous to a 2µF capacitor in parallel with 25MΩ connected to ground. The LTC1043's nominal 800Ω switch resistance is between the input signal source and the 2µF capacitance. ⌐⊿
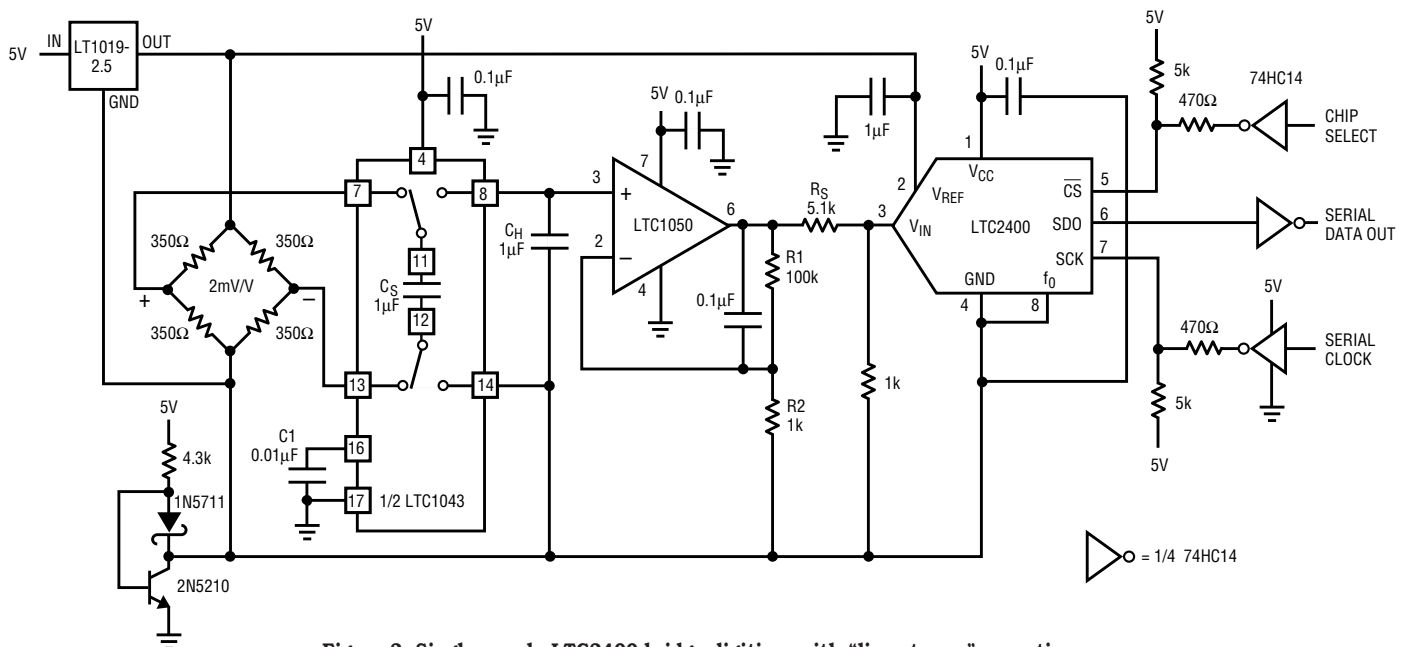

Figure 2. Single-supply LTC2400 bridge digitizer with "live at zero" operation

4.5µA Li-Ion Battery Protection Circuit

by Albert Lee

Li-Ion Battery Undervoltage Lockout

Figure 1 shows an ultralow power, precision undervoltage-lockout circuit. The circuit monitors the voltage of a Li-Ion battery and disconnects the load to protect the battery from deep discharge when the battery voltage drops below the lockout threshold. Storing a battery-powered product in a discharged state puts the battery at risk of being completely discharged. In a discharged condition, current to the protection circuitry continuously discharges the battery. If the battery is discharged below the recommended end-of-discharge voltage, overall battery performance degrades, the cycle life is shortened and the battery may die prematurely. In contrast, if the lockout voltage is set too high, maximum battery capacity is not realized.

The low-battery mode of operation is indicated when, for instance, a cell phone automatically powers down after the battery-low indicator has been flashing for some time. If the phone is misplaced in this condition and found months later, the protection circuitry shown in Figure 1 will not overdrain and damage the battery because the protection circuitry takes less than 4.5µA of current. At this low current, the time the Li-Ion battery takes to reach the end-of-discharge voltage is significantly extended. For other protection circuitry that typically requires higher current, the rate of discharge is faster, allowing the battery voltage to drop below the safe limit in a shorter time. Note that if the battery is allowed to discharge below the safe limit, unrecoverable capacity loss occurs.

The Micropower Voltage Reference and Op Amp

The LT1389 is not just another voltage reference. Its very low current consumption makes it the ideal choice for applications that require maximum battery life and excellent precision. It requires only 800nA of current and provides 0.05% initial voltage accuracy and 20ppm/°C maximum temperature drift, equating to 0.19% absolute accuracy over the commercial temperature range and 0.3% over the industrial temperature range. Operating at one-fifteenth the current required by typical references with comparable accuracy, the LT1389 is the lowest power voltage reference available today. The LT1389 precision shunt voltage reference is available in four fixed-voltage versions: 1.25V, 2.5V, 4.096V and 5.0V. It is available in the 8-lead SO package, in commercial and industrial temperature grades.

Low power ($I_S < 1.5µA$) and precision specifications make the LT1495 rail-to-rail input/output op amp the perfect companion to the LT1389. The extremely low supply current is combined with excellent amplifier specifications: input offset voltage is 375µV maximum with a typical drift of only 0.4µV/°C, input offset current is 100pA maximum and input bias current is 1nA maximum. The device characteristics change little over the supply range of 2.2V to ±15V. The low bias currents and offset current of the amplifier permit the use of megohm-level source resistors without introducing significant errors. The LT1495 is available in plastic 8-pin PDIP and SO-8 packages with the standard dual op amp pinout.

Consuming virtually no current, the LT1389 and the LT1495 are ideal choices for the UVLO circuit and many other battery applications.

Circuit Operation

The circuit is set up for a single-cell Li-Ion battery, where the lockout voltage—the voltage when the protection circuit disconnects the load from the battery— is 3.0V. This voltage, set by the ratio of R1 and R2, is sensed at node A. When the battery voltage drops below 3.0V, node A falls below the threshold at node B, which is defined as:

$$V_B = 1.25V + I \bullet R4 = 1.37V$$
where
$$I = (V_t - 1.25V)/(R3 + R4) = 800nA$$
$$V_t = \text{lockout voltage}$$

The output of U1 will then swing high, turning off SW1 and disconnecting the load from the battery. However, once the load is removed, the battery voltage rebounds and will cause node A to rise above the reference voltage. The output of U1 will then switch low, reconnecting the load to the battery and causing the battery voltage to drop below 3.0V again. The cycle repeats itself and oscillation occurs.

To avoid this condition, R5 is added to provide some hysteresis around the trip point. When the output of U1 swings high to shut off SW1, node B is bumped up 42mV above node A, preventing oscillation around the trip

Figure 1. Undervoltage lockout circuit

(within figure:)
V_{BATT}
SW1
TO LOAD
R1 3.57M 0.1%
R3 2.05M 1%
B
+
U1 1/2 LT1495
−
R_{SW} 1M 5%
A
U2 LT1389 1.250V
Li-Ion CELL 4.1V
R2 3M 0.1%
R4 150k 1%
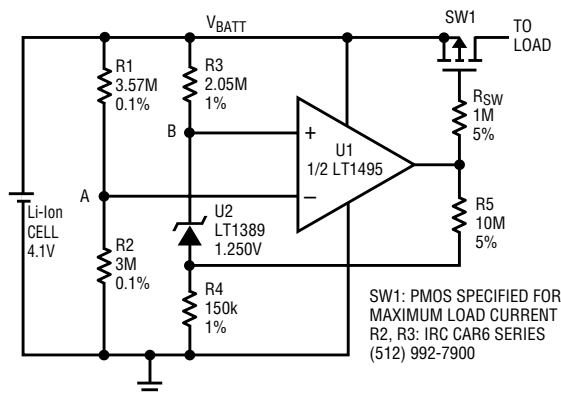R5 10M 5%

SW1: PMOS SPECIFIED FOR MAXIMUM LOAD CURRENT
R2, R3: IRC CAR6 SERIES
(512) 992-7900

point. Using the formula below, the amount of hysteresis for the circuit is calculated to be 92mV. Hence, V_{BATT} must climb back above 3.092V before the battery is connected.

Hysteresis = $V_B' \cdot R1/R2 + V_B - V_t$
where
$V_B' = (V_{OMAX} - I \cdot R4) \cdot R4/R5 + V_{REF} + I \cdot R4$
V_t = lockout voltage
V_{OMAX} = maximum output swing (high) of U1 at V_{BATT} is equal to the lockout voltage

Consult the battery manufacturer regarding the maximum ESR at maximum recommended discharge current. Multiply the two values to get the minimum hysteresis required.

Being Precise

The worst-case voltage-monitor accuracy is better than 0.4%. Interestingly, the battery's longevity and capacity are directly related to the depth of discharge. More cycles can be obtained by partially rather than fully discharging the Li-Ion battery, and, conversely, more use time can be obtained by fully discharging a Li-Ion battery. Cutting off the load at the perfect end-of-discharge voltage would ideally result in the best of both cases. To perform this task requires an accurate overall system. For example, if the optimum lockout voltage is to be set at 3.1V, a 5% overall accurate system would yield

Figure 2. V_{BATT} vs V_A with hysteresis

±155mV, cutting off at either at 2.945V or at 3.255V. At a lockout voltage of 3.255V, maximum capacity is not obtained. In addition, the operating range is reduced, with the fully charged battery voltage being 4.1V. For a 0.4% overall accurate system, the lockout voltage would be at 3.088V or at 3.112V, more than twelve times better accuracy and optimally achieving the highest capacity. Furthermore, the load is kept disconnected with only 4.5µA to the protection circuit. Thus, the protection circuit works by preventing deep discharge of the battery.

Conclusion

There need not be a trade-off between performance and current consumption. The LT1389 nanopower precision shunt voltage reference and the LT1495 1.5µA precision rail-to-rail input/output op amp deliver the highest performance with virtually zero current consumption. ↗

Figure 2. Battery-backup circuit with LT1512 battery charger

PowerPath, continued from page 31
the external NMOS switches are allowed to be in current limit, and the value of R_{SENSE} determines the inrush current limit, which is set at 2× to 3× of the maximum required output current.

When V^+ falls below 2.5V, the LTC1473L's undervoltage lockout circuit turns off both switches. With a built-in hysteresis of 100mV, the LTC1473L becomes active again when V^+ rises above 2.6V. Therefore, for 3.3V systems, small Schottky diodes are used to power V^+ from both DCIN and BAT1 so that the undervoltage lockout circuit will not be falsely tripped. Since the LTC1473L has an I_Q of less than 100µA at 3.3V, the drop across the Schottky diode is less than 0.4V, leaving enough room for a typical ±5% supply tolerance.

Glitch-free and seamless transition of power is crucial for maintaining normal operation in low voltage electronic equipment. The LTC1473L makes the transition transparent and trouble free. (For systems using supply voltages between 6V and 28V, refer to the LTC1473 data sheet.) ↗

New Device Cameos

LTC1663: 10-Bit, Rail-to-Rail Voltage Output, SMBus-Compatible DAC in 5-Lead SOT-23

The LTC1663 is a 10-bit voltage output DAC with true buffered rail-to-rail output voltage capability; its inherently monotonic architecture provides for excellent linearity. Communication with the LTC1663 is via the 2-wire SMBus interface. The interface, combined with the double buffered internal data registers, allows for individual or simultaneous update of multiple devices on a single 2-wire bus. The LTC1663 operates from a single 2.7V to 5.5V supply while consuming only 80µA supply current and maintaining the SMBus-specified 0.6V VIL and 1.4V VIH input thresholds.

Each LTC1663 provides a choice of two references. The reference for the DAC is either the supply voltage or an internal bandgap reference. Selecting the internal bandgap reference will set the full-scale output voltage range to 2.5V. Otherwise, the full-scale range is equal to the supply voltage.

The DAC can be put in low current standby mode for use in power conscious systems. Power-on reset ensures that the DAC output is at 0V when power is initially applied and all internal registers are cleared. The LTC1663 in the 8-lead package includes three user-definable address bits, which can be set for up to eight different addresses for use by multiple devices on the same bus.

The LTC1663 is available in the 5-lead SOT-23 and 8-lead MSOP plastic surface mount packages.

LTC1727/LTC1728: Micropower, Precision Triple Supply Monitors in a Small Outline Package

The LTC1727 is a triple supply monitor intended for systems with multiple supply voltages; it is available in an 8-pin MSOP package. Each supply monitor input has its own open-drain output for individual supply monitoring, as well as a common open-drain reset output with a 200ms delay. The LTC1728 is the 5-pin SOT-23 version of the LTC1727 without the individual monitor outputs. Two of the supply monitor input thresholds are preset at the factory; the third is a high impedance input with a 1V threshold that allows the user to program the monitor voltage.

The LTC1727/LTC1728 are powered from either of the two preset supply monitor inputs, allowing the reset output to be in the correct state, independent of supply sequencing. In addition, the reset output is guaranteed to be in the correct state for supply voltages as low as 1V. Due to a unique architecture, the LTC1727/LTC1728 may also be configured to monitor one or two supply inputs instead of three, depending on system requirements.

The LTC1727/LTC1728 are both available in versions that monitor 3.3V, 5V and adjustable or 3.3V, 2.5V and adjustable, with tight 1.5% accuracy specifications and glitch immunity that ensures reliable reset operation without false triggering. The 15µA typical supply current makes the LTC1727/LTC1728 ideal for power conscious systems.

LTC2408: 8-Channel, 24-Bit, Delta-Sigma ADC

The LTC2408 combines the breakthrough technology developed for the LTC2400 24-bit delta-sigma converter with an 8-channel analog multiplexer. Leveraging the high accuracy and ease-of-use found in the LTC2400, the LTC2408 offers 4ppm INL, 4ppm full-scale, 0.5ppm offset and 0.3ppm noise performance. An internal oscillator eliminates the need for external frequency setting components.

From the user's point of view, the LTC2408 is the simplest to use and most accurate delta-sigma ADC on the market. Single-cycle settling eliminates the need to sift through invalid data each time the input channel is changed. The user may switch the input channel as frequently as once per conversion with no latency or filter settling errors. This simplifies the system software and increases the effective data output rate.

The channel selection and data output are accessible through a simple 4-wire SPI interface. The LTC2408 is available in a 28-lead SSOP package. The device operates from a single 2.7V–5.5V supply and consumes 220µA. *LT*

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

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Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp.
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SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim.
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SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included.
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SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included.
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MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

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1994 Linear Databook, Vol III—This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded.
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