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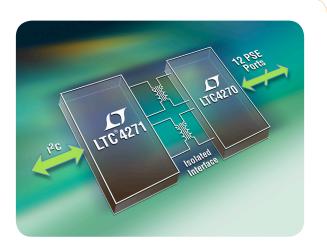
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LTPoE++ Extends PoE to 90W with Reliable and Easy-to-Use Standard

Heath Stewart

Power over Ethernet, or PoE, is an increasingly popular way to deliver both power and data over existing Ethernet cable, thus freeing applications from the constraint of AC-power proximity. As the number PoE solutions has grown so has the applications' appetite for power.

A new proprietary standard, LTPoE++[™], satisfies this hunger by extending the PoE and PoE+ specifications to 90W of PD delivered power. LTPoE++ also dramatically reduces engineering complexity in power sourcing equipment (PSEs) and powered devices (PDs) when compared to other power-expansion solutions.



Linear offers a comprehensive lineup of PoE and LTPoE++ products. The LTC[®]4270/71 chipset reduces PoE costs and complexity by replacing undesireable opto-couplers with a simple off-the-shelf transformer. Like all LTPoE++ products, this chipset also extends PoE delivered power to 90W. Plug-and-play simplicity and safe, robust power delivery are hallmarks of LTPoE++. The capabilities of this standard expand the field of Ethernet-powered applications by several orders of magnitude, enabling entirely new classes of PDs, such as power-hungry picocells, base stations or heaters for pan-tilt-zoom cameras.

HISTORY OF PoE

POE is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added POE capability in 2003. The original POE spec, known as 802.3af, allowed for 48V DC power at up to 13W. Although the initial specification was widely popular, the 13W cap limited the number of possible applications. In 2009, the IEEE released a new standard, known as 802.3at or POE+, increasing the voltage and current requirements to supply 25.5W of power.

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In the lab.

JIM WILLIAMS REMEMBERED

I have known Jim Williams for 30 years. I have known him as the consummate engineer, scientist, writer, humorist, and family man. In all areas that Jim ventured, he excelled. His combination of personal integrity, drive and humble interaction with other people drew many friends, both for his writing and personal interactions.

Jim's intuitive understanding of electronics enabled him to design complicated circuits in his head, which he tested with real parts to prove the circuits. The ability to design circuits also requires analysis of the results of the testing. His strong analytical ability ensured test results were correct and circuits were well understood.

Jim took his developments and turned them into words for publication. He helped engineers of all ages understand circuits intuitively like he did. There are few sources for advanced circuit understanding and design—especially the way it was taught by Jim. His circuits and his writings provided insight so that other people could approach his understanding of design. In all the time I've known Jim, I have never known him to refuse to help someone with a circuit.

While Jim's vocation, avocation and hobby were electronics, he had a great sense of humor and art. His electronic sculptures are unique, beautiful and functional. He built these structures (with much cursing) and careful selection of aesthetically pleasing functional parts. Beyond his art, he had a great sense of humor, which was often foisted on his friends, myself included.

In his personal life, he was a dedicated father to his son Michael and husband to his wife Siu. Both of these people were very much a part of his life.

A successful poet is the rarest of all vocations. Jim Williams was unique: a poet who wrote in electronics.

—Bob Dobkin

Linear in the News

EDN HONORS LINEAR DESIGNERS AS INNOVATORS OF THE YEAR

Robert Dobkin and Tom Hack of Linear were selected as Innovators of the Year in EDN's 21st annual Innovation Awards. The two were selected by the readers of EDN magazine for their work in developing the LT®4180 Virtual Remote Sense™ Controller, which was also chosen by EDN as winner of the EDN Innovation Award in the Power ICs category for its innovative design, providing designers with new flexibility options in power design.

The LT4180 is a Virtual Remote Sense DC/DC controller that eliminates the remote sense wires required to compensate for the voltage drop in cables, wires and circuit board trace runs. Voltage drops in wiring and cables that cause load regulation errors are usually corrected by an additional set of sensing wires. The LT4180 continuously interrogates the line impedance and corrects the regulator's output voltage. The device maintains a corrected regulated voltage at the load regardless of current or line impedance. The 3v to 50v input voltage range address a variety of applications, including remote instrumentation, battery charging, wall adapters, notebook power, surveillance equipment and halogen lighting.

TIMERBLOX FAMILY SELECTED FOR EE TIMES ACE AWARD

Linear's TimerBlox[®] family of ICs was named winner in EE Times' Seventh Annual Creativity in Electronics (ACE) Awards for Most Popular Product of the Year in the Analog-Mixed Signal category due to its innovative design of simple, accurate timing solutions. Awards are presented in 15 categories and are judged by the editors and a blue-ribbon panel of industry experts.

Linear's TimerBlox family is a complete line of robust, tiny, accurate, low power devices that solve five common timing functions:

- voltage-controlled oscillator
- low frequency oscillator
- pulse width modulated oscillator
- monostable pulse generator (one-shot)
- delay

By combining devices, just about any timing problem can be solved easier and faster than would be possible using discrete components. For more information see www.linear.com/timerblox.

CHINA PRESS CONFERENCE

On May 27, Linear Technology CEO Lothar Maier held a press conference in Shenzhen, China with 17 assembled editors from the major technical publications in China. In his presentation, Mr. Maier gave an overview of Linear and discussed the company's strategy and commitment to the China market. In the presentation, he discussed the company's focus on three major markets:

- Industrial—including medical, security, factory automation, instrumentation and industrial control
- Communications infrastructure including cellular base stations to support worldwide growth in wireless networks, as well as networking
- Automotive electronics—including battery stack monitors for hybrid and electric vehicles, as well as LED lighting systems

Mr. Maier also discussed how Linear's high performance analog products fit into the evolving China market, with the growth of design-intensive electronics industries, including industrial, communications infrastructure and automotive markets.

CONFERENCES & EVENTS

Techno-Frontier—Power Systems Japan 2011, Tokyo Big Sight, Tokyo, Japan, July 20-22. Linear will showcase the latest power product offerings, including μModule[®] DC/DC regulators, μModule isolators, energy harvesting solutions and LTspice[®] design tools. Info at www.jma.or.jp/tf/en11/index.html.

EDN China Automotive Electronics Conference— Electric Vehicle Battery Management System Design, Shanghai Jianguo Hotel, Shanghai, China, July 28; Shenzhen Exhibition & Conference Center, Shenzhen, China, August 30. Linear will present an overview of its product offering for high performance battery management system design for electric vehicles.

DEVICE			PSE						
	STANDARD		802.3AT		LTPoE++				
TY		ТҮРЕ	TYPE 1	TYPE 2	38.7W	52.7W	70W	90W	
	802.3AT	TYPE 1	13W	13W	13W	13W	13W	13W	
		TYPE 2	13W	25.5W	25.5W	25.5W	25.5W	25.5W	
	++3	38.7W	13W	25.5W	38.7W	38.7W	38.7W	38.7W	
		52.7W	13W	25.5W		52.7W	52.7W	52.7W	
		70W	13W	25.5W	—	_	70W	70W	
PD	LTPoE++	90W	13W	25.5W				90W	

Table 1. PSE and PD power delivery matrix shows extended power levels of LTPoE++

defines Type 1 PSEs and PDs to include PSEs and PDs delivering up 13W. Type 2 PSEs and PDs deliver up to 25.5W.

LTPoE++ EVOLUTION

The IEEE POE+ 25.5W specification had not yet been finalized when it became clear that there was a significant and increasing need for more than 25.5W of delivered power. In response to this need, the LTPOE++ specification reliably allocates up to 90W of delivered power to an LTPOE++ PD.

The LTPOE++ specification provides reliable detection and classification extensions to existing IEEE POE protocols. LTPOE++ is backward compatible and interoperable with existing Type 1 and Type 2 PDs. Unlike other proprietary power-extending

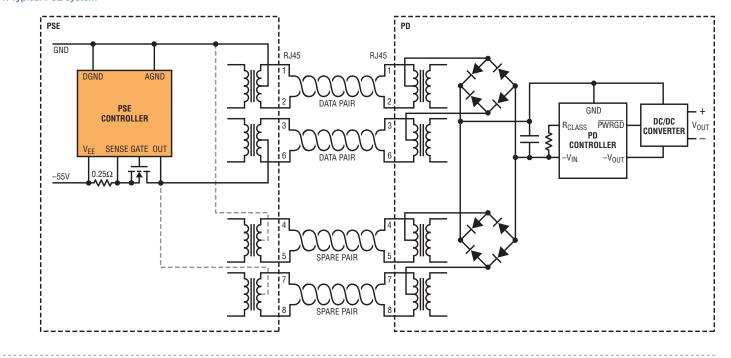


Figure 1. Typical PoE system

(LTPOE++, continued from page 1)

The IEEE standard also defines POE terminology, as shown in Figure 1. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: endpoints (typically network switches or routers), which send both data and power, and midspans, which inject power but pass data through. Midspans

are typically used to add POE capability

to existing non-POE networks. Typical

PD applications are IP phones, wireless

access points, security cameras, cellular

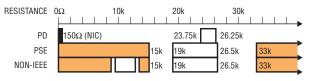
femtocells, picocells and base stations.

The IEEE POE+ specification specifies

backward compatibility with 802.3af

PSEs and PDs. The POE+ specification





solutions, Linear's LTPOE++ provides mutual identification between the PSE and PD. LTPOE++ PSEs can differentiate between an LTPOE++ PD and all other types of IEEE compliant PDs, allowing LTPOE++ PSEs to remain compliant and interoperable with existing equipment.

LTPOE++ PSEs and PDs seamlessly interoperate with IEEE 802.3at Type 1 and Type 2 devices. Type 1 PSEs generally encompass 802.3af functionality at and below 13W. Type 2 PSEs extend traditional POE to 25.5W. The following points reference Table 1:

- Type 1 PSEs will power all Type 1, Type 2 and LTPOE++ PDs with up to 13W.
- Type 2 PSEs will power Type 1 PDs with up to 13W and provide 25.5W to Type 2 and LTPOE++ PDs.
- LTPOE++ PDs can power up with limited functionality even when attached to traditional Type 1 and 2 PSEs.
- LTPOE++ PSEs interoperate with Type 1 and Type 2 PDs. LTPOE++ PDs are powered to the designed limit of the LTPOE++ PSE. When an LTPOE++ PD is identified, the PD will be powered up if the PSE power rating meets or exceeds the requested PD power. For example, a 52.7W LTPOE++ PSE can power both 38.7W and 52.7W PDs.

IEEE-COMPLIANT PD DETECTION

LTPOE++ physical detection and classification is a simple, backward-compatible extension of existing schemes. Other power extension protocols violate the IEEE specification, as shown in Figure 2, and risk powering up known noncompliant NICs. Any high Table 2. PSE vs PD vs application power

STANDARD	ТҮРЕ	PSE POWER V _{MAX}	PSE POWER V _{MIN}	PD POWER V _{MIN}	APPLICATION POWER*
	Туре 1	17.8W	15.4W	13W	11.7W
802.3AT	Туре 2	36W	34W	25.5W	23W
	Dual Type 2	72W	68W	51W	46W
	38.7W	47W	43W	38.7W	34.8W
170-5-1	52.7W	66W	63W	52.7W	47.4W
LTPoE++	70W	94W	89W	70W	63W
	90W	133W	125W	90W	81W

*Assumes DC/DC converter efficiency of 90%

power allocation scheme violating the IEEE-mandated detection resistance specifications risks damaging and destroying non-PoE Ethernet devices.

The following rules define any detection methodology for the highest levels of safety and interoperability.

- *Priority 1:* Don't turn on things you shouldn't turn on.
- *Priority 2:* Do turn on things you should.

Linear Technology PSEs provide extremely robust detection schemes utilizing fourpoint detection. False positive detections are minimized by checking for signature resistance with both forced-current and forced voltage measurements.

LTPoE++ ADVANTAGES

Standard POE PSEs use two of the four available Ethernet cable pairs for power. Some power-extending topologies use two PSEs and two PDs over one cable to deliver 2×25.5 power. This "dual Type 2" topology is shown in Figure 3. The main problem with this strategy is that it doubles the number of components, thus doubling PSE and PD costs. Additionally, robust design considerations require two DC/DC converters at the PD, one for each component PD, where each DC/DC converter is a relatively complex flyback or forward isolated supply.

One of the DC/DC converters in a dual Type 2 set-up can be eliminated by ORing the PD's output power as shown in Figure 4. This approach still requires two PSEs and two PDs, with the associated cost and space disadvantages. The voltage drop incurred by the power ORing diodes might be considered a fair trade-off for the savings gained by using a single DC/DC converter. In most cases diode ORed power sharing architectures remain attractive until surge protection testing begins. Due to intrinsic reductions in surge protection tolerance, these solutions rarely meet PD design goals. The increased power capability of LTPoE++ expands the field of ethernet-powered applications by several orders of magnitude, enabling entirely new classes of PDs, such as power-hungry picocells, base stations or even heaters for pan-tilt-zoom cameras.

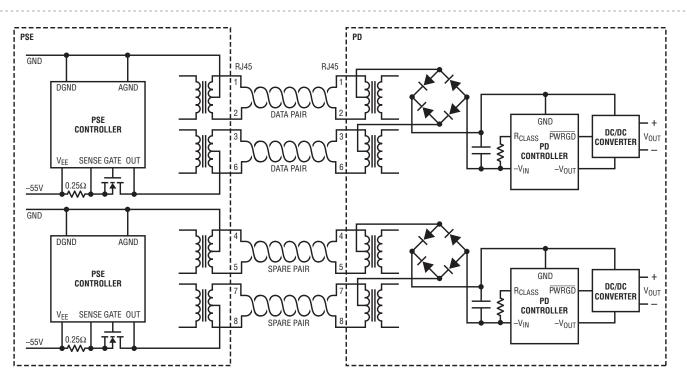


Figure 3. The expensive way to extend PoE+ power. Dual Type 2 PD provides more power than standard PoE+ PD, but it also doubles the cost and component count.

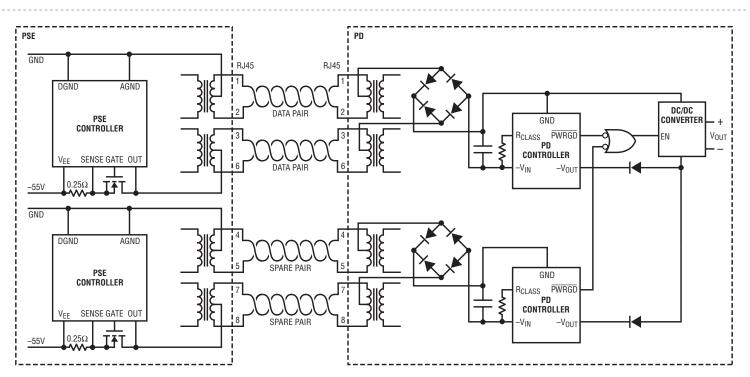
In contrast, LTPOE++ solutions, as shown in Figure 5, require only a single PSE, PD and DC/DC converter, resulting in significant board space, cost and development time advantages.

LLDP INTEROPERABILITY AND OPTIONS

During selection and architecture of a POE system, many PD designers are surprised to discover the hidden costs of Link Layer Discovery Protocol (LLDP) implementations. LLDP is the IEEEmandated PD software-level power negotiation. LLDP requires extensions to standard Ethernet stacks and can represent a significant software development effort. Unfortunately the open-source community effort to provide LLDP support is still in its infancy.

While Type 2 PSEs may optionally implement LLDP, fully IEEE-compliant Type 2 PDs must implement both physical classification and LLDP power negotiation capabilities. First, this places the burden of LLDP software development on all Type 2 PDs. In addition, designs are complicated by the dual power requirements inferred by the LLDP requirement. Specifically, the PD-side processor must be fully functional at the 13W power level and then have the ability to negotiate, via LLDP, for the delivery of additional power. Clearly this requirement can increase development and system costs and complexity.

LTPOE++ offers LLDP implementation options. LTPOE++ PSEs and PDs autonomously negotiate power level requirements and capabilities at the hardware level while remaining fully compatible with LLDP-based solutions. In short, LTPOE++ gives system designers the choice to implement or not implement LLDP. Proprietary end-to-end systems may choose to forgo LLDP support. This creates time-to-market advantages while further reducing BOM costs, board size and complexity.



Linear Technology is committed to LTPoE++ technology and provides an entire family of PSE and PD solutions. A full family of PSEs, spanning 1- to 12-port solutions is now available.

Figure 4. Less expensive, but flawed, alternative for extending PoE+ power. This scheme is similar to the dual Type 2 set-up shown in Figure 3, but a diode ORed power sharing architecture reduces some of the cost by eliminating one DC/DC converter in the PD. However, due to intrinsic reductions in surge protection tolerance, these solutions rarely meet PD design goals.

POWER CLAIMS DEMYSTIFIED POE power paths can be divided into three main components: the power produced by the PSE, the power delivered to the PD and the power delivered to the application. Claims of PSE and PD power delivery capabilities must be carefully examined before useful comparisons can be made. One vendor may describe the power as delivered by the PSE, another the power delivered to the PD, while the PD designer typically cares about power consumed by the application.

Although the PSE power metric is the least useful of the three, it is the one most often cited in marketing materials. PSE power is generally defined as the power delivered at the PSE end of the Ethernet cable. Power capability is sometimes further distorted when vendors specify power at the maximum rated voltage, which is rarely achieved.

PD power or "delivered power" is the power delivered to the PD end of the Ethernet cable, prior to the diode bridge. Quoted PD power is a more useful metric than PSE power, since it must account for significant losses over 100 meters of CAT-5e cable. PD power claims make no assumptions about the application's DC/DC converter and diode bridge efficiencies, which are unknown to PSE and PD silicon vendors.

A PD designer is most interested in the power delivered to the application when all system effects are considered, including the resistance of the Ethernet magnetics, diode bridge voltage drops and DC/DC converter efficiency. This metric, while the most telling, is the most difficult to accurately specify.

Table 2 shows actual performance comparisons at all stages of the power path. Note that the dual Type 2 configuration delivers far less power than the LTPOE++ 70W and 90W solutions. LTPoE++ offers a robust, end-to-end high power PoE solution with up-front cost savings. Combined with Linear Technology's excellent application support, proven delivery record and reputation for reliability, LTPoE++ is the most comprehensive high power solution on the market.

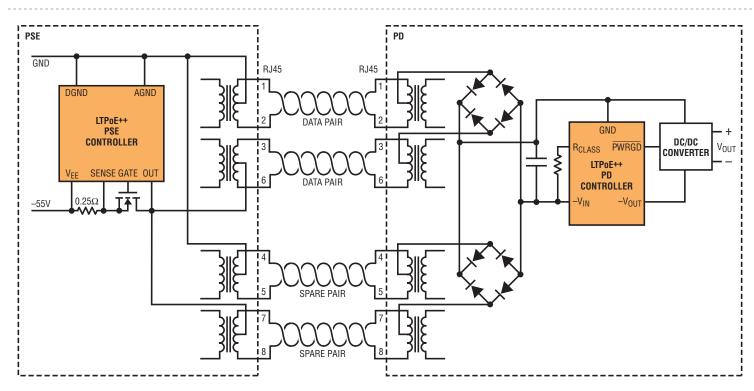


Figure 5. The LTPoE++ architecture is the only PoE power-extending solution that provides 90W at the PD while keeping complexity and costs in check.

PSE AVAILABILITY

Linear Technology is committed to LTPOE++ technology and provides an entire family of PSE and PD solutions. A full family of PSEs, spanning 1- to 12-port solutions is now available, shown in Table 3.

CONCLUSION

LTPOE++ offers a robust, end-to-end high power POE solution with up-front cost savings. Combined with Linear Technology's excellent application support, proven delivery record and reputation for reliability, LTPOE++ is the most comprehensive high power solution on the market. LTPOE++ systems simplify power delivery and allow system designers to concentrate their design efforts on their high value applications.

PSE PART	# PORTS	DELIVERED PD POWER (MAX)
LTC4274A-1	1	38.7W
LTC4274A-2	1	52.7W
LTC4274A-3	1	70W
LTC4274A-4	1	90W
LTC4266A-1	4	38.7W
LTC4266A-2	4	52.7W
LTC4266A-3	4	70W
LTC4266A-4	4	90W
LTC4270A	12	38.7W-90W (pin selected)

Table 3. LTPoE++ PSEs

Two Wide Input Range Monolithic Switching Regulators Make it Easy to Fit Boost, Flyback, SEPIC and Inverting Topologies into Tight Spaces

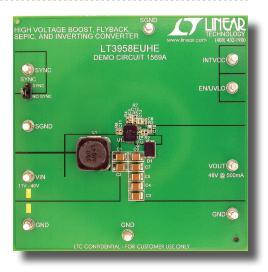
Bin Zhang

The LT3957 and LT3958 are high power monolithic switching regulators that can generate a positive or a negative output from a wide range of input voltages. The LT3957 operates over an input range of 3V to 40V, making it suitable for everything from portable electronics to automotive and industrial applications. The LT3958 extends the input voltage to 80V for high voltage telecommunications supplies. Both produce high power from a small footprint as shown by the boost converter layout in Figure 1.

These versatile switching regulators can be configured as boost, flyback, SEPIC or inverting converters. The LT3957 and LT3958 feature a rugged low side N-channel power MOSFET rated for 5A/40V and 3.5A/80V respectively. A novel FBX pin architecture provides accurate regulated positive or negative output with a simple resistor divider. These ICs also include soft-start, frequency foldback, input undervoltage lockout, adjustable frequency and synchronous switching.

FEATURES

By integrating the power MOSFET and LDO onto the die, the LT3957 and LT3958 simplify converter design, shrink the solution size and reduce cost when compared to non-monolithic solutions. The LT3957 has an integrated 40V/30mΩ N-MOSFET switch with an internally programmed current limit of 5.9A (typical). The LT3958 has an integrated 84V/90mΩ N-MOSFET switch with an internally programmed current limit of 4A (typical). Each IC has an internal high voltage LDO, which allows LT3957





to be powered from a supply as high as 40v, and for LT3958 as high as 80v.

The LT3957 and LT3958 use a constant frequency, peak current mode control scheme, providing fast transient response and an easy to stabilize feedback loop at variable inputs and outputs. The switching frequency can be programmed over a 100kHz to 1MHz range with a single

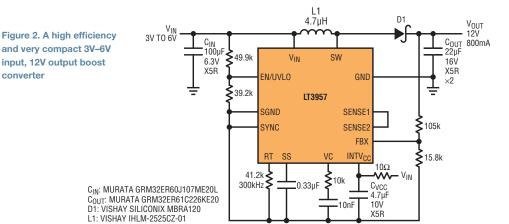
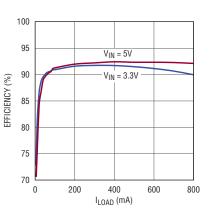


Figure 3. Efficiency of the converter in Figure 2



The LT3957 and LT3958 feature a rugged low side N-channel power MOSFET rated for 5A/40V and 3.5A/80V respectively. A novel FBX pin architecture provides accurate regulated positive or negative output with a simple resistor divider.

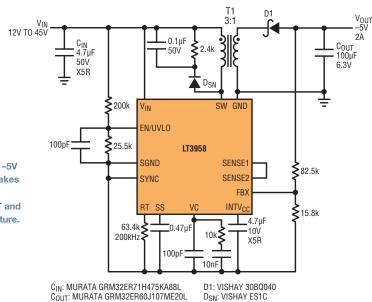


Figure 4. A simple and compact 12V to 45V input, -5V output flyback converter takes advantage of the LT3958's rugged 84V-rated MOSFET and the novel FBX pin architecture.

D_{SN}: VISHAY ES1C T1: COILTRONICS VP2-0066

external resistor, which allows designers to optimize component size and performance parameters, such as minimum/ maximum duty cycle and efficiency.

At the heart of each of the LT3957 and LT3958 is a pair of feedback error amplifiers: one regulates a positive output and the other, a negative output. When the converter starts up, the output voltage ramps positive or negative depending on the topology selected. The appropriate error amplifier seamlessly takes over the feedback control, while the other becomes inactive. In this way, these parts can automatically regulate to the desired output voltage in different converter topologies.

The LT3957 and LT3958 contain several features to limit the peak switch currents and output voltage overshoot during start-up or recovery from a fault condition. The ss pin voltage modulates the peak switch current, thereby allowing the output capacitor to charge gradually toward its final value while preventing switch current from reaching current limit. Selection of a capacitor on the ss pin determines the start-up/restart time. The frequency foldback function reduces the switching frequency when FBX voltage is close to ov to ensure that the IC maintains control over the switch current. An overvoltage protection function protects both the positive and negative output converters from excessive output voltage overshoot. The internal power switch is turned off immediately when the FBX pin voltage exceeds the positive regulated voltage by 8% (typical), or negative regulated voltage by 11% (typical).

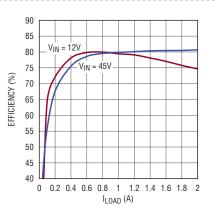


Figure 5. Efficiency of the converter in Figure 4

A 3V-6V INPUT, 12V OUTPUT **BOOST CONVERTER**

Figure 2 shows a 3V–6V input, 12V output boost power supply using the LT3957. To ensure the 3v minimum operation voltage, the voltage drop across the internal LDO is eliminated by connecting the INTV_{CC} pin directly to V_{IN} pin through a 10 Ω resistor (given that the maximum v_{IN} operating voltage of 6v is below INTV_{CC}'s maximum voltage rating of 8v). Figure 3 shows the efficiency of this converter.

A 12V-45V INPUT, -5V OUTPUT FLYBACK CONVERTER

The LT3957 or LT3958 can be configured as a flyback converter for applications where the converters have multiple outputs, isolated outputs or high input/output voltage conversion ratios. The flyback converter has a very low parts count for multiple outputs, and with prudent selection of transformer turns ratio it can have high output/input voltage conversion ratios with a desirable duty cycle.

The frequency foldback feature of the LT3957 and LT3958 provides robust

design features

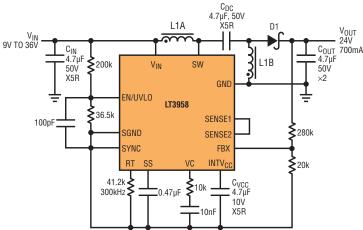


Figure 6. A simple and compact 9V-36V input, 24V output SEPIC converter with short-circuit protection

CIN, COUT, CDC: MURATA GRM32ER71H475KA88L D1: VISHAY 10BQ100 L1A, L1B: COILTRONICS DRQ127-330

output short-circuit protection. Each IC's FBX feature allows the flyback converter to easily produce either positive or negative outputs. Figure 4 shows a LT3958 in a flyback converter that operates from a 12v to 45V input and delivers 2A to a -5V output. Figure 5 shows the efficiency of this converter at different input voltages.

A 9V–36V INPUT, 24V OUTPUT SEPIC CONVERTER

Figure 6 shows the LT3958 in a 9V to 36V input, 24V output SEPIC converter. This topology allows for the input to be higher, equal or lower than the desired output voltage. In a SEPIC converter, no DC path exists between the input and output, which is an advantage for applications requiring the output to be disconnected from the input source when the circuit is shut down. This design can sustain an indefinite output short-circuit condition due to its topology and the frequency foldback feature. Figure 7 shows the efficiency of this converter at different input voltages.

A 4V–15V INPUT, –5V OUTPUT INVERTING CONVERTER

An inverting converter is similar to the SEPIC converter in that it can step up or step down the input, but with a negative output. It also offers output disconnect and short-circuit protection. Figure 8 shows a 4v-15v input, -5v output inverting

100 95 $V_{IN} = 24V$ $V_{IN} = 9V$ 90 V_{IN} = 36V 85 EFFICIENCY (%) 80 75 70 65 60 55 50 700 100 200 300 400 500 600 0 ILOAD (mA)

Figure 7. Efficiency of the converter in Figure 6.

converter using LT3957 as the switching regulator. Figure 9 shows the efficiency of this converter at different input voltages.

CONCLUSION

The LT3957 and LT3958 are versatile monolithic switching regulators that can be configured as boost, flyback, SEPIC or inverting converters accepting a wide range of input voltages. By integrating the power MOSFET and LDO, they greatly simplify converter design, shrink solution size and reduce costs. These ICs also offer low shutdown current, soft-start, frequency foldback, input UVLO, adjustable frequency and synchronization. The combination of these features makes the LT3957 and LT3958 suitable for a variety of applications ranging from battery portable electronics to automotive, industrial and telecommunications power supplies.

Figure 9. Efficiency of the converter in Figure 8

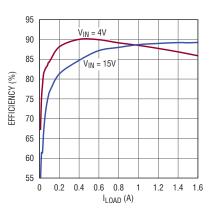
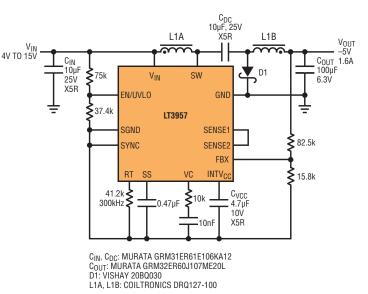


Figure 8. A simple and compact 4V–15V input, –5V output inverting converter with shortcircuit protection



Multiprotocol Transceivers Combine RS485 and RS232 in a Single Device to Simplify and Shrink Applications that Use Both Standards

Steven Tanghe

The RS232 and RS485¹ data transmission interface standards are in widespread use today despite their relatively advanced age—RS232 was introduced almost 50 years ago; RS485, 30 years ago. Such longevity for any standard is uncommon in today's rapidly changing electronics landscape, where consumer demand can force obsolescence in a handful of years.

Although the once ubiquitous RS232 port on personal computers has largely been replaced by USB, RS232 continues to proliferate in applications requiring rugged, short distance, point-to-point communication, such as in sensors, test equipment, device programming and diagnostics.

Likewise, RS485 thrives thanks to its high performance in harsh environments. Its differential signaling scheme and wide common mode tolerance provide excellent noise immunity, allowing high speed communication over relatively long distances. Perhaps equally important in the RS485 standard is the ability to network several devices on a single bus, thereby reducing wiring overhead. RS485 is specified as the physical layer for many Fieldbus networks including PROFIBUS and INTERBUS.

To simplify the design of R\$485 and R\$232 systems, the LTC2870 and LTC2871 multiprotocol transceivers combine both types of transceivers on a single device. Both support data rates as high as 20Mbps for the single R\$485 transceiver and 500kbps for two R\$232 transceivers.

These devices are designed to support a wide variety of applications with features that make them flexible and robust:

- They accept a wide range of input supply voltages from 3v to 5.5v, as well as a logic supply pin, allowing a digital interface down to 1.7v with no level translation needed.
- Integrated termination resistors are automatically engaged for compatibility with Rs232 or Rs485 operation.
- Half- and full-duplex control and loopback functions provide system configurability and diagnostics capability.
- Robust performance allows continuous operation during ESD strikes of up to 26kV on the bus pins.
- Both devices are offered in small QFN and TSSOP packages, as shown in Figure 1.

The LTC2870 and LTC2871 differ in how their transceiver I/Os are pinned out, as well how they are controlled. The LTC2870 offers two RS232 transceivers that share I/O pins with an RS485 transceiver. It can operate in either RS232 mode or RS485 mode but not both at once. The LTC2871 provides additional flexibility by pinning the RS485 and RS232 transceivers out separately so that all transceivers

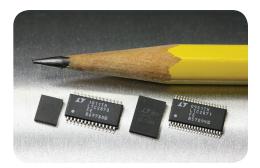


Figure 1. The LTC2870 and LTC2871 are offered in small QFN and TSSOP packages

can be operated concurrently as shown in Table 1. Figure 2 shows a simplified block diagram for each device.

APPLICATIONS

The LTC2870 and LTC2871 can be configured in a variety of ways. Application of these devices falls into three main categories:

- *Fixed interface:* The LTC2870 or the LTC2871 can be permanently configured as either an RS232 or RS485 interface. For instance, Figure 3 shows both modes of operation for the LTC2870. If two versions of a product are offered, one with each interface, a multiprotocol transceiver minimizes design differences, reducing inventory, and simplifying product qualification.
- *In situ configuration changes with a shared connector:* Some applications require the signaling interface to change between Rs232 and Rs485 during normal product usage. For example, a node in an alarm system might be networked with other nodes via an Rs485 communication bus. However, the node can be configured for local Rs232 access,

Table 1. Product selection guide

PART NUMBER	CONFIGURABLE TRANSCEIVER COMBINATIONS (RS485 + RS232)	PACKAGES
LTC2870	(0 + 0), (1 + 0), (0 + 2)	28-Lead QFN, 28-Lead TSSOP
LTC2871	(0 + 0), (1 + 0), (1 + 1), (1 + 2), (0 + 1), (0 + 2)	38-Lead QFN, 38-Lead TSSOP

allowing programming or diagnostics. Signaling pins are shared between the Rs485 and the Rs232 transceivers, with one transceiver active at any given time, as shown in Figure 4. The LTC2870 changes modes between Rs232 and RS485 via control of the $485/\overline{232}$ pin, which can be manipulated though processor control, manual jumper settings, or protocol-specific cables that connect the pin to V_L or ground. The LTC2871 can be

used in a similar way but with independent access to all signal pins.

• *Simultaneous operation*. Some applications require concurrent Rs485 and Rs232 communication. For example, in point-of-sale applications, a cash register may communicate with a server

Figure 2. Simplified block diagrams of the LTC2870 and the LTC2871

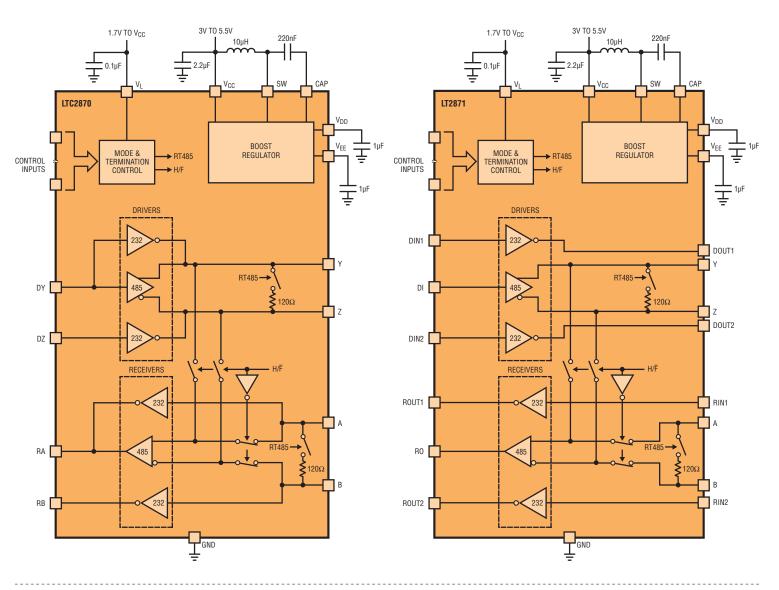
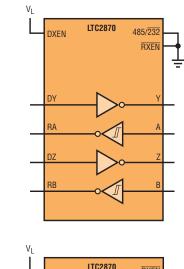


Figure 3. The LTC2870 configured for RS232 (a) or RS485 (b) communications. The RS485 configuration also shows the RS485 termination resistors optionally switched in with the TE485 pin tied high.

via RS485 but also accept input from an RS232-equipped keypad. The LTC2871, with completely independent RS232 and RS485 transceivers, enables separate terminals for each protocol with a single IC. Another example of simultaneous usage is translation between RS232 and RS485 protocols. Figure 5 shows the LTC2871 configured as an RS232 4000-foot "extension cord" implemented by converting to RS485 for the long cable run and converting back to RS232 at the ends.

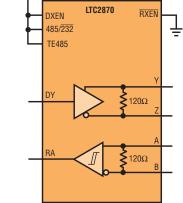
THE WHOLE IS BETTER THAN THE SUM OF ITS PARTS

Using a multiprotocol device, such as the LTC2870 with shared RS485 and RS232 interface pins, offers a number of advantages over simply combining standalone RS485 and RS232 transceivers. First, by combining the function of both transceivers in one device, the overall footprint on a circuit board is reduced. Second, all of the interface pins on the RS232 can tolerate inputs to ±15V. Most RS485 devices can only tolerate -7 to 12V, so connecting such a device to RS232 pins would lower the shared pin rating.

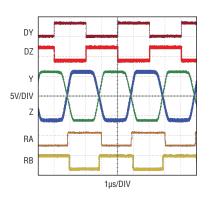


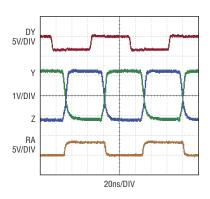
а

b



Perhaps the biggest obstacle in combining individual R\$485 and R\$232 transceivers concerns the termination resistors used in each signaling standard. This situation is illustrated in Figure 6, where two different devices are connected to the same bus. The input resistance of the R\$232 receivers is specified to be 5k (nominally), which acts as a termination resistor for an R\$232 driver connected to it. On the other hand, the differential R\$485 receiver can be terminated with 120Ω resistors across its





inputs if it is located at the end of the signaling bus, to reduce signal reflections. The challenge is in switching out the resistors that are not needed in the selected transceiver mode. For example, in R\$485 mode, the 5k resistors should not be present and likewise, in R\$232 mode, the 120Ω differential termination must not be present.

The LTC2870 and LTC2871 seamlessly switch between termination schemes as needed, using internal components.

Table 2. Termination control in the LTC2870. The LTC2870 and LTC2871 seamlessly switch between termination schemes as needed, using internal components. The RS485 120Ω termination resistor can be disabled in any mode by setting TE485 pin low, which is useful if the transceiver is not positioned at the end of the bus.

INPUTS			RESULTING TERMINATION				
485/232	TE485	RXEN	120Ω: A TO B, Y TO Z	5k: A TO GND, B TO GND	MODE		
1	0	Х	No	No	RS485 Mode Without Termination		
1	1	Х	Yes	No	RS485 Mode With Termination		
0	Х	0	No	Yes	RS232 Mode, Receiver Enabled		
0	Х	1	No	No	RS232 Mode, Receiver Disabled		

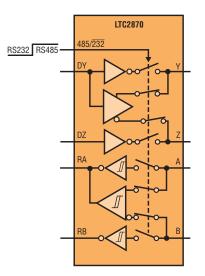
design features

There is no need for external termination components or relays to control them. Furthermore, the RS485 120 Ω termination resistor can be disabled in any mode by setting TE485 pin low, which is useful if the transceiver is not positioned at the end of the bus. Table 2 summarizes the termination control in the LTC2870.

The LTC2871 offers similar controls but since the RS232 and RS485 pins are not shared, all of the termination resistors can be engaged simultaneously if desired. Refer to the data sheet for details.

SOME SPECIFICS REGARDING THE **RS485 TERMINATION RESISTOR** RS485 communicates differentially over a bus containing one or more pairs of twisted wires. If the transition time of the signal driven into the bus is significantly less than the round trip delay to the load and back, then the bus needs to be terminated differentially with a resistor whose characteristic impedance matches that of the bus. This termination should be placed at the receiver end of the bus or both ends of the bus, but not in between. The absence of termination or improper termination introduces reflections that can cause severe waveform distortion.²

When RS485 termination is enabled on the LTC2870 or LTC2871, the 120Ω differential resistors are connected across receiver inputs A and B and also across



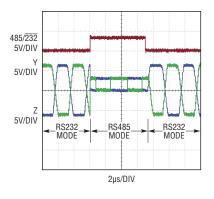


Figure 4. LTC2870 protocol switching, using the 485/232 pin. Oscilloscope traces show the driver outputs toggling data during mode changes.

driver outputs Y and Z. The driver termination is not strictly necessary for the case when this device is actively driving the bus, such as the master in Figure 7. However, the Y to Z termination is necessary in applications such as the slave at the far end of the bus in Figure 7, where another device is driving the bus.

The RS485 standard specifies cable with a characteristic impedance of 120Ω while RS422 specifies 100Ω cable. These cables generally contain one or more twisted pairs as well as ground shields or a ground wire (sometimes called a drain wire). As an alternative to shielded twisted pair, unshielded 100Ω Category 5 (CAT5) cabling is increasingly applied in RS485 and RS422 systems as an economic alternative. The LTC2870 and LTC2871 perform equally well with 100Ω or 120Ω cable. Even when the internal termination resistor, nominally 120Ω , is used to terminate a 100Ω cable, the impedance mismatch has negligible impact on the resulting signal. For instance, the effect of using a 120Ω termination on each end of a 100Ω cable is to develop an overshoot of about 10% at the receiver end with a duration equal to

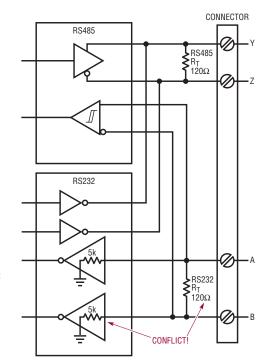


Figure 6. Termination resistors pose challenges when separate RS232 and RS485 transceivers are used in combination.

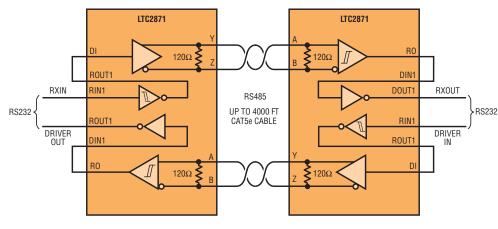
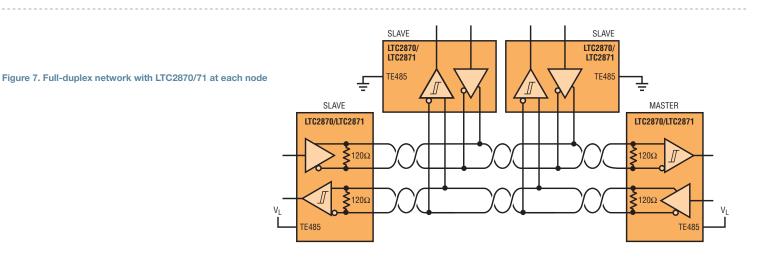


Figure 5. RS232 "Extension cord" using the LTC2871's simultaneous RS232 and RS485 communication mode

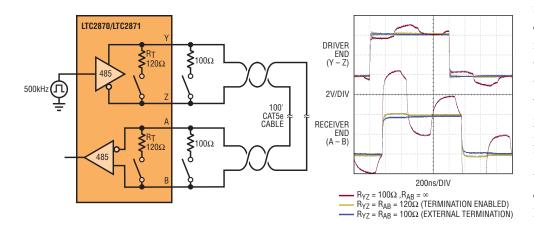
The only required external components are one 10μ H inductor for the boost voltage and one 220nF cap for the voltage inversion, as well as the bypass caps on the generated V_{DD} and V_{EE} rails.



twice the one-way propagation delay in the cable. This small deviation from ideal is easily tolerated in most communications systems, and can improve performance, which is why the PROFIBUS standard specifies a similar termination mismatch.

Figure 8 shows the results of using the LTC2871 internal 120Ω termination resistor to terminate 100 feet of CAT5e cable

compared to the same cable terminated with 100Ω . Although the internal terminator is not a perfect match for the 100Ω cable, there is almost no effect on the overall signal other than a slight amplitude increase at the beginning of the received signal, which can improve system performance via increased signal overdrive and noise margin. Normal





cable variation, stub reflections and discontinuities have a far greater impact on signal integrity. The figure also shows the devastating effect of leaving the cable unterminated at the receiving end, where reflections degrade the signal substantially.

INTERNAL RS232 SUPPLY ENOUGH TO DRIVE TWO TRANSCEIVERS RS232 signals are driven on a single wire with respect to ground at levels that must exceed 5v and -5v. A DC/DC boost converter and capacitive inverter are integrated into the LTC2870 and LTC2871 to produce both positive and negative voltages used to support these drive levels while operating on a single 3V-5.5V supply. The only required external components are one 10µH inductor for the boost voltage and one 220nF cap for the voltage inversion, as well as the bypass caps on the generated v_{DD} and v_{EE} rails. Figure 9 shows the LTC2870 or LTC2871 configured in a typical application with all of the required external components.

Predictable fault handling is important for robust system design. LTC2870 and LTC2871 receivers produce a high output, called a failsafe condition, in response to an idle bus, disconnected bus or shorted bus.

3V TO 5.5V 470nF 22µH 2.2u CAF CAF SW Vcc LTC2870/ LTC2870/ V LTC2871 LTC2871 SV GND GND Figure 10. Running two LTC2870s or LTC2871s 2.2µF 2.2µF Ι

INDUCTOR: TAIYO YUDEN CBC2518T220M OR MURATA LQH32CN220K53

Many modern RS485 receivers meet failsafe requirements by introducing a negative offset into the differential threshold. In this way, whenever the bus is shorted or undriven, but terminated, the input to the receiver is zero, which is interpreted as a high level. The receiver in this case is unbalanced, since the threshold is not symmetric around zero volts-the average of a differential signal.

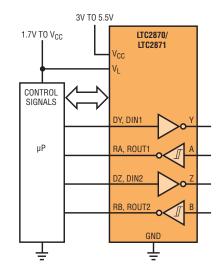


Figure 11. The V_L pin permits low voltage logic interface

Two LTC2870 or LTC2871 devices can be powered simultaneously from the internal DC/DC converter of one device, reducing the number of external components. Figure 10 shows two LTC2870s, two LTC2871s or one of each sharing a single internal RS232 supply.

LOGIC SUPPLY PIN SUPPORTS 1.7V **TO 5.5V SUPPLIES**

A separate logic supply pin v_L allows the LTC2870 and LTC2871 to interface with any logic signals from 1.7V to 5.5V. All logic I/Os use v_L as their high supply. Optionally, v_L can be tied to v_{CC} . Figure 11 shows the LTC2870 or LTC2871 used with a low voltage microprocessor.

RS485 BALANCED RECEIVER AND FAILSAFE

Failsafe operation is a term used to describe how a receiver reacts to various conditions, most of which are faults. Predictable fault handling is important for robust system design. LTC2870 and LTC2871 receivers produce a high output, called a failsafe condition, in response to all of the following conditions:

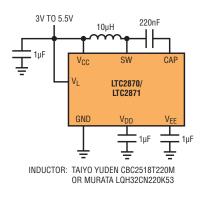


Figure 9. Typical supply connections with external components shown

• Idle Bus. All drivers on the bus are disabled with high impedance outputs. This condition is not actually a fault; it is a normal mode of operation in RS485. Some receivers cannot support this by themselves but require a resistor network to bias the differential signals on the bus in such a way that the receiver senses it as a high input. The LTC2870 and LTC2871 support this function without requiring a bus-biasing network, whether the bus is terminated or not.

from a single, shared DC/DC converter

- Disconnected Bus. This category of failsafe operation refers to the case where the receiver becomes disconnected from the bus. This is similar to the idle bus state but is truly a fault condition. Receivers that rely on bus biasing resistors to handle an idle bus condition do not respond properly to this type of fault.
- Shorted Bus. In this situation, the receiver inputs are shorted together. Some receivers provide failsafe operation for open, but not shorted, inputs. Again, bus-biasing resistors are not effective for shorted bus conditions.

100 Ω unshielded Category 5 (CAT5) cabling is used with RS485 and RS422 systems as an economic alternative to specialized shielded twisted pair cabling. With this in mind, the LTC2870 and LTC2871 perform equally well with 100 Ω cable or 120 Ω cable. Even when the internal 120 Ω termination resistor is used to terminate a 100 Ω cable, the resulting signals are not degraded.

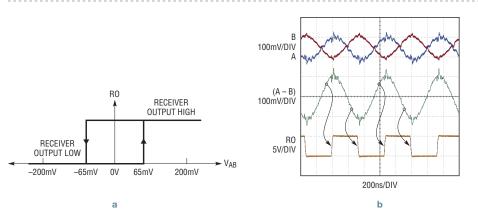
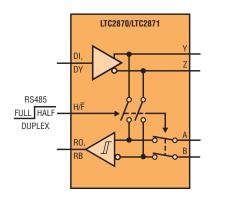


Figure 12. (a) RS485 receiver input threshold characteristics for fast moving signals. (b) Measured 3Mbps signal driven down 4000ft of CAT5e cable. Top Traces: receiver signals after transmission through cable; Middle Trace: math showing the differences of the top two signals; Bottom Trace: receiver output, exhibiting excellent duty cycle.

The unbalanced receiver can introduce severe signal pulse-width and duty-cycle distortion for weak signals that result from transmission over long cables.

The LTC2870 and LTC2871 use a balanced receiver with a rising threshold of 65mV and a falling threshold of -65mV for signals transitioning through that window in less than 2µs, as shown in Figure 12. If the differential signal lingers within this window for more than 2µs, the positive

Figure 13. RS485 full- and half-duplex control in the LTC2870



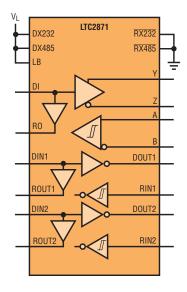
threshold drops down to -40mV to support all modes of failsafe operation, as previously described. The balanced receiver architecture permits transmission over longer cables than an unbalanced receiver and offers the additional benefit of excellent noise immunity due to the wide effective differential input signal hysteresis of 130mV for typical communications

Figure 12 highlights the performance of the LTC2871 balanced receiver, where a signal is driven through 4000 feet of CAT5e cable at 3Mbps. Even though the differential signal peaks at just over ±100mV with slow edges, the output maintains nearly a perfect signal and the receiver introduces almost no duty cycle distortion.

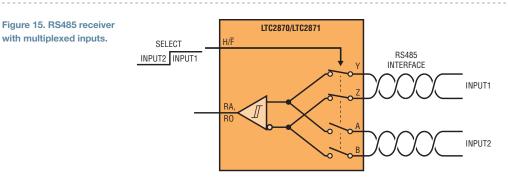
DUPLEX AND LOOPBACK CONTROL RS485 networks can be wired in a 2-wire, half-duplex configuration or a 4-wire, fullduplex configuration. In some systems the interface may need to support both. The LTC2870 and LTC2871 offer on-the-fly flexibility via the H/F pin. When the H/F control is low, the device is in full-duplex mode, with the driver outputs on the Y and Z pins and the receiver inputs on the A and B pins. If the H/F pin is high, the R\$485 transceiver enters half duplex mode where the receiver takes its inputs from the Y and Z pins. This works seamlessly with the termination control and has no effect on R\$232 operation. Figure 13 shows the simplified block diagram illustrating this flexibility.

The LTC2870 and LTC2872 also feature a logic loopback feature that can be used for diagnostics and as a debug tool. The loopback mode works for both the RS232 and RS485 transceivers, and provides a logic path from the driver input pin to the corresponding receiver output pin. The driver and receiver are not engaged in the loop; just logic buffers are used. This allows diagnostic tests to be run

Figure 14. Logic loopback control in the LTC2871. Loopback works whether or not the drivers are enabled.



The LTC2870 and LTC2871 multiprotocol transceivers simplify the design of RS485 and RS232 systems by combining both types of transceivers on a single device. They support data rates as high as 20Mbps for the single RS485 transceiver and 500kbps for two RS232 transceivers.



without disturbing the bus. Optionally, the bus may be driven during loopback by simply enabling the appropriate driver. Figure 14 shows loopback operation.

MORE APPLICATIONS

The rich feature sets of the LTC2870 and LTC2871 make it possible to build applications that would otherwise be challenging to produce. For example,

Figure 16. RS232 triple transceiver with

selectable line interface (a), and logic

interface (b)

Figure 15 shows an RS485 receiver with multiplexed inputs making use of the half- and full-duplex control.

Figure 16 shows how to combine two LTC2871 devices to make a triple RS232 transceiver with either a selectable line or logic interface. This application makes use of the $\overline{CH2}$ pin, which selectively disables the second RS232 transceiver.

When disabled, the driver and receiver outputs are not driven and the receiver input becomes high-z. This allows these pins to be connected to the same pins on another device whose CH2 pin is driven with the complementary state of the first.

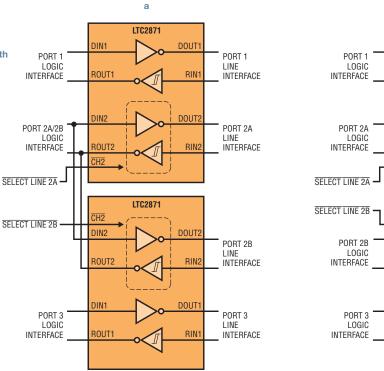
CONCLUSION

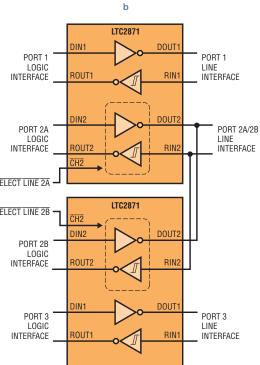
The LTC2870 and LTC2871 are flexible 3V to 5.5V multiprotocol transceivers that communicate using RS485 and RS232 signaling on either shared I/O pins (LTC2870) or separate I/O pins (LTC2871). Integrated selectable termination and duplex control allow easy configuration with minimal external components.

Notes

1 Formally, TIA/EIA-485 and TIA/EIA-232

2 "Rugged 3.3V RS485/RS422 Transceivers with Integrated Switchable Termination," by S. Tanghe, R. Schuler, *LT Magazine*, March 2007.





Step-Down DC/DC Controller in 2mm × 3mm DFN Includes FET Drivers, DCR Sensing and Accepts Inputs to 38V

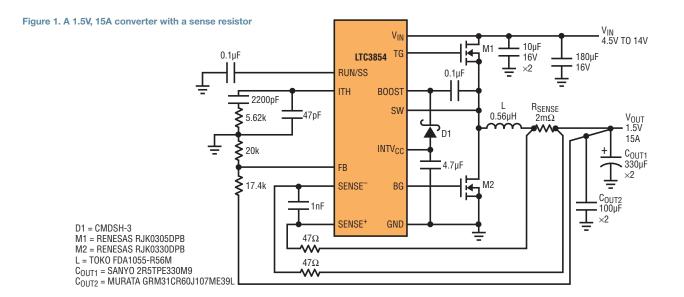
Mike Shriver

Wide input voltage range and reliability are desirable features in any buck converter. The LTC3854 delivers these features and more in a 2mm × 3mm DFN or MSE package. This current mode controller with integrated N-channel FET gate drivers can produce output voltages ranging from 0.8V to 5.5V over an input voltage range of 4.5V to 38V.

SENSING THE CURRENT

The LTC3854 employs a fixed frequency peak current mode topology, which provides a cycle-by-cycle current limit. Current can be sensed with discrete sense resistors in series with the inductor. Alternately, the DC resistance of the inductor (DCR) can be used to sense current instead of a sense resistor by placing an RC filter across the inductor to recreate the triangular current sense waveform. The advantage of DCR sensing is improved efficiency (thanks to the elimination of the power losses of the sense resistor), lower parts count and lower cost. The disadvantage is a less accurate current limit due to DCR variations part-to-part and over temperature.

Figure 1 shows a 1.5V, 15A converter that uses a sense resistor to sense the output current; Figure 2 shows the same circuit, but with DCR sensing. The full load efficiency of the circuit with a sense resistor is 86.9%, while the full load efficiency increases to 88.7% (see Figure 3) with DCR sensing. The 400kHz switching frequency provides a good balance between high efficiency on one hand and a fast load step response on the other. The load step response shown in Figure 4 shows that the output voltage remains within \pm 50mV for a 50%-to-100% load step.



The wide input voltage range of the LTC3854 allows it to be used in a wide variety of applications, including automotive, industrial and communications.

WIDE INPUT VOLTAGE RANGE **APPLICATIONS**

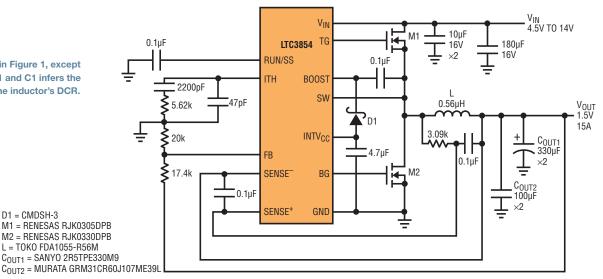
The input voltage range of the LTC3854 allows it to be used in a wide variety of applications, including automotive, industrial and communications. One example of a wide input converter is the 5V, 10A converter in Figure 5, which can be used for

an input voltage range of 6v to 38v. The strong gate drivers and low QG FETs allows for 94% efficiency at a 32v input voltage and 100% load as shown in Figure 6.

The small size and low pin count of the LTC3854 allows the control section of the 2.5V/5A converter with a 4.5V to 26V input

Figure 2.

voltage range shown in Figure 7 to fit within a 180mm² area. Dual channel FETs are used to minimize the size of the power stage. The 400kHz switching frequency allows the use of a small 2.2µH inductor with a 7mm × 7mm footprint. The entire converter (minus the bulk input capacitor) can fit in a 430mm² area.





92

90

88

84

82

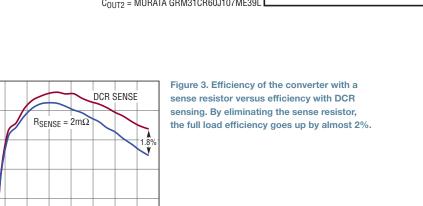
80

2 0

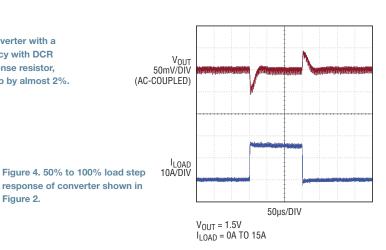
4 6 8 10 12 14 16

 I_{LOAD} (A)

EFFICIENCY (%) 86



 $V_{IN} = 12V$



V_{IN} 6V TO 38V VIN 150µF 0.1µF LTC3854 TG 4711F 50V 50V ×2 RUN/SS 0.1µF ITH BOOST 2200pF R_{SENSE} **₹**7.5k SW 100pF 3.6µH 3mΩ VOUT 5Ŭ **7**D1 10A INTVCC 8.06k C_{OUT1} 4 7uF 220µF FB M2 ξ 42.2k SENSE BG K 4.7nF SENSE⁺ GND 16Ω $\mathbf{\mathcal{N}}$ 16Ω Ś

Figure 5. 5V, 10A converter with a 6V to 38V input voltage range

D1 = ZETEX ZLLS1000 M1, M2 = INFINEON BSC093N04LS L = COILTRONICS HC1-3R6-R C_{OUT1} = SANYO 6TPE220MI

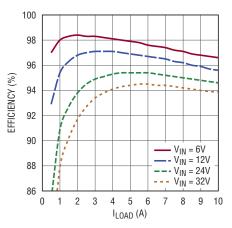


Figure 6. Efficiency of the 5V, 10A converter

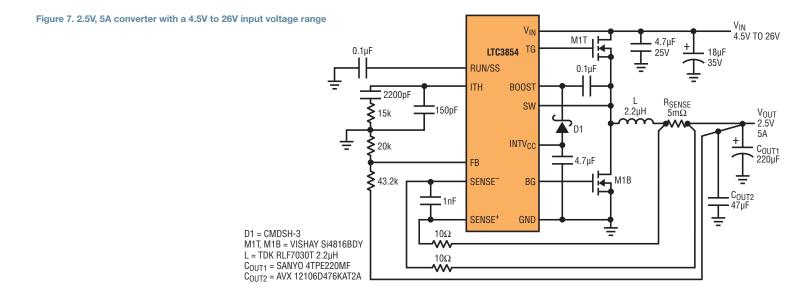
SOFT-START, LOW DROPOUT AND **HIGH STEP-DOWN RATIOS**

The LTC3854 features a programmable soft-start set with a capacitor on the RUN/SS pin. As the output voltage ramps up, the converter operates in discontinuous mode to prevent reverse current from flowing into the inductor. This allows the part to safely turn on into a prebiased output. After ramp-up, the part operates

in continuous conduction mode. Other features are a maximum duty cycle of 97% for low dropout voltage applications, a low minimum on-time of 75ns for applications with high step-down ratios, foldback current limit in addition to the cycle-by-cycle current limit and a built-in 5v linear regulator for bias.

CONCLUSION

The LTC3854 delivers reliability and efficiency for cost-sensitive and space-constrained applications. The device can produce output voltages ranging from 0.8v to 5.5v over an input voltage range of 4.5v to 38v. The LTC3854's 2mm × 3mm DFN and MSE packages, along with a 400kHz switching frequency, minimize solution size.



No Blocking Diode Needed to Protect Sensitive Circuits from Overvoltage and Reverse Supply Connections

Victor Fleury

What would happen if someone connected 24V to your 12V circuits? If the power and ground lines were inadvertently reversed, would the circuits survive? Does your application reside in a harsh environment, where the input supply can ring very high or even below ground? Even if these events are unlikely, it only takes one to destroy a circuit board.

What can you do to protect your sensitive circuits from voltages that are too high, too low, or even negative? To block negative supply voltages, system designers traditionally place a power diode in series with the supply. However, this diode takes up valuable board space and dissipates a significant amount of power at high load currents.

Another common solution is to place a high voltage P-channel MOSFET in series with the supply. The P-channel MOSFET dissipates less power than the series diode, but the MOSFET, and the circuitry required to drive it, drives up costs.

One drawback to both of these solutions is that they sacrifice low supply operation, especially the series diode. Also, neither protects against voltages that are too high—protection that requires more circuitry, including a high voltage window comparator and charge pump.

UNDERVOLTAGE, OVERVOLTAGE AND REVERSE-SUPPLY PROTECTION

The LTC4365 is a unique solution that elegantly and robustly protects sensitive circuits from unpredictably high or negative supply voltages. The LTC4365 blocks positive voltages as high as 60v and negative voltages as low as -40v. Only voltages in the safe operating supply range are passed along to the load. The only external active component required is a dual N-channel MOSFET connected between the unpredictable supply and the sensitive load.

Figure 1 shows a complete application. A resistive divider sets the overvoltage (ov) and undervoltage (uv) trip points for connecting/disconnecting the load from v_{IN} . If the input supply wanders outside this voltage window, the LTC4365 quickly disconnects the load from the supply.

The dual N-channel MOSFET blocks both positive and negative voltages at v_{IN} . The LTC4365 provides 8.4v of enhancement

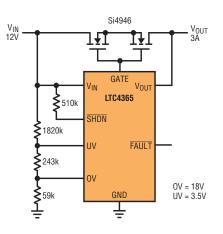


Figure 1. Complete 12V automotive undervoltage, overvoltage and reverse-supply protection circuit

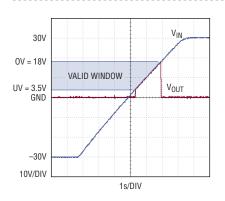
to the gate of the external MOSFET during normal operation. The valid operating range of the LTC4365 is as low as 2.5V and as high as 34V—the OV–UV window can be anywhere in this range. No protective clamps at v_{IN} are needed for most applications, further simplifying board design.

Accurate and Fast Overvoltage and Undervoltage Protection Two accurate (±1.5%) comparators in the LTC4365 monitor for overvoltage (OV) and undervoltage (UV) conditions at v_{IN} . If the input supply rises above the OV or below the UV thresholds, respectively, the gate of the external MOSFET is quickly turned off. The external resistive divider allows a user to select an input supply range that is compatible with the load at v_{OUT} . Furthermore, the UV and OV inputs have very low leakage currents (typically < 1nA at 100°C), allowing for large values in the external resistive divider.

Figure 2 shows the how the circuit of Figure 1 reacts as v_{IN} slowly ramps from -30V to 30V. The UV and OV thresholds are set to 3.5V and 18V, respectively. v_{OUT} tracks v_{IN} when the supply is inside the 3.5V–18V window. Outside of this window, the LTC4365 turns off the N-Channel MOSFET, disconnecting v_{OUT} from v_{IN} , even when v_{IN} is negative.

Novel Reverse Supply Protection The LTC4365 employs a novel negative supply protection circuit. When the LTC4365 senses a negative voltage at v_{IN} , it quickly connects the GATE pin to v_{IN} . There is no diode drop between the GATE and v_{IN} voltages. With the gate of the external

The LTC4365 is a unique solution that elegantly and robustly protects sensitive circuits from unpredictably high or negative supply voltages. The LTC4365 blocks positive voltages as high as 60V and negative voltages as low as -40V. Only voltages in the safe operating supply range are passed along to the load.



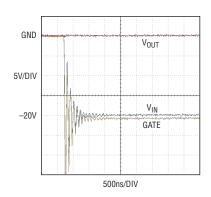


Figure 2. Load protection as VIN is swept from -30V to 30V

N-channel MOSFET at the most negative potential (v_{IN}) , there is minimal leakage from v_{OUT} to the negative voltage at v_{IN} .

Figure 3 shows what happens when v_{IN} is hot plugged to -20v. v_{IN} , v_{OUT} and GATE start out at ground just before the connection is made. Due to the parasitic inductance of the $v_{\ensuremath{\text{IN}}}$ and $\ensuremath{\text{GATE}}$ connections, the voltage at $v_{\rm IN}$ and GATE pins

Figure 3. Hot swapping VIN to -20V

ring significantly below -20v. The external MOSFET must have a breakdown voltage that survives this overshoot.

The speed of the LTC4365 reverse protection circuits is evident by how closely the GATE pin follows VIN during the negative transients. The two waveforms are almost indistinguishable on the scale shown. Note that no additional external circuits are needed to provide reverse protection.

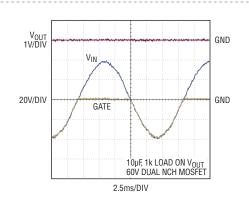


Figure 4. 36ms recovery timer blocks 28V, 60Hz AC line voltage

AC BLOCKING

The LTC4365 has a recovery delay timer that filters noise at V_{IN} and helps prevent chatter at v_{OUT}. After either an ov or uv fault (or when v_{IN} goes negative) has occurred, the input supply must return to the desired operating voltage window for at least 36ms in order to turn the external MOSFET back on.

V_{QUT}

GND

GND

0A

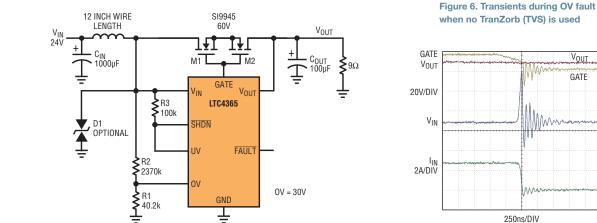


Figure 5. OV fault with large VIN inductance

The LTC4365's novel architecture results in a rugged, small solution size with minimal external components, and it is available in tiny 8-pin 3mm × 2mm DFN and TSOT-23 packages.

Going out of and then back into fault in less than 36ms keeps the MOSFET off.

Figure 4 shows the LTC4365 blocking an AC line voltage of 40V to -40V. The GATE pin follows v_{IN} during the negative portions, but remains at ground when v_{IN} goes positive. Note that v_{OUT} remains undisturbed.

HIGH VOLTAGE TRANSIENTS DURING FAULT CONDITION

Figure 5 shows a test circuit designed to produce transients during an overvoltage condition. The nominal input supply is 24v with an overvoltage threshold of 30v. Figure 6 shows the waveforms during an overvoltage condition at v_{IN} . These transients depend on the parasitic inductances on the v_{IN} and GATE pins. The circuits survived the transients without damage, even though the optional power clamp (D1) was not used during the experiments. **SELECT BETWEEN TWO SUPPLIES** With the part in shutdown, the v_{IN} and v_{OUT} pins can be driven by two different power supplies at different voltages. The LTC4365 automatically drives the GATE pin below the lower of the two supplies, thus preventing current from flowing in either direction through the external MOSFET. The application of Figure 7 uses two LTC4365s to select between two power supplies. Care should be taken to ensure that only one of the two LTC4365s is enabled at any given time.

REVERSE V_{IN} HOT SWAP WHEN V_{OUT} IS POWERED

LTC4365 protects against negative V_{IN} connections even when V_{OUT} is driven by a separate supply. With the LTC4365 in shutdown and V_{OUT} powered to 20V, Figure 8 shows the waveforms when V_{IN} is hot swapped to -20V. As long as the breakdown voltage of the external MOSFET is not exceeded (60V), the 20V supply at V_{OUT} is not affected by the reverse polarity connection at V_{IN} .

CONCLUSION

The LTC4365 controller protects sensitive circuits from overvoltage, undervoltage and reverse supply connections. The supply voltage is passed to the output only if it is qualified by the user adjustable UV and ov trip thresholds. Any voltage outside this window is blocked, up to 60v and down to -40v.

The LTC4365's novel architecture results in a rugged, small solution size with minimal external components, and it is available in tiny 8-pin 3mm × 2mm DFN and TSOT-23 packages. No reverse voltage blocking diode in series with the supply is needed; the LTC4365 performs this function automatically with back-toback external MOSFETS. The LTC4365 has a wide 2.5V to 34V operating range and consumes only 10µA during shutdown.



Power Supply Works with FET Drivers, DrMOS and Power Blocks for Flexible Placement Near Microprocessors

Theo Phillips

As microprocessors demand progressively more current at lower voltages, it becomes important to minimize conduction losses by placing the power supply as close to the load as possible. This increases the value of every square millimeter of board space near the load—particularly when multiple power stages are used. It is also important to locate the DC/DC controller away from high current paths, which can be difficult when the MOSFET gate drivers are in the controller package, because the gate traces must also be kept short. Sometimes the best solution is to use external power train devices or discrete N-channel MOSFETs and associated gate drivers.

The LTC3860 is a dual output step-down DC/DC controller designed to work in conjunction with drivers or power train devices such as DTMOS and power blocks, enabling flexible design configurations with PolyPhase[®] operation. Up to 12 stages can be paralleled to increase output current and clocked out of phase to minimize input and output filtering (Figure 1). In PolyPhase configurations, both output voltage (V_{OUT}) and ground terminals are monitored using a single differential amplifier, enabling tight regulation even where IR losses occur through vias, trace runs and interconnects. Regulation is further enhanced by the accuracy of the 600mV reference, which is ±0.75% with junction temperatures from 0°C to 85°C.

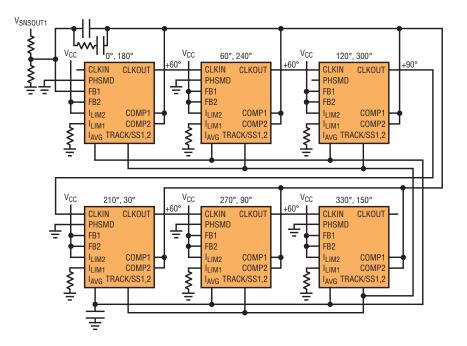


Figure 1. Pin interconnections for a 12-phase buck converter using the LTC3860

Voltage mode operation ensures that per-phase currents up to 30A can be achieved while a stable switching waveform is maintained. In a current mode converter, the voltage on the output of the error amplifier controls the peak or valley switch current, such that the switch current must always be monitored. With typical sense voltages of less than 100mV and current sense elements having resistance of less than $1m\Omega$, the introduction of noise is always a concern. In contrast, the LTC3860 compares the differentially sensed error voltage on VOUT to a sawtooth ramp, which is on the order of 1v. The ramp controls duty cycle—the larger the error voltage, the longer each phase's top switch stays on.

A 2-PHASE, SINGLE OUTPUT REGULATOR USING INTEGRATED DRIVER-MOSFETS (DrMOS) Citing needs for high power density, increased efficiency at high switching frequencies, and interoperability between controllers and power devices, Intel has issued a set of technical specifications for integrated driver-MOSFETS (DrMOS) used in step-down DC/DC converters powering its microprocessors. The compact layout reduces efficiency losses due to stray

Because the LTC3860 has a PWM output instead of onboard MOSFET drivers, it can occupy board space away from critical high current paths. Its applications include high current power distribution and industrial systems, and telecom, DSP and ASIC supplies.

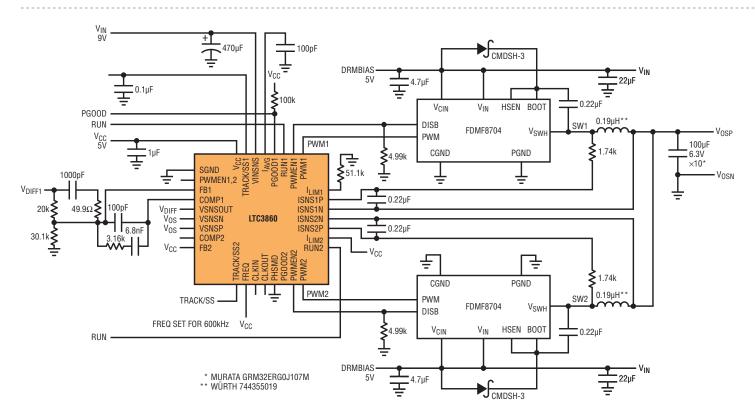


Figure 2. A 2-phase, single output converter using the FDMF8704 in each power stage to produce a 1V, 50A converter with all ceramic output capacitors

inductance. Several manufacturers have produced compliant devices. They are expected to operate at >500kHz (preferably 1MHz), deliver 25A per phase at ~1V from a 5V-16V input, and occupy 8mm × 8mm or 6mm × 6mm packages with defined pinouts. They must accept a PWM input, which is used to alternately turn the top and bottom MOSFETS on and off when the input is high or low. It must be possible to turn both MOSFETS off (three-state), by leaving the PWM pin floating or by pulling the DISB pin of the DrMOS low. An external inductor is required. The LTC3860 provides a PWM signal compatible with DrMOs-compliant devices. For example, the Fairchild FDMF8704 DrMOS is specified for operation up to 1MHz at 25A per phase, and the LTC3860 can be programmed for a switching frequency from 200kHz-1.2MHz. The LTC3860's high and low commands are interpreted by the FDMF8704 as top MOSFET on and bottom MOSFET on, respectively. This DrMOS does not recognize three-state signals on the PWM pin, but both of its MOSFETS turn off when its DISB pin is pulled low. The LTC3860's PWMEN pulls high through an open drain whenever PWM is high or low. When PWM is

three-state, an external resistor pulls the PWMEN pin low. Thus, three-state operation of the power stage is accomplished here by tying the PWMEN pin of the LTC3860 to the DISB pin of the DTMOS.

Figure 2 is the schematic for a 2-phase, single output converter using the FDMF8704 in each power stage to produce a 1V, 50A converter. A switching frequency of 600kHz is selected by tying CLKIN low and FREQ high. The effective frequency is 1.2MHz, because the two channels operate 180° out of phase.

By reducing the latency between clock cycles, the high switching frequency

The LTC3860 has internal current sharing, and only requires simple pin configurations and one external capacitor at the I_{AVG} pin to run phases together. The I_{AVG} pin stores a charge corresponding to the instantaneous average current of all phases.

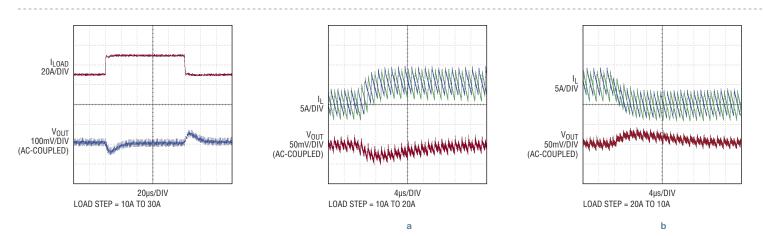


Figure 3. Load transient response for the converter of Figure 2

improves transient response. Stable operation is possible with all ceramic output capacitors, which minimize the output ripple because of their low ESR. Figure 3 shows the converter's transient response to a large load step.

A common drawback of voltage mode converters is that they do not play well together when they are combined to increase power capability. They typically use the outputs of onboard op amps as their loop compensation nodes. Because these outputs are low impedance, they cannot just be tied together to balance the current from each power stage. An external circuit would be needed for each phase.

The LTC3860 has internal current sharing, and only requires simple pin configurations and one external capacitor at the I_{AVG} pin to run phases together. The I_{AVG} pin stores a charge corresponding to the instantaneous average current of all phases. The slave channel's FB pin is connected to $INTV_{CC}$, a single differential amplifier is placed ahead of the master's FB pin, and each TRACK/SS, COMP, and output is tied to the other. The power stages are now actively balanced. One power good indicator, PGOOD1, reports undervoltage and overvoltage events.

The maximum current sense mismatch between phases is ±2mV between channels on the same IC or on different ICs. This translates to tight current sharing between channels in PolyPhase applications, particularly when the current sense elements are well matched. Here, the Würth 744355019 inductors' DC resistance is specified to have a tolerance of ±10% at 20°C. Figures 4a and 4b show that the inductor current levels follow each other closely during a load transient.

A differential amplifier provides remote sensing of the output voltage. v_{SNSP} and v_{SNSN} are tied to v_{OUT} and PGND at the point of load. The potential between these pins is translated, with unity gain,

to a potential between v_{SNSOUT} and SGND. v_{SNSOUT} is tied to the feedback string leading to FB of the master channel. This arrangement overcomes error due to board interconnection losses, which often result in voltage offsets between power ground and SGND. For this 1V output, the difference between no load and full load v_{OUT} is typically just 1mV.

Figure 4. The converter of Figure 2 demonstrates stable current sharing at

both edges of a load transient: (a) rising edge; (b) falling edge.

WHEN EFFICIENCY IS THE PRIORITY When efficiency is a higher priority than minimizing board space, operating the LTC3860 at a relatively low switching frequency reduces switching losses, while adding a synchronous MOSFET reduces conduction losses, particularly if the converter operates at low duty cycle. Since DTMOS packages contain just one main and one synchronous MOSFET, it becomes beneficial to use discrete FETs and drivers. The powerful LTC4449 driver is ideally suited to the task.

The LTC4449 is designed to drive top and bottom MOSFETs in a synchronous

When efficiency is a higher priority than minimizing board space, operating the LTC3860 at a relatively low switching frequency reduces switching losses, while adding a synchronous MOSFET reduces conduction losses, particularly if the converter operates at low duty cycle. Since DrMOS packages contain just one main and one synchronous MOSFET, it is beneficial to use discrete FETs and drivers.

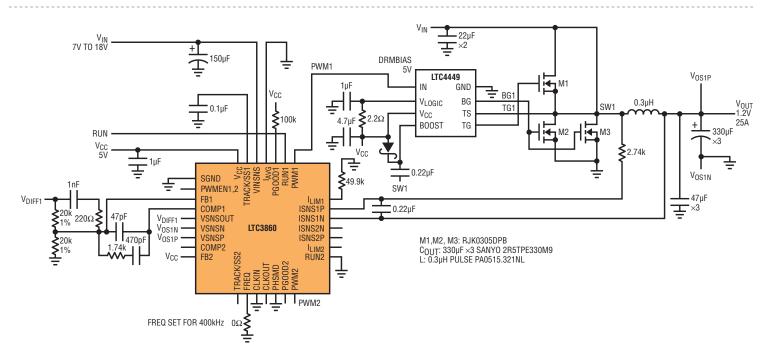


Figure 5. The LTC3860 can use the LTC4449 to drive discrete MOSFETs. A synchronous MOSFET is added to improve efficiency.

DC/DC converter. It accepts high, low and three-state inputs, with thresholds proportional to the LTC3860 power supply because the LTC4449 V_{LOGIC} is at the same potential as the LTC3860 v_{CC} . The v_{CC} of the LTC3860 can range from 3V to 5.5V, and if it drops below the undervoltage lockout (UVLO) threshold (2.9V falling, 3.0V rising), both channels of the LTC3860 are disabled. UVLO ensures that the driver operates only when v_{CC} is at safe levels.

For maximum efficiency, the LTC4449's top gate has pull-up and pull-down times of 8ns and 7ns; the bottom gate, 7ns and 4ns, while looking into 3000pF loads. Adaptive shoot-through protection ensures that the dead times are short enough to avoid power loss, but not so short that cross-conduction

can occur. The driver is available in a low profile 2mm × 3mm DFN package.

Figure 5 shows a schematic for a single channel, 400kHz, single phase converter using the LTC4449 and discrete MOSFETS. Figure 6 shows the improvement in efficiency compared to a DTMOS solution operating at the same frequency with the same passive components.

Discrete MOSFETS also provide an input voltage capability higher than the DrMOS requirement (16v). The VINSNS pin of the LTC386o, which connects to the supply at the drain of the main MOSFET, can handle up to 24v. This allows LTC386o applications to benefit from the large number of 30v MOSFETS available from various manufacturers. 400kHz operation is set by tying the FREQ and CLKIN pins low. Other switching frequencies, from 250kHz to 1.25MHz, can be programmed with a single resistor from FREQ to ground, or synchronized with an external signal source, with a smooth transition to and from the resistor-set frequency if an interruption in the sync signal occurs. No external PLL filter components are required for synchronization.

The VINSNS pin monitors the input voltage and immediately adjusts the duty cycle in a manner inversely proportional to v_{IN} , bypassing the feedback loop. This feature brings two benefits: a set of compensation values works across the entire v_{IN} range, and during a line transient deviation in v_{OUT} is minimal, as Figure 7 shows. Instead of selecting power stage components, designers have the option of specifying an entire power stage on a small PC board. Known as a power block, it includes MOSFETs, a MOSFET driver, an inductor, and minimal input and output capacitors.

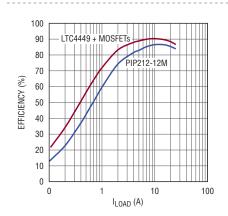


Figure 6. The circuit of Figure 5 shows improved efficiency compared with a typical DrMOS solution. The compromise is in board space—a DrMOS occupies 36mm² or 64mm², and the driver and three MOSFETs occupy 101mm², excluding the traces connecting the components.

The ILIM pin provides a handle for setting current limit. It sources 20µA through an external resistor, providing a voltage proportional to the current limit. When current limit is reached, the LTC3860 three-states the PWM output, resets the soft-start timer, and waits 32768 switching cycles before restarting (Figure 8).

The LTC3860 has the ability to start up into a prebiased output. When the TRACK/SS voltage is below the voltage at FB, the LTC3860 will not switch (except for refresh pulses, which keep the boost capacitor charged). When TRACK/SS exceeds FB, switching commences, but inductor current is not allowed to reverse until the output reaches regulation, when continuous conduction mode begins. Thus, the output is allowed to rise gently (Figure 9).

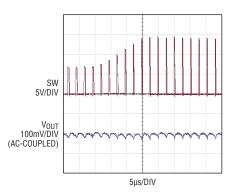
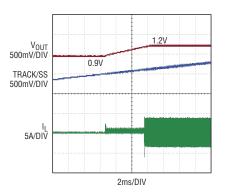


Figure 7. Through its VINSNS pin, the LTC3860 provides line feedforward compensation, preventing steady state and dynamic variations in V_{OUT} when V_{IN} is not constant.

WHEN SIMPLICITY IS REQUIRED

Instead of selecting power stage components, designers have the option of specifying an entire power stage on a small PC board. Known as a power block, it includes MOSFETS, a MOSFET driver, an inductor and minimal input and output capacitors. Electrical and mechanical connection is made through standoffs which surface mount onto the main board.





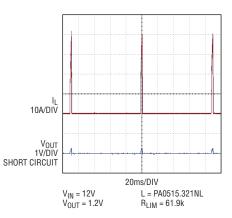


Figure 8. Short circuit behavior of the LTC3860

Connections are also provided for temperature sensing and inductor DCR sensing. They typically operate at 12v input, switching at 400kHz–500kHz and source 20A–40A. Unlike DTMOS, power blocks do not occupy a standard footprint.

The LTC3860 is shown in Figure 10 coupled with a Delta power block. This high current, 400kHz, 2-phase application can source 45A at its output. Since each channel operates 180° out of phase with respect to the other, the effective switching frequency is doubled, minimizing stress on the input and output capacitors. The power block's physical dimensions are approximately 1.0" L \times 0.5" W \times 0.5" H, yielding a small solution size. Topside heat sinks are provided for the onboard MOSFETS, and 200LFM airflow at <55°C is required. The LTC3860 is a dual output step-down DC/DC controller designed to work in conjunction with drivers or power train devices such as DrMOS and power blocks, enabling flexible design configurations with PolyPhase operation. Up to 12 stages can be paralleled.

SOME OPTIONS WITH THIS VERSATILE CONTROLLER

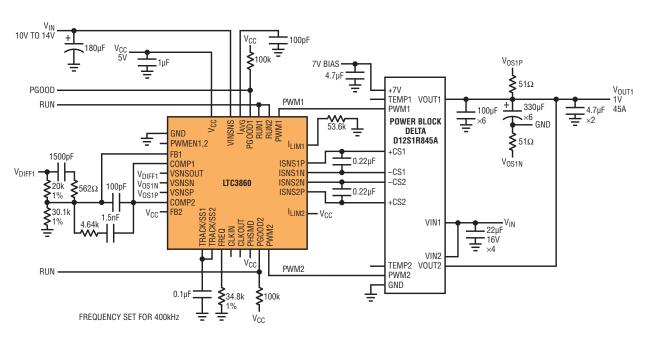
The applications presented here use the drop across the inductor to sense current sharing and current limit. If a small increase in power loss is acceptable, greater accuracy may be achieved by using a discrete sense resistor in series with the inductor. The applications here also have output voltages in the 1.x range. Outputs as low as 0.6v (the reference voltage) or as high as 4v (the maximum output voltage of the differential amplifier) are also possible, with ±1% reference voltage accuracy over an operating temperature range of -40°C to 125°C.

Instead of the default 2ms soft-start used by the applications here, adjustable softstart (>2ms) and tracking are also possible for each output. Longer soft-start times are achieved by adding >10nF from TRACK/SS to ground. Tracking is achieved by driving the pin with a DC voltage of less than 0.6v. The output regulates to the lowest of the internal 600mV reference, the voltage on the TRACK/SS pin, or the internal soft-start ramp for that channel.

CONCLUSION

The LTC3860 is a voltage mode buck controller that supports up to 12 phases in parallel with onboard current sharing. It may be used with DTMOS, power blocks or discrete MOSFETs and the LTC4449 driver. Because the LTC3860 has a PWM output instead of onboard MOSFET drivers, it can occupy board space away from critical high current paths. Its applications include high current power distribution and industrial systems, and telecom, DSP and ASIC supplies. The LTC3860 is available in a 32-lead 5mm × 5mm QFN package.





The Harsh Reality of Wide-Ranging 4V–36V Automotive Batteries Is No Problem for Triple Output Regulator in $4mm \times 5mm$ QFN

Michael Nootbaar

DC/DC converters for automotive applications must operate in an environment of extremes. Input transients can exceed the nominal battery voltage by a factor of five and last hundreds of milliseconds, while temperatures under the hood soar far above the capability of typical commercial grade ICs. In this harsh environment, space is tight, so even the most robust devices must perform multiple functions.

The LT3694/LT3694-1 meets these requirements by combining a 2.6A switching regulator and two low dropout linear regulators in a compact 4mm × 5mm QFN package or a thermally enhanced TSSOP. The switching regulator requires a single inductor and has an internal power switch, cycle-by-cycle current limiting and track/soft-start control. Each LDO requires only an external NPN pass transistor and includes foldback current limiting and track/soft-start control. An internal overvoltage detector shuts off the switching regulator when V_{IN} exceeds 38v, protecting the switch and the Schottky rectifier. This allows it to survive transients on VIN up to 70V without damage to itself or the rectifier.

4V-36V INPUT SWITCHING REGULATOR

The LT3694/LT3694-1 includes a 36v monolithic switching regulator capable of providing up to 2.6A of output current from input voltages down to 4v. Output voltages can be set as low as the feedback reference of 0.75v.

The regulator uses a current mode, constant frequency architecture, which keeps loop compensation simple. External compensation allows custom tailoring of loop bandwidth, transient response and phase margin.

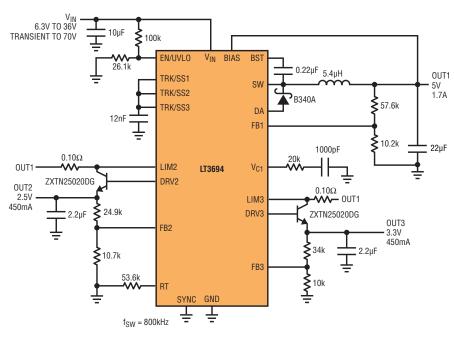
TWO LOW DROPOUT LINEAR REGULATORS

The LT3694/LT3694-1 includes two LDO linear regulators that use an external NPN pass transistor to provide up to 0.5A of output current. The base drive can supply up to 10mA of base current to the pass transistor and is current limited. The LDO is internally compensated and is stable with output capacitance of 2.2µF or greater. It uses the same 0.75V feedback reference as the switching regulators.

The LDO drive current is drawn from the BIAS pin if it is at least 0.9V higher than the DRIVE pin voltage, otherwise it's drawn from v_{IN} . This reduces the power consumption of the LDO, especially when v_{IN} is relatively high.

The LDO has foldback current limiting by monitoring a sense resistor in the collector of the NPN pass transistor. The initial threshold is set at 60mV, but folds back as v_{FB} decreases until at $v_{FB} = 0$ the threshold is at 26mV. A sense resistor of 0.1 Ω sets the operating current limit at 600mA, but the short circuit current limit drops to 260mA. This reduces power dissipation in the pass transistor with a shorted output.





The LT3694/LT3694-1 combines a 2.6A switching regulator and two 500mA low dropout linear regulators in a compact 4mm \times 5mm QFN package or a thermally enhanced TSSOP.

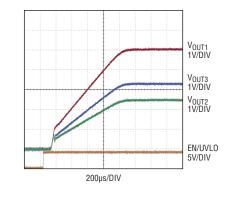
The LDOS can be shut down by pulling the FB pin above 1.25V with at least 30µA. If independent control of the LDOS is needed, each LDO output can be forced to oV by pulling its TRK/SS pin low. If the track or soft-start functions are needed, use an open drain output in parallel with the track or soft-start circuitry described below. If track and soft-start are not necessary, then a standard CMOS output (from 1.8V to 5V) with a 1k series resistor works fine.

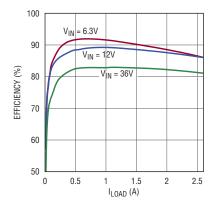
TRACK/SOFT-START CONTROL

The buck regulator and each LDO has its own track/soft-start (TRK/SS) pin. When this pin is below the 0.75V reference, the regulator forces its feedback pin to the TRK/SS pin voltage rather than the reference voltage. The TRK/SS pin has a 3µA pull-up current source.

The soft-start function requires a capacitor from the TRK/SS pin to ground. At startup, this capacitor is at ov, which forces the regulator output to ov. The current source slowly charges the capacitor voltage up and the regulator output ramps up proportionally. Once the capacitor voltage reaches 0.75v, the regulator locks onto the internal reference instead of the TRK/SS voltage. The TRK/SS pin is pulled low on any shutdown event (overvoltage, overtemperature, undervoltage) in order to discharge the soft-start capacitor.

The track function is achieved by connecting the slave regulator's TRK/SS pin to a resistor divider from the master regulator output. The master regulator uses a normal soft-start capacitor as described







above to generate the start-up ramp that controls the other regulators. The resistor divider ratio sets the type of tracking, either coincident (ratio equal to slave feedback divider ratio) or ratiometric (ratio equal to master feedback divider ratio plus a small offset). The TRK/SS pins can also be tied together to a single capacitor to provide ratiometric tracking, but only if the LDOs are not shut down by pulling FB high (see the section "Two Low Dropout Linear Regulators" above).

ENABLE AND UNDERVOLTAGE PROTECTION

The LT3694/LT3694-1 includes an enable and user programmable undervoltage lockout function using the EN/UVLO pin. The undervoltage lockout can protect against pulse stretching. It can also protect the input source from excessive current since the buck regulator is a constant power load and draws more current when the input source is low. The undervoltage lockout shuts off all three regulators when tripped.

Figure 3. Switching regulator efficiency

These two functions use a pair of built-in comparators at the EN/UVLO input. The enable comparator has a 0.5v threshold and activates the internal bias circuits of the LT3694/LT3694-1. When EN/UVLO is below the enable threshold, the LT3694/LT3694-1 is in shutdown and draws less than 1µA with 12V input. The undervoltage comparator has a 1.2V threshold and has 2µA of hysteresis. The UVLO hysteresis is a current sink that activates when EN/UVLO drops below the 1.2v threshold. A resistor divider from VIN to the EN/UVLO input sets the trip voltage and hysteresis. The undervoltage threshold is accurate over temperature to allow tight control over the trip voltage. The EN/UVLO pin should be connected to v_{IN} if the function isn't used.

FREQUENCY CONTROL

The switching frequency is adjustable from 250kHz to 2.5MHz, set by a single resistor to the R_T pin. Higher frequencies allow smaller inductors and capacitors, but use more power and have a smaller

(continued on page 43)

Ultralow Power 16-Bit High Speed Signal Chain Solution for Portable Sampling Systems

Clarence Mayott

The LTC2195 family of ultralow power, dual 16-bit, 25Msps to 125Msps analog-to-digital converters (ADCs) dissipate half the power of competing 16-bit solutions, extending battery run times in portable electronics. Despite consuming only ~1.5mW/Msps per channel, the LTC2195 does not shirk performance to save power, yielding a 76.8dB signal-to-noise ratio (SNR) and 90dB of spurious free dynamic range (SFDR) at base-band (0MHz–62.5MHz, the first Nyquist zone). Serial LVDS outputs reduce the number of data lines required for routing the ADC data while minimizing digital feedback.

SIGNAL PATH DESIGN

The LTC2195 family is an ideal solution for applications that require 16-bit performance and ultralow power consumption to extend battery life. Portable medical imaging equipment is a perfect example. In many imaging applications the signal from the image sensor must be conditioned before being sampled by the ADC. For this task, it is important to choose a low noise, low power amplifier that matches the performance of the ADC, such as the LTC6406, which makes a good match for the LTC2195 family.

The LTC6406 is a fully differential amplifier with low noise $(1.6nV/\sqrt{Hz} \text{ at the input})$ and high linearity (+44dBm OIP3 at 20MHz) in a small 3mm × 3mm

QFN package. External resistors set the gain, giving the user maximum design flexibility. Low power consumption (59mW with a 3.3V supply) minimizes the effect on the system power budget. This amplifier also has a common mode voltage range that extends down to 0.5V meaning it can be paired seamlessly with the LTC2195, which has a nominal common mode voltage of 0.9V.

Typically the output of an image sensor is single-ended. This requires a single-ended to differential translation before being sampled by the ADC. If response to DC is also required, a transformer cannot be used. This situation mandates a low noise amplifier that is capable of doing single-ended to differential translation, like the LTC6406.

The amplifier must be followed by a filter to reduce the wideband noise of the amplifier and to isolate the output of the amplifier from the ADC inputs the ADC inputs produce common mode glitches associated with the commutation of the sample caps. A filter helps attenuate these glitches, protecting the amplifier. A high order filter is not required, since the noise of the amplifier is fairly low. With a corner frequency of 12MHz, the filter used here is adequate—it does not degrade the performance of the ADC.

The final filter should be designed to reduce only the wideband noise of the amplifier, not as a selectivity filter with a

		25Msps	40Msps	65Msps	80Msps	105Msps	125Msps
SINGLE CHANNEL	7×7 QFN 1.8V Single ADCs, Parallel Outputs	2160	2161	2162	2163	2164	2165
DUAL Channel	9×9 QFN 1.8V Dual ADCs Parallel Outputs	2180	2181	2182	2183	2184	2185
	7 × 8 QFN 1.8V Dual ADCs, Serial LVDS Outputs	2190	2191	2192	2193	2194	2195
POWER	(mW/Ch)	40	60	80	100	155	185

Table 1. The new generation of ultralow power 16-bit ADCs

In many imaging applications the signal from the image sensor must be conditioned before being sampled by the ADC. For this task, it is important to choose a low noise, low power amplifier that matches the performance of the ADC, such as the LTC6406, which makes a good match for the LTC2195 family.

steep transition band. A steep transition band in the filter increases insertion loss and degrades the OIP3 of the amplifier, which leads to distortion of the signal from the image sensor. The circuit shown in Figure 1 accomplishes this goal.

RESULTS

Figure 2 shows the performance of this circuit. The results show that the linearity of the amplifier does not degrade the SFDR of the ADC at low input frequencies. The SNR also remains unchanged at 76.5dB. The LTC6406 does not degrade the SNR or the SFDR of the LTC2195 when using it at unity gain.

MODIFICATIONS

For this design there are some trade-offs that can be made to change the performance of the system. First, the gain can change by increasing the feedback resistors, or decreasing the source resistors. Typically the source resistors are set by the output impedance of the sensor itself. The feedback resistors are then used to modify the gain of the amplifier. The LTC6406 can be used to produce attenuation or gain depending on the output of the image sensor. As the gain of the amplifier increases, the amount of compensation capacitance required to stabilize the amplifier decreases. In this unity gain application 1.8pF is enough to produce good results. If the amplifier is used to attenuate the signal, more capacitance is required.

The low order, low pass filter in Figure 1 attenuates the wideband noise of the amplifier with a cutoff frequency of 12MHz. This cutoff frequency can be increased by decreasing the value of the final capacitors. Because the amplifier cannot drive a low impedance, and the ADC wants to see a low impendence at its analog inputs the impendence of the filter has been optimized to satisfy both the amplifier and the ADC. If a higher order filter is required, it should be located prior to the final drive amplifier, and more gain should be used in the amplifier stage to accommodate for the insertion loss in the filter. Some filtering is required between the final amplifier and the ADC. Even a

simple RC low pass filter is better than driving the ADC directly into the amplifier.

ABOUT THE LTC2195

The LTC2195 is a 16-bit 125Msps, simultaneous sampling, dual ADC operating from a single 1.8v supply. This circuit can be easily applied to the 14- or 12-bit members of the family or to converters that sample at much lower sample rates. The LTC2195 family also contains dual and single channel ADCs with parallel outputs. The LTC2185, 2-channel ADC and the LTC2165 single channel ADC have the same excellent 16-bit performance and low power as the LTC2195, but with parallel outputs that can simplify the FPGA code required to collect data. These flexible ADCs include the choice of CMOS, DDR CMOS or DDR LVDS outputs with programmable digital output timing, programmable LVDS output current and optional LVDS output termination. The LTC2185 and LTC2165 also have the popular randomizer and alternate bit polarity features that help to reduce digital feedback. More information about alternate bit polarity mode and (continued on page 43)

Figure 1. Imaging application

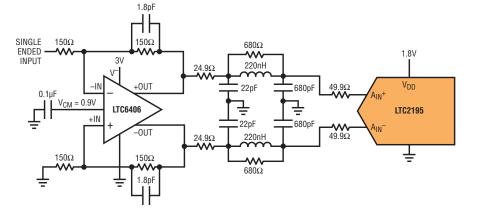
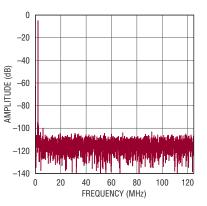


Figure 2. FFT results of circuit in Figure 1 with $F_S = 125Msps F_{IN} = 1MHz$



Two Monolithic DC/DC Converters Take 3.6V–15V Inputs Down to 0.6V at High Frequency, Shrinking Battery-Powered Applications in Everything from Handhelds to Automobiles

Mylien Tran and Theo Phillips

When a relatively high voltage rail (12V) must be stepped down to a relatively low level (3.3V, 1.8V), the traditional go-to converter is a DC/DC switching controller that drives external MOSFETs. In many applications, replacing the typical controller-MOSFET-diode combo with a monolithic regulator would save space, design time and cost. The problem is that 12V rails are too high for many monolithic buck converters, which usually cannot be used with inputs above 6V. Additionally, switching losses typically prevent practical operation above ~1MHz, precluding the use of the smallest possible inductors, and in the end, negating some size advantages of a monolithic regulator.

The LTC3601 and LTC3604 are high performance monolithic synchronous step-down regulators capable of supplying up to 1.5A and 2.5A, respectively. They operate from a wide input voltage range of 3.6V to 15V—a range encompassing battery chemistries found in handheld devices, PCs, and automobiles. Their unique constant frequency/controlled on time architecture has a minimum on-time of 20ns, ideal for high step-down ratio applications that demand high switching frequencies and fast transient response while maintaining high efficiency.

DEFAULT CONFIGURATION WITH MINIMAL COMPONENTS

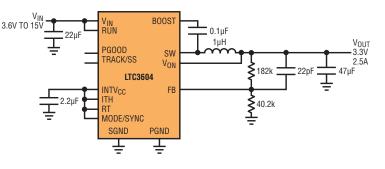
To reduce external component count, cost, and design time, switching frequency and loop compensation may be set with simple pin configurations. Figure 1 shows a typical application. To enable 2MHz operation, the oscillator frequency program pin (RT) is tied to the internal 3.3V regulator output pin (INTVCC). Default compensation is applied when the compensation pin (ITH) is tied to INTVCC, producing a clean load transient response (Figure 2). Operating frequency is programmable from 800kHz to 4MHz with an external resistor from RT to ground. For switchingnoise-sensitive applications, the LTC3601 and LTC3604 can be externally synchronized over the same frequency range regardless of the state of RT. No external PLL components are required for syncing.

Some applications call for shifting the switching frequency during operation, usually to avoid interference with adjacent radio receivers. Figure 3 shows that the deviation in output voltage is minimal even when the sync frequency introduced at MODE/SYNC is changing rapidly.

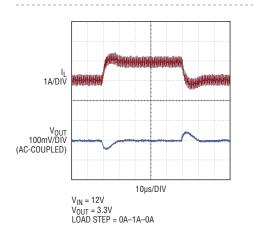
Both ICs feature optional Burst Mode[®] operation for superior efficiency at low load currents (Figure 4), or alternatively, forced continuous mode, which gives up light load efficiency for minimal output ripple and constant frequency operation. Even so, Burst Mode operation ripple is typically only 20mV.

The built-in internal 400µs soft-start timer prevents current surges at v_{IN} during start-up. Longer soft-start times can be implemented by ramping the TRACK pin or connecting a capacitor from TRACK pin to ground ($t_{SS} = 430,000 \times C_{TRACK/SS}$). An open drain PGOOD pin monitors the output and pulls low if the output voltage is ±8% from the regulation point. The additional v_{IN} overvoltage and short-circuit protection make for an all-around robust IC.

Figure 1. A wide input range to 3.3V, 2.5A application



The LTC3601 and LTC3604 employ a unique constant frequency/controlled on time architecture with a minimum on-time of 20ns—ideal for high step-down ratio applications that demand high switching frequencies and fast transient response.



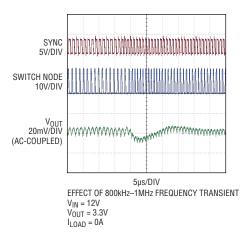


Figure 2. Fast transient response of the circuit in Figure 1

HIGH FREQUENCY, LOW DUTY CYCLE, NO PROBLEM

Many microprocessors require low voltage 1.x volt rails, but they also reside in applications that demand high switching frequencies to keep passive components small and avoid RF interference with critical frequency bands. The problem is that achieving the magic combination of high a step-down ratio and high switching frequency can be elusive, because it requires such a short minimum on-time. Figure 5 shows the schematic for the LTC3604 in a 4 MHz, 12V–1.8V application. The 38ns

Figure 3. The synchronized switching frequency can be shifted on the fly, with little change in V_{OUT} .

on-time required for this application is well above the LTC3604's 20ns minimum.

The design in Figure 5 takes advantage of a number of the LTC3604's features. Normally the minimum input voltage is 3.6v, but here the undervoltage lock-out is raised to 6v by adding a resistive divider from v_{IN} to RUN. Soft-start time is increased to 4.3ms by adding 10nF capacitance from TRACK to ground. The switching frequency is synchronized to 4MHz from an external source. If that source should fail, the internal

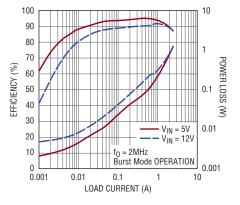


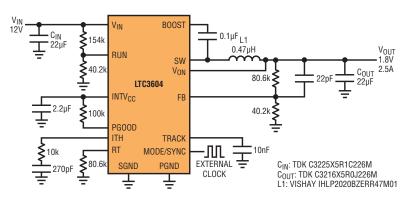
Figure 4. Burst Mode operation yields high efficiency at light loads, and low R_{DS(ON)} switches maintain high efficiency at maximum load.

oscillator (also set at 4MHz) will take over. Finally, loop compensation is external.

CONCLUSION

The LTC3601 and LTC3604 are part of a new generation of monolithic DC/DC converters capable of handling relatively high input voltages and lower duty cycles. Their compact size, high performance, and minimal components design make them ideal for compact applications. Both ICs are offered in compact, thermally enhanced 3mm × 3mm QFN and MSOP packages.

Figure 5. The LTC3604 can operate at high frequency (4 MHz) and low duty cycle, allowing high step-down ratios from a compact footprint



Simple Circuit Monitors Health of –48V Telecom Lead-Acid Battery Backup Systems

Jon Munson

Telecommunications infrastructure has always been powered by voltages that are negative with respect to ground to minimize corrosion in buried cable. Telcos typically use –48V power, with backup power supplied by large battery arrays to carry the system through utility outages. These power backup systems traditionally comprise four 12V lead-acid batteries in series, though newer lithium cell technology promises to make inroads as systems are updated.

Every battery backup system must be continually monitored for the charge state and health of the batteries. In fact, although stacking batteries is easy, it can be difficult to build a monitoring system that can measure and digitize both the condition of individual cells, and monitor the high voltage potential of the combined cells. Enter the LTC6803 multicell battery stack monitor.

The LTC6803 is designed to measure and digitize individual cell potentials in large lithium cell stacks with total potentials

beyond 6ov (surviving surges to 75v). Although the LTC6803 is ostensibly designed to monitor lithium-based battery systems, it can just as well be used to support traditional –48v lead-acid battery stacks. Regardless of cell chemistry, all the measuring potentials are below ground

CSB

SDO

SD

SCK

VCC

0

VL

D01

D02

GND

SDOEE

µC_CSB

►uC MISO

µC_MOSI

uC SCK

►µC_VCC

UC GND

1ııF

10uH CSB CSBC CS2B SDC SDOI SD02 SDI SCKO SDI2 12V SLA V+ SCK SCK2 C12 V_{MODE} VCC2 PDZ7.5B S12 GPI02 AVCC2 10uH 4.7u C11 GPI0⁻ PDZ S11 WDTE 12 4.7uF ITM2883-5S C10 LTC6803-1 N **-** 12V AV⁻ PDZ7 SLA TOS S10 4.7uF VREG AV⁺ <u>C9</u> PDZ7 V+ **S**9 VREF 10µH 1uF 4.7µF C8 V_{TEMP2} GND2 1uF PDZ7 **S**8 VTEMP 4.7uF 12V C7 N PDZ7 SLA V S7 4 711F S1 **C6** PDZ7 C1 **S6** 10µH 4.7µF C_{5} S2 PDZ7 **S**5 C2 4.7µF **S**3 12V C4 PDZ7 SI A C3 4.7uF PDZ7 ~~ 4.7uF

PDZ7

4.7µF PDZ7 4.7µF

-48V

100nF

100Ω

Figure 1. Isolated lead-acid telecom battery-stack monitor

Although the LTC6803 is ostensibly designed to monitor lithium-based battery systems, it can also be used to support traditional –48V lead-acid battery stacks.

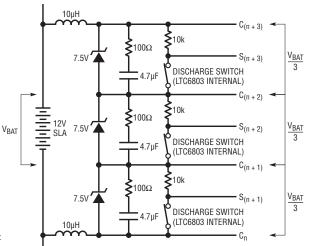


Figure 2. Voltage-divider structure for each 12V battery measurement

or possibly floating during maintenance procedures. Ideally, these batteries should be measured by circuitry that is independent of the relative grounding between the batteries and the central-office equipment, thus Galvanic isolation is desirable.

A SIMPLE SOLUTION FOR LEAD-ACID STACKS

Since the ADC range for an individual LTC6803 input channel maxes out at 5.37V, divider networks are used to spread each 12V battery potential across three channels. Figure 1 shows how. Each battery potential is acquired by summing triplets of input channel readings (C_N inputs). Here the cell-balancing controls (S_N output discharge switches) are re-purposed to continually activate voltage dividers using external 10k resistors by setting all DCC configuration bits to 1. In this way, each channel is converting a 4v nominal potential.

The 4.7μ F bypass capacitors accurately hold the intermediate voltages as small ADC sampling currents flow, while 100Ω series resistors and 10μ H inductors provide hot-insert surge limiting. For best accuracy, the STCVDC conversion command (0x60) should be used so that the always-enabled discharge switches remain on throughout the conversion process.

When communication has stopped and the part times-out, or it is directly commanded to standby mode, the balancing discharge switches are turned off and the dividers are effectively disconnected so that no appreciable battery drain occurs. A simplified equivalent circuit of a particular divider section is shown in Figure 2.

An LTM2883 SPI data isolator is used so that the circuit accommodates any grounding differential with respect to the associated microprocessor circuitry. The LTM2883 also provides isolated DC power rails that can furnish several hundred mW if needed.

CONCLUSION

The LTC6803 provides a flexible solution for telecom battery stack measurement, including stacks using 12V lead-acid batteries. The 12V units are measured by summing the readings of three input channels that have been hardware configured to split the 12V into sub-measurements, thus achieving an effective full-scale range of 16.1V for each battery. Isolation of the data acquisition function from the processor support is important for elimination of grounding errors and safety hazards and is readily provided by the LTM2883 SPI isolator module.

Easy, $\pm 5V$ Split-Voltage Power Supply for Analog Circuits Draws Only 720nA at No Load

Jim Drew

Analog circuits often need a split-voltage power supply to achieve a virtual ground at the output of an amplifier. These split-voltage power supplies are generally low power supplies supporting tens of milliamps of differential current loads. Figure 1 shows such a power supply using two LTC3388-3 20V high efficiency step-down regulators powered from a 6V–12V power source.

The positive voltage rail is created by configuring one LTC3388-3 in its standard buck topology while the negative voltage rail is created with a second LTC3388-3 by grounding the v_{OUT} connection and using the GND pin as the negative voltage rail. The negative voltage rail is connected to the exposed pad of this LTC3388-3 and must be isolated from the system ground plane and have sufficient surface area to provide adequate cooling of the LTC3388-3.

The LTC3388-1 and LTC3388-3 are high efficiency step-down regulators that draw only 720nA (typ) of DC current at no load while maintaining output regulation. They are capable of supplying up to 50mA of load current and contain an accurate undervoltage lockout (UVLO) feature to maintain a low quiescent current when the input is below 2.3v. The output voltage is digitally programmable to four output regulated voltages along with a PGOOD status pin that indicates that the outputs are above 92% (typ) of the output setting. The LTC3388-1 can be digitally set to 1.2v, 1.5v, 1.8v or 2.5v while the LTC3388-3 can be set to 2.8v, 3.0v, 3.3v or 5.0v. Both devices are available in a 10-lead MSE or a 3mm × 3mm DFN package.

OPERATION OF THE SPLIT-VOLTAGE SUPPLY

Configuring the LTC3388 as a buck regulator creates a positive voltage by ramping the inductor current up to I_{PEAK} (150mA typ) through an internal PMOS switch and then ramping the current down to omA through an internal NMOS switch. This action charges the output capacitor to slightly above the regulation voltage at which time the buck regulator enters sleep mode.

As the output voltage decays due to an external load, the buck regulator remains

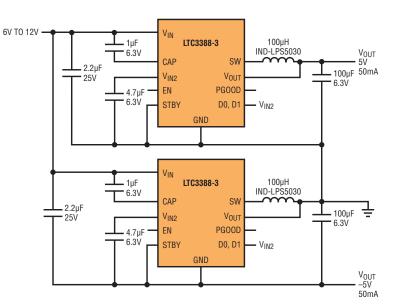
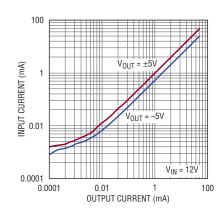


Figure 1. Easy split-voltage power supply

Figure 2. Input current versus output current for the split voltage power supply of Figure 1 (-5V curve also applies to -5V supply shown in Figure 3)



The LTC3388-1 and LTC3388-3 are high efficiency step-down regulators that draw only 720nA (typ) of DC current at no load while maintaining output regulation. They are capable of supplying up to 50mA of load current and contain an accurate undervoltage lockout (UVLO) feature to maintain a low quiescent current when the input is below 2.3V.

in sleep mode and an internal sleep comparator monitors the output voltage. When the output voltage drops below the regulation voltage, the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with MOSFET switching and maintains an output voltage at light loads. The buck regulator is able to support 50mA of average load current when it is switching.

A negative output voltage rail is created by grounding the v_{OUT} node of the buck regulator. This sets the ground reference connection of the LTC3388 as a negative voltage rail. The voltage from the v_{IN} pin to the negative voltage rail is the sum of the input voltage plus the magnitude of negative voltage rail. This limits the source voltage to 20V (the LTC3388's $v_{IN(MAX)}$) minus the magnitude of the negative rail voltage.

The inductor current is ramped up to I_{PEAK} through the internal PMOS switch as in the buck regulator configuration and then down to zero through the NMOS switch, charging the output capacitor to a negative voltage. This switching action is that of an inverting critical

conduction synchronous buck-boost converter. The maximum output current of this configuration is limited by the peak current of the inductor, the input voltage and the magnitude of the output voltage. The expression below estimates the maximum output current available.

$$I_{OUT} = \frac{I_{PEAK}}{2} \bullet \frac{V_{IN}}{V_{IN} + V_{OUT}}$$

In a split voltage power supply application, the analog circuit is connected between the positive voltage rail and the negative voltage rail. This results in the load current of both regulators to be equal in magnitude. Figure 2 is a plot of the input current versus the output current for the circuit in Figure 1. At very low load currents, <10µA, the effect of the input quiescent current can be seen as a positive offset in the input current. For higher load currents, >100µA, this effect is minimal and the input current is approximately equal to the output current. The expression for the input current may be approximated as:

$$I_{IN} = \frac{I_{OUT}}{\eta} \bullet \frac{V_{OUT}^+ | V_{OUT}^- |}{V_{IN}} + 2 \bullet I_Q$$

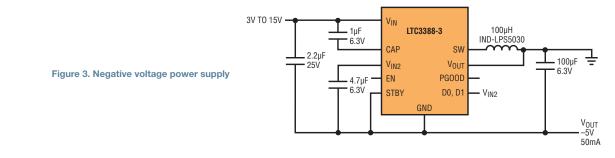
n = EFFICIENCY

NEGATIVE VOLTAGE SUPPLY

Figure 3 shows the buck-boost configuration creating a negative output voltage rail. In this configuration the input voltage needs only be above the UVLO voltage of 2.5V (typ) to start the regulator. The -5V curve in Figure 2 applies here with a 12V input, as in the previous circuit.

CONCLUSION

An easy-to-implement split-voltage power supply using the LTC3388 yields a low quiescent current, high efficiency solution for powering low current analog circuits that need a virtual ground output. The output voltage of each device is digitally programmable to four output voltages from 1.2v to 5.0v and will support a load current up to 50mA. Each regulator requires only four external capacitors and one inductor, covering minimal board real estate. A PGOOD status pin is provided to indicate when the output is within regulation. The LTC3388-1 and the LTC3388-3 are available in a 10-lead MSE or a 3mm × 3mm DFN package.



Product Briefs

RF-TO-DIGITAL µMODULE RECEIVERS REDUCE SIZE, COST AND TIME-TO-MARKET FOR BASE STATION DESIGNS

The LTM[®]9004 and LTM9005 are two breakthrough RF-to-digital µModule receivers that integrate the key components for 3G and 4G base station receivers (WCDMA, TD-SCDMA, LTE, etc.) and smart antenna WiMAX base stations. The integrated µModule receivers offer a dramatic reduction in board space, integrating the RF mixer/demodulator, amplifiers, passive filtering and 14-bit, 125Msps ADCs in one conveniently small package. The LTM9004 implements a direct conversion architecture with an I/Q demodulator, lowpass filter and a dual ADC. The LTM9005 implements an IF-sampling architecture with a downconverting mixer, saw filter and a single ADC. This high level of integration enables smaller boards or higher channel count systems, alleviating issues related to separation and routing of signals, while providing a significant reduction in design and debug time. These receivers harness years of signal chain design experience and offer it in an easy-to-use 22mm × 15mm µModule package.

Cellular service providers are under intense pressure to reduce capital (CAPEX) and operating (OPEX) expenses. Supporting trends include the need for smaller, lighter, lower power base stations such as remote radio heads (RRH) that can be mounted on the tower with the antenna; and high density, high channelcount macrocell base stations with higher efficiency; and the use of small, digital repeaters. These µModule receivers address these trends directly. At only 25% of the board space area of discrete designs, the LTM9004 and LTM9005 save critical space and also reduce the time and effort required for optimizing the design and layout of dozens of high frequency components. This leads to lower development costs, fewer components to source and stock, and faster time to market.

Two receiver architectures dominate base station designs: direct conversion and IF-sampling. Direct conversion demodulates the RF signal and downconverts to DC (OMHz in the frequency domain). This simplifies the filter, allowing lowpass filters with a 10MHz cutoff (20MHz signal bandwidth). The LTM9004 implements this architecture. Other filter options are available for different signal bandwidths. IF-sampling downconverts to an intermediate frequency (IF), 140MHz in this case, and the signal is demodulated in the digital domain. The 20MHz signal filtering is done with a surface acoustical wave (SAW) filter integrated in the LTM9005. Other filter bandwidths are available.

The LTM9004 and LTM9005 are packaged in a space-saving 22mm × 15mm LGA package, utilizing a multilayer substrate that shields sensitive analog lines from the digital traces to minimize digital feedback. Supply and reference bypass capacitance is placed inside the μ Module package, tightly coupled to the die, providing a space, cost and performance advantage over traditional packaging.

µMODULE BATTERY CHARGERS WITH ACTIVE CURRENT LIMIT DELIVER 2A FROM UP TO 32V_{IN}

The LTM8061 and LTM8062 are the first devices in a new family of complete system-in-a-package µModule chargers, supporting an output charge current up to 2A. Both parts provide a complete, efficient 1MHz switching step-down charger solution with just one input capacitor. The LTM8061 features active input current management to protect against supply rail droop, while providing maximum charge current to the load. The LTM8062 actively manages the output charge current to maximize the power sourced from a solar cell following maximum peak power tracking (MPPT) principles. The LTM8061 and LTM8062 operate from an input voltage range of 4.95V to 32V with support for preconditioning, constantcurrent and constant voltage mode operation. A 0.5% and 0.75% accurate float voltage, respectively, ensures maximum energy storage at charge termination set by a minimum current threshold detection or adjustable internal timeout.

The LTM8061 is specifically targeted for charging Li-ion or Li-polymer batteries with float voltages of 4.1V, 4.2V, 8.2V and 8.4V. An externally adjustable float voltage allows the LTM8062 to support charging of single-and multicell Li-ion, Li-polymer, lithium iron phosphate (LiFePO⁴) and sealed lead acid (SLA) batteries up to 14.4V.

To maintain the battery at full charge, the LTM8061 and LTM8062 automatically initiate a recharge cycle once the battery voltage drops to 2.5% below the float voltage. Safety features include bad-battery detection and NTC resistor input with fault indicator suitable for use with a LED. An internal input reverse voltage blocking diode is available to prevent leakage current from the battery when the power source is not present. The LTM8061 and LTM8062 are available in an RoHs compliant 9mm × 15mm × 4.32mm LGA package.

60V BATTERY CHARGING CONTROLLER AND POWER MANAGER

The LTC4000 is a high voltage controller and power manager that converts virtually any externally compensated DC/DC power supply into a full-featured battery charger. The LTC4000 is capable of driving typical DC/DC converter topologies, including buck, boost, buck-boost, SEPIC and flyback. The device offers precision input and charge current regulation and operates across a wide 3V to 60V input and output

$({\tt LTC2195}, {\it continued from page 43})$

digital feedback can be found in the video "Reduce Digital Feedback in High Speed Data Conversion Systems - LTC2261" at www.linear.com. There are also pincompatible 14- and 12-bit versions of the dual LTC2185 that also provide excellent performance, and extremely low power consumption for high speed ADCs. The complete family can be seen in Table 1.

(LT3694, continued from page 33) allowable step-down range due to the minimum on and off time constraints.

This brings us to the difference between the LT3694 and the LT3694-1. The LT3694 switching frequency can be synchronized to an external clock by connecting it to the SYNC pin. The resistor on the RT pin should be set provide a free running frequency 20% below the sync frequency. The LT3694-1 replaces the SYNC pin with a CLKOUT pin, allowing the LT3694-1 to be used as the master voltage range—compatible with a variety of different input voltage sources, battery stacks and chemistries. Typical applications include high power battery charger systems, high performance portable instruments, battery back-up systems, industrial battery-equipped devices and notebook/sub-notebook computers.

The LTC4000 features an intelligent PowerPath[™] topology that preferentially provides power to the system load when input power is limited. The LTC4000 controls external PFETs to provide low loss reverse current protection, efficient charging and discharging of the battery and instant-on operation to ensure that system power is available at plug-in even with a dead or deeply discharged battery. External sense resistors and precision sensing enable accurate currents at high efficiency, allowing the LTC4000 to work with converters that span the power range from milliwatts to kilowatts.

The LTC4000's full-featured controller charges a variety of battery chemistries including lithium-ion/polymer/phosphate, sealed lead acid (SLA), and nickel-based. The device also provides charge status indicators through its FLT and CHRG pins. Other features of the battery charger include: ±0.2% programmable float voltage, selectable timer or C/x current termination, temperature-qualified charging using an NTC thermistor, automatic recharge, C/10 trickle charge for deeply discharged cells and bad battery detection.

The LTC4000 is housed in a low profile (0.75mm) 28-pin 4mm × 5mm QFN package and a 28-lead ssop package.

CONCLUSION

The LTC2195 is the perfect ADC for powerconscious, high resolution sensor applications, while the LTC6406 is a good match as a driver amplifier—it does not compromise the performance of the LTC2195 and its power requirements are also low. Data sheet performance of the ADC can be easily achieved by using a relatively low order

clock for synchronizing other switching regulators. The CLKOUT produces a clock signal running at ~50% duty cycle.

TRIPLE-OUTPUT CONVERTER WITH VOLTAGE TRACKING

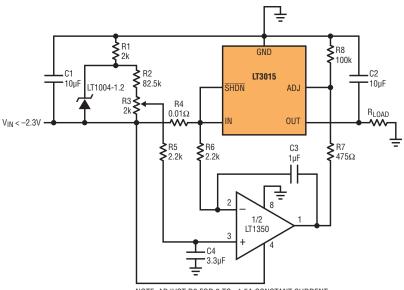
Figure 1 shows a wide input range, 6.3V to 36V, converter that generates three outputs: 5V, 3.3V and 2.5V. The outputs track ratiometrically, set via a common TRK/SS connection. Figure 2 shows the start-up waveforms of the three outputs along with the enable signal. Figure 3 shows the switching regulator efficiency at different input voltages. filter to reduce the wideband noise of the amplifier. The pairing of the LTC2195 and the LTC6406 is the ideal combination for any portable image sensor application, combining excellent performance with low power consumption. For more information about the LTC2195 family and the LTC6406 visit www.linear.com.

CONCLUSION

The LT3694/LT3694-1 offers robust, compact power supply solutions by squeezing three regulators into a tiny 4mm × 5mm QFN or a 20-lead TSSOP package. One regulator is an efficient switching regulator and the other two are low noise, low dropout linear regulators. Just a few small external components are needed to create an extremely compact triple output solution.

ADJUSTABLE CURRENT SINK

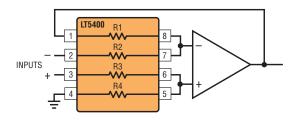
The LT3015 is a low noise, low dropout, negative linear regulator with fast transient response. The device supplies up to 1.5A of output current at a typical dropout voltage of 310mV. With minimal external circuitry, the LT3015 can be configured as an adjustable current sink. www.linear.com/3015



NOTE: ADJUST R3 FOR 0 TO -1.5A CONSTANT CURRENT

DIFFERENCE AMPLIFIER

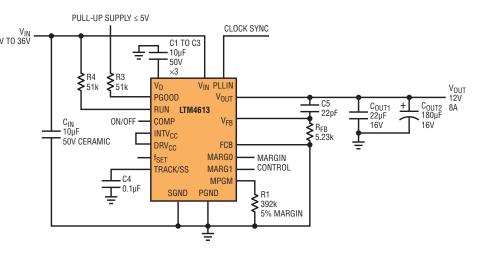
The LT5400 is a quad resistor network with excellent matching specifications over the entire temperature range. These resistor networks provide precise ratiometric stability required in highly accurate difference amplifiers, voltage references and bridge circuits. www.linear.com/5400



THIS CIRCUIT CAN BE IMPLEMENTED USING ANY LT5400 RESISTOR OPTION

EN55022B COMPLIANT 36V $_{\rm IN},$ 15V $_{\rm OUT},$ 8A, DC/DC $\mu MODULE$ REGULATOR

V_{IN} The LTM4613 is a complete, ultralow noise, 8A switch mode ^{22V TO 36V} DC/DC power supply. Included in the package are the switching controller, power FETs, inductor and all support components. Only bulk input and output capacitors are needed to finis h the design. The onboard input filter and noise cancellation circuits achieve low noise coupling, effectively reducing the electromagnetic interference (EMI). Furthermore, the part can be synchronized with an external clock to reduce undesirable frequency harmonics. www.linear.com/4613



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