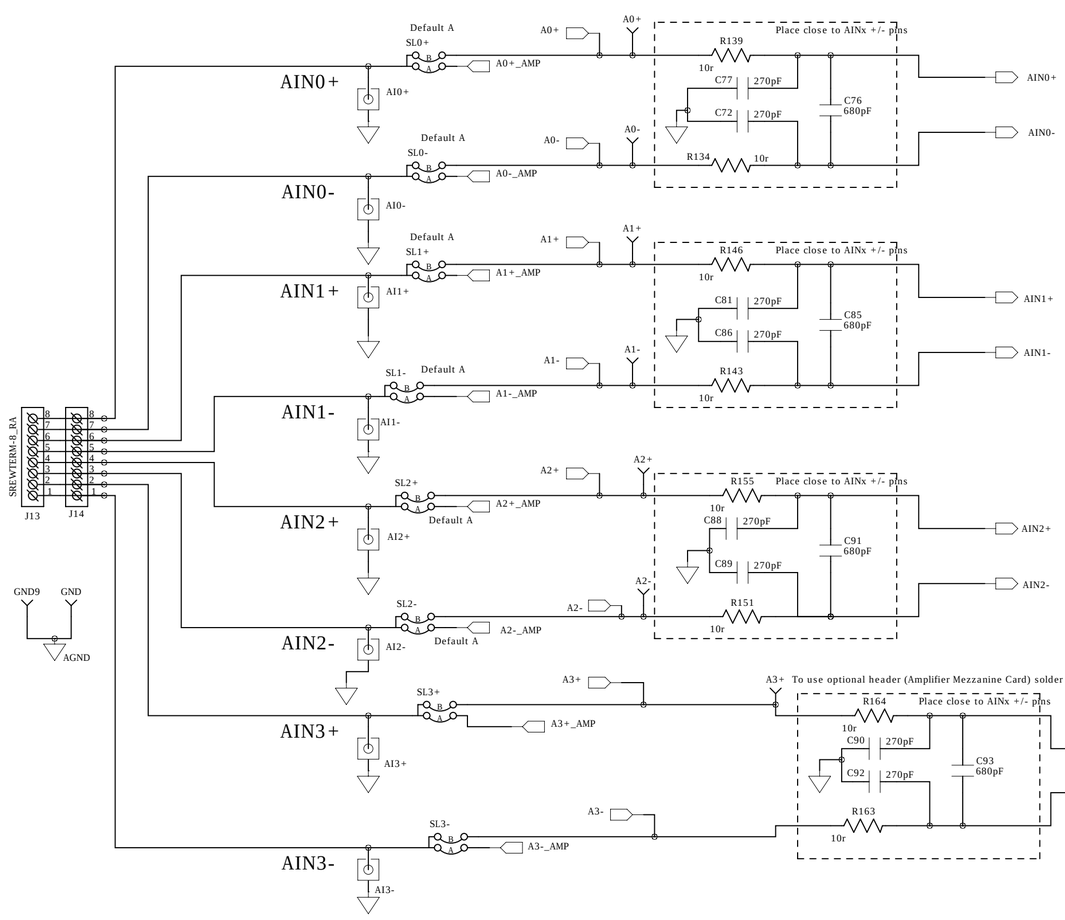
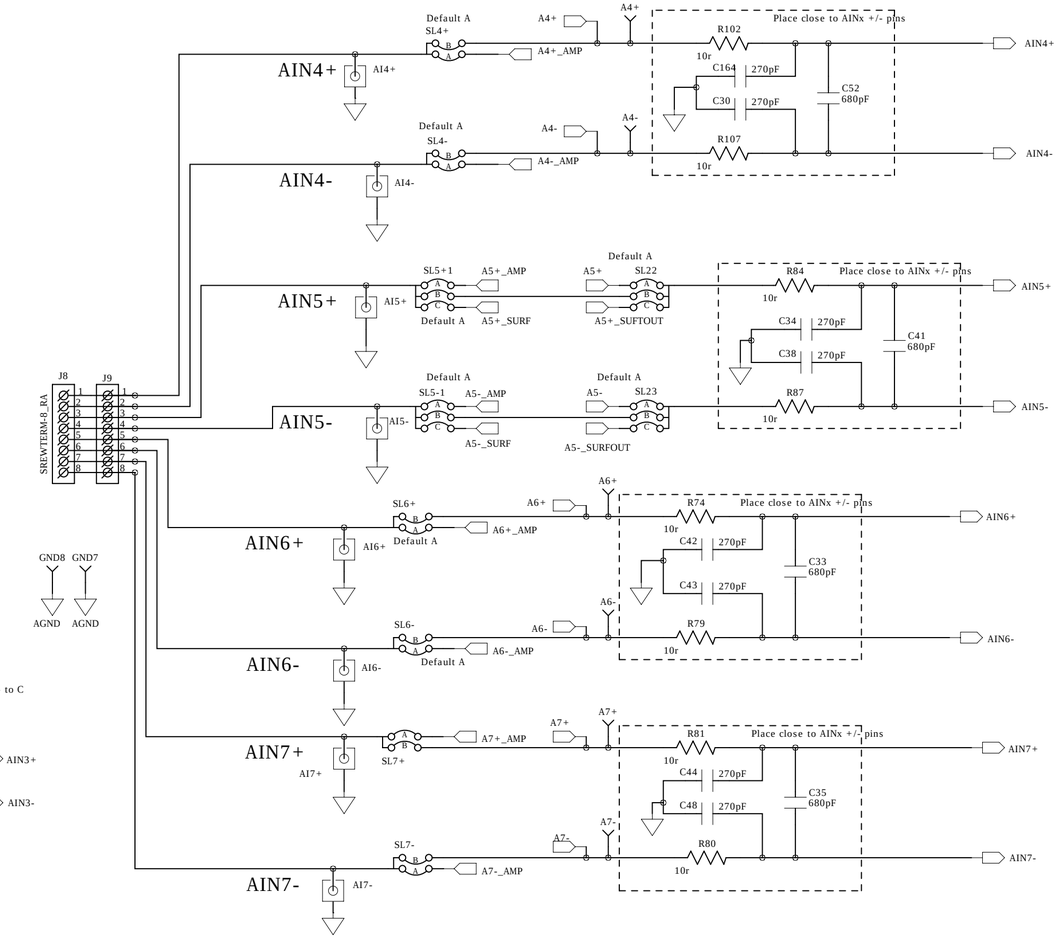
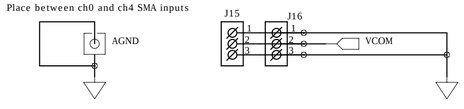
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Analog Inputs

Solder Link Connections:
A: Buffered input (Default)
B: Direct to ADC Input pins
C: Route through 'Amplifier Mezzanine Card' for Alternative Amplifier Evaluation (Ch 5 ONLY)







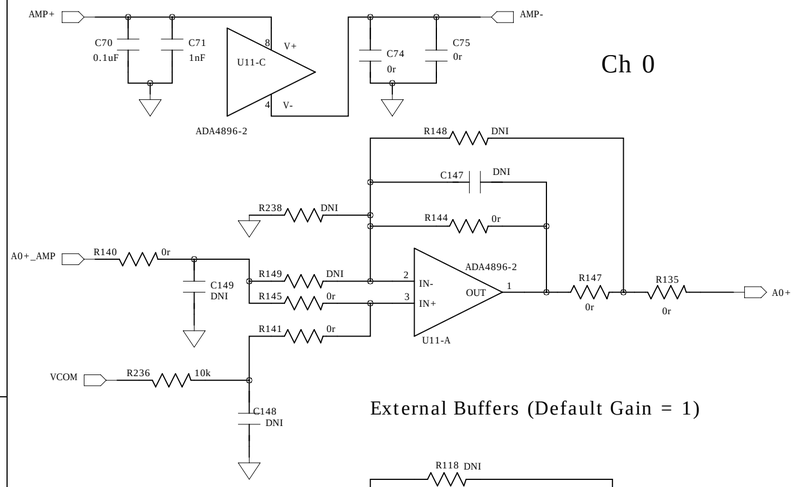
Place SL20,SL21 after amplifier and surfboard

Close to RC input network

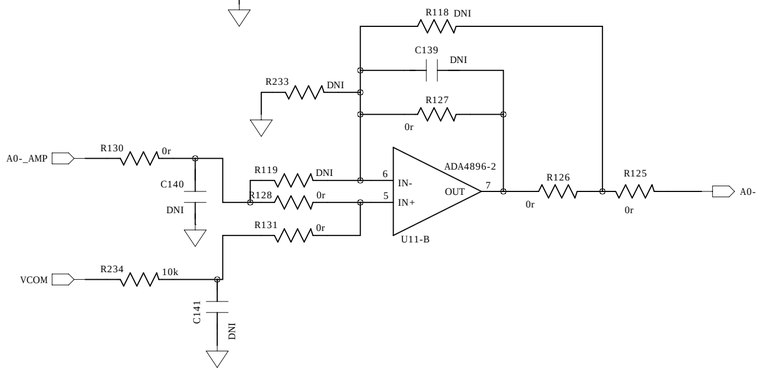
DRAWN: Rob Finnerty	DATED:	COMPANY: Analog Devices	
CHECKED: Martin Madden	DATED:	TITLE: EVAL-AD7768FMCZ	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 02-0	REV: A
		SCALE: <Scale>	SHEET: 1 OF 7

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

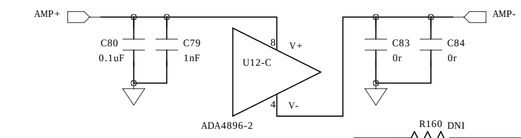
Ch 0

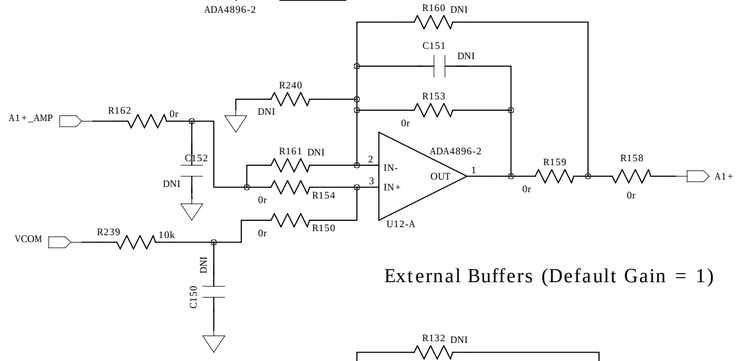


External Buffers (Default Gain = 1)



Ch 1





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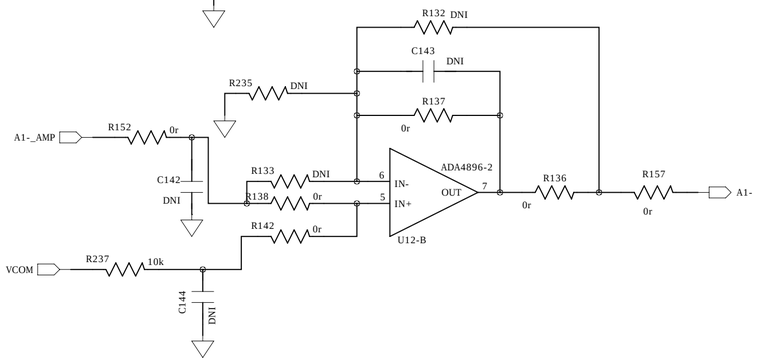
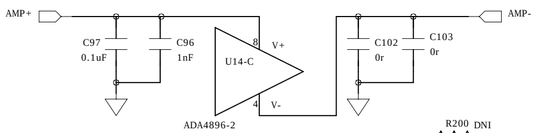
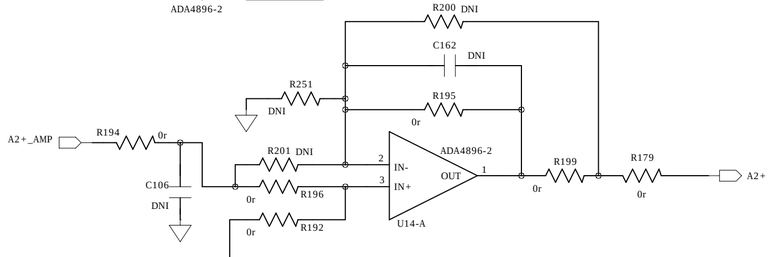




Ch 2



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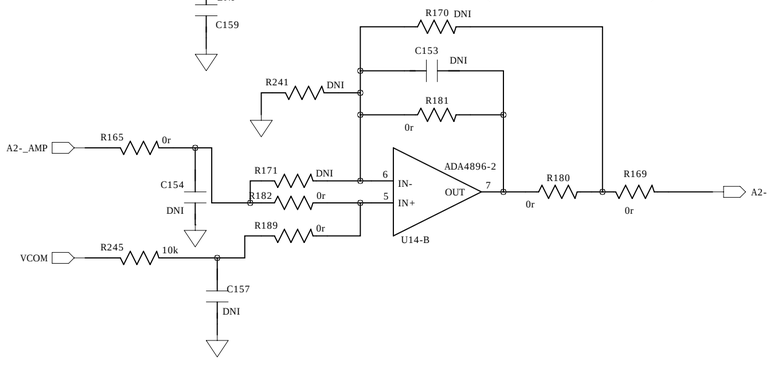
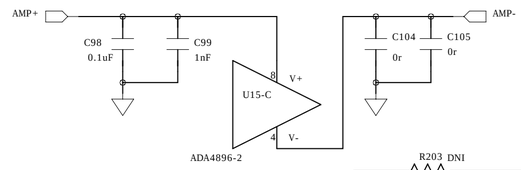
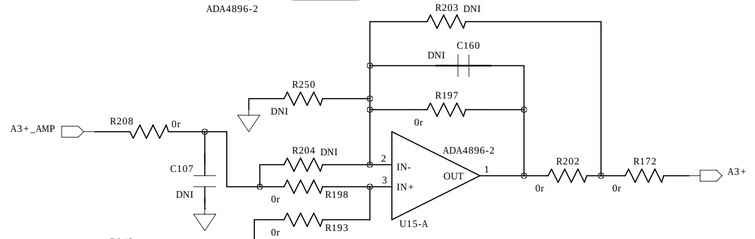
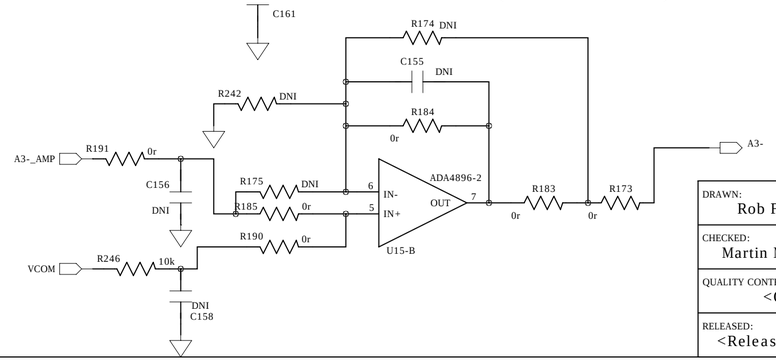


Ch 3





External Buffers (Default Gain = 1)



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CHECKED: Martin Madden	DATED: 24/11/2014	TITLE: EVAL-AD7768FMCZ	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 02-0	REV: A
		SCALE: <Scale>	SHEET: 2 OF 7

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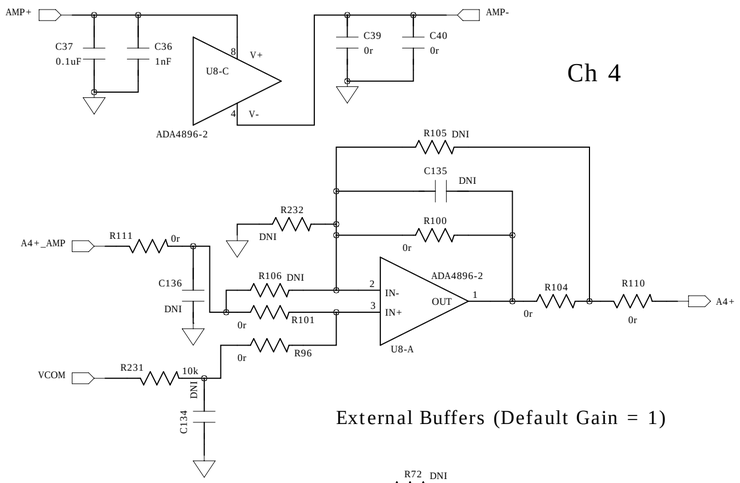
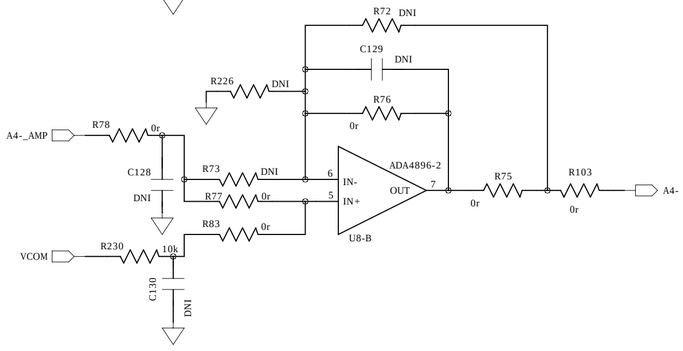
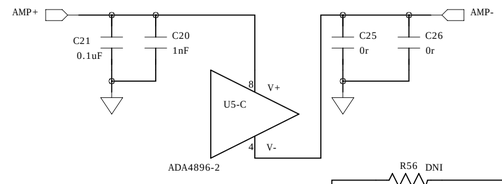
Ch 4

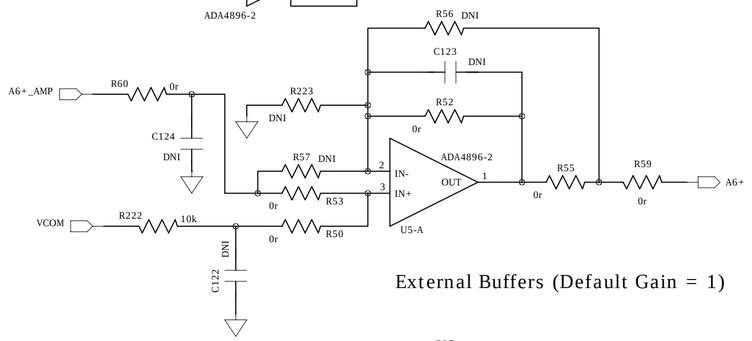


External Buffers (Default Gain = 1)

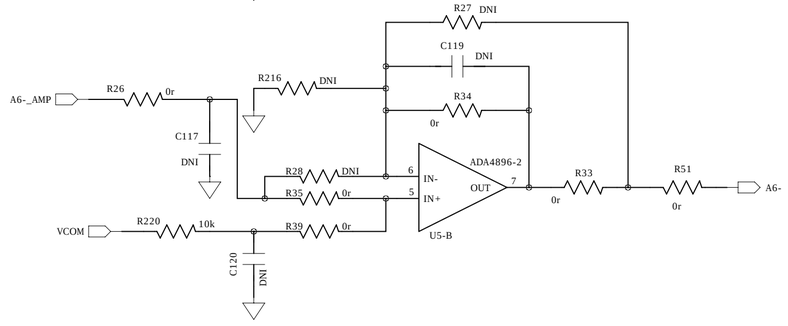


Ch 6

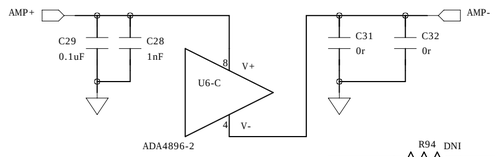


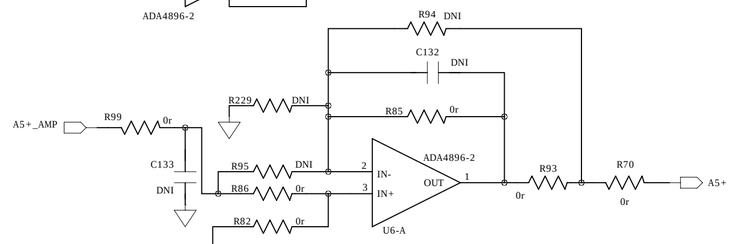


External Buffers (Default Gain = 1)



Ch 5





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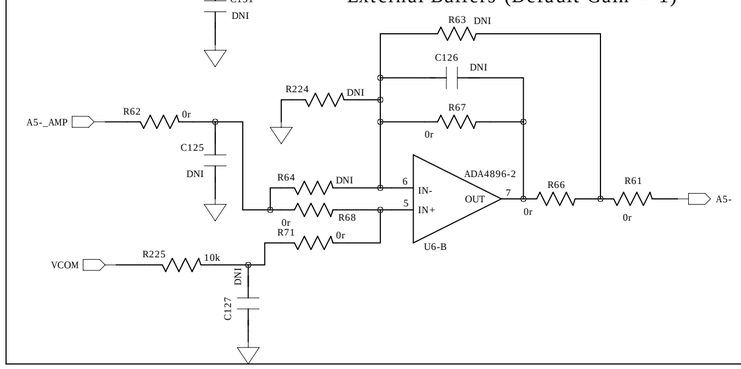
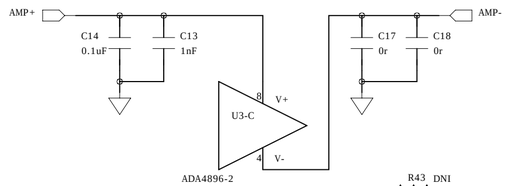
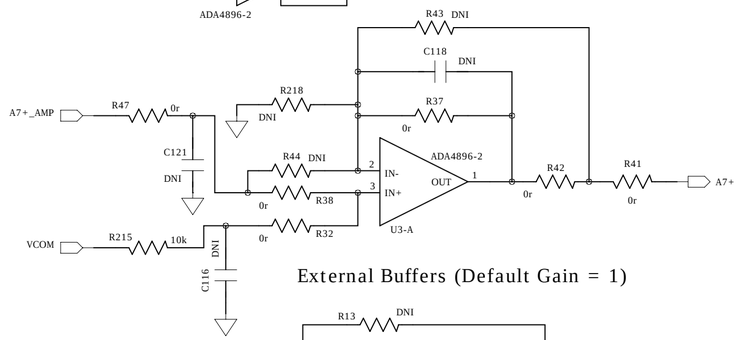
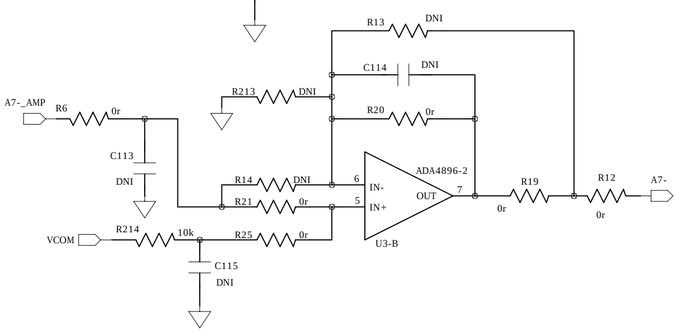


Ch 7





External Buffers (Default Gain = 1)



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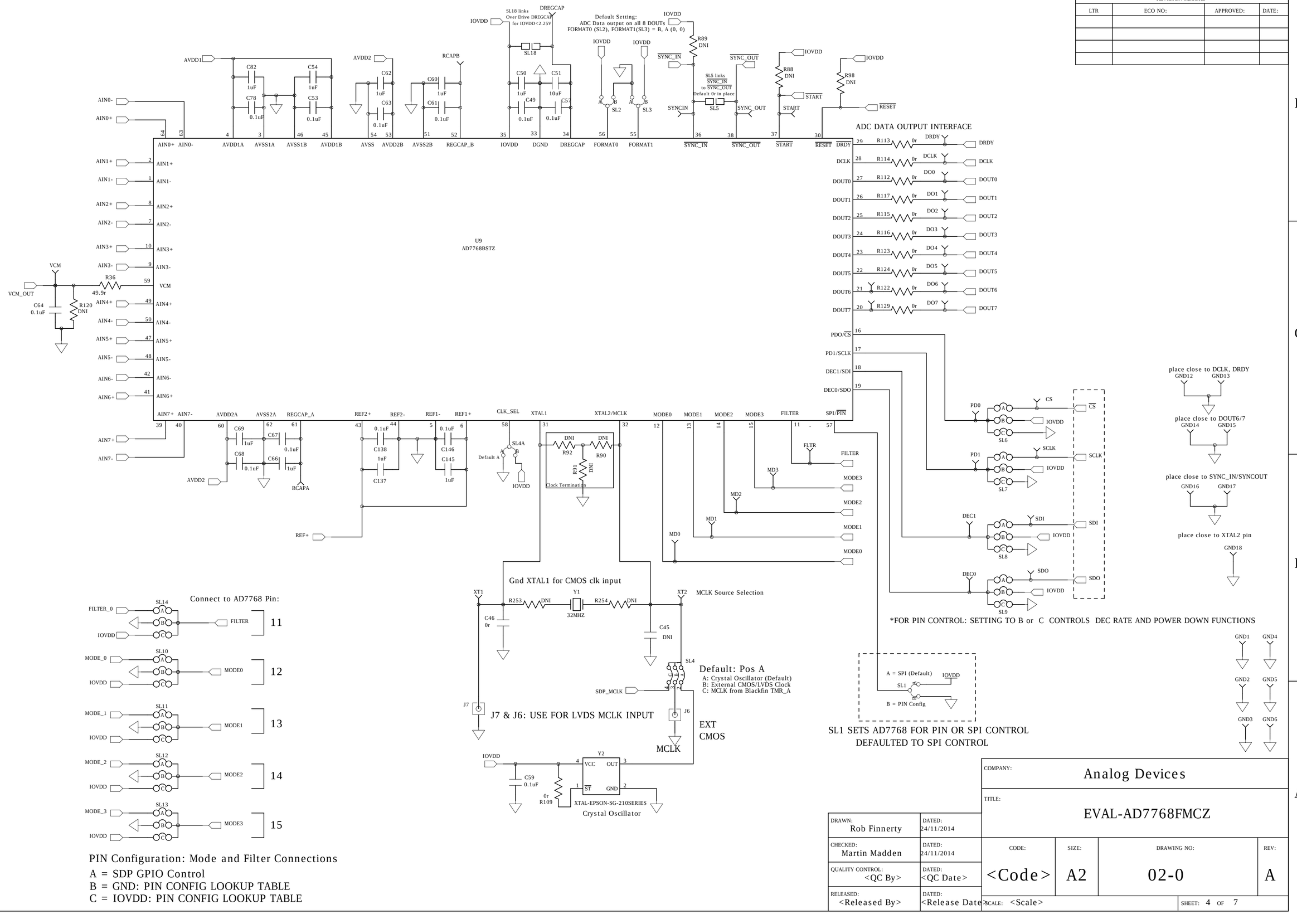
CHECKED: Martin Madden	DATED: 24/11/2014	TITLE: EVAL-AD7768FMCZ	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 02-0	REV: A
		SCALE: <Scale>	SHEET: 3 OF 7

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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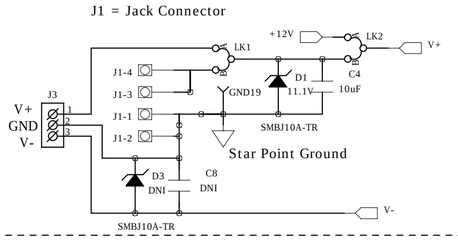
		SCALE: <Scale>	SHEET: 4 OF 7

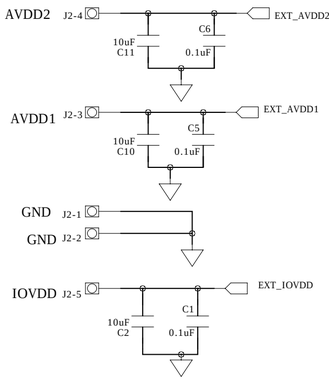
6	5	4	3	2	1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

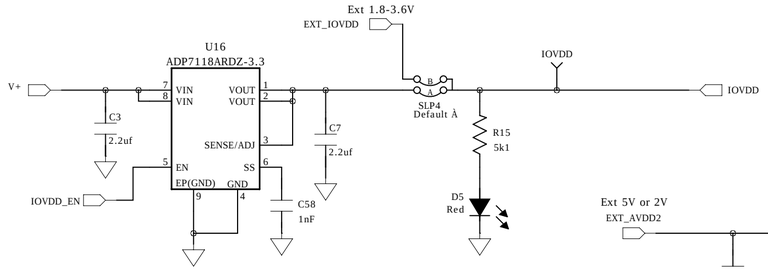
POWER SUPPLY : Jack or Bench Connection

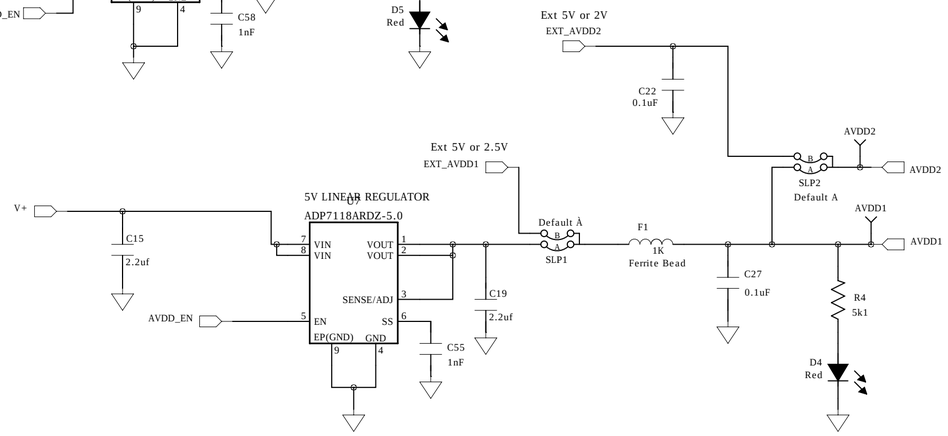


External supply: Stand-Alone Operation

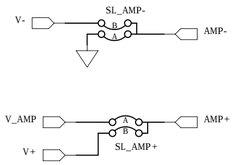


5V, 1.8V Regulators

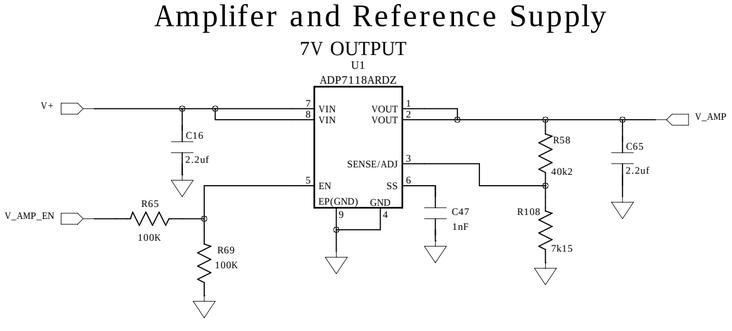




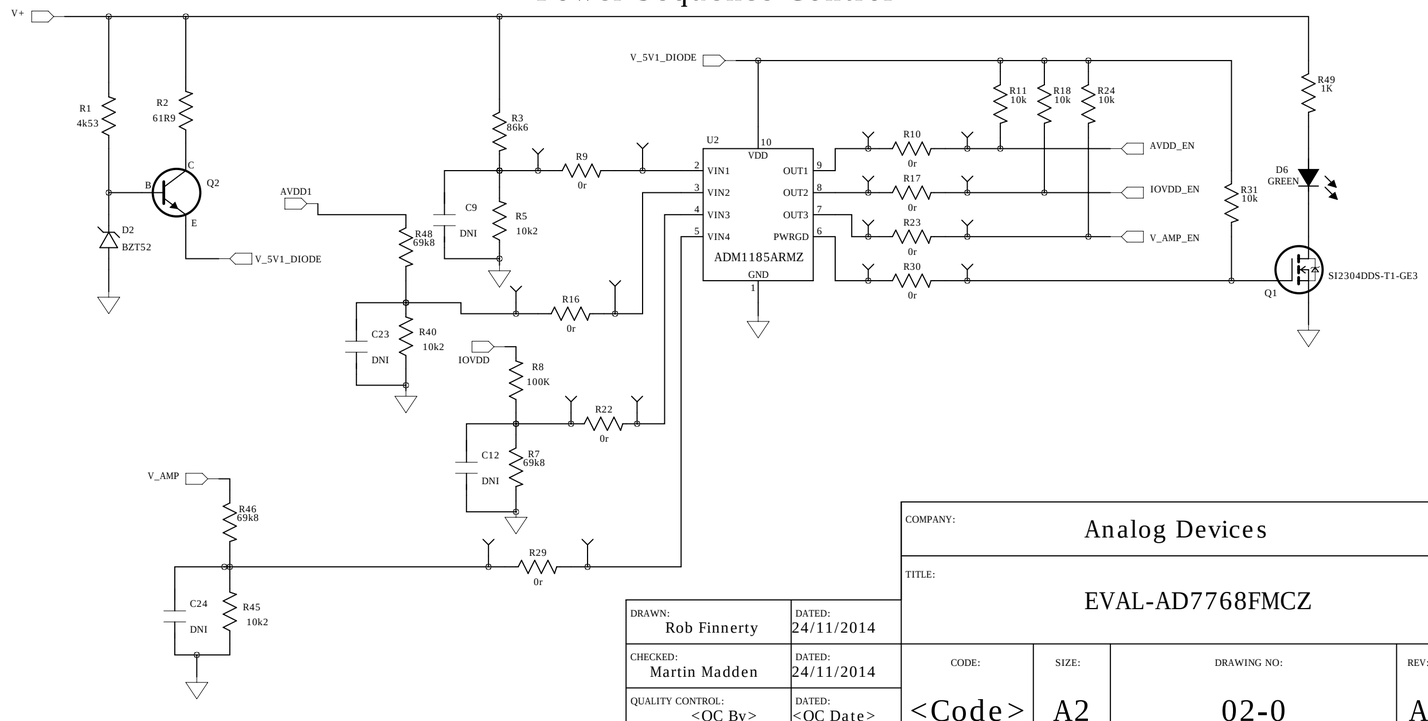
Select Amplifier Rails



Amplifer and Reference Supply



Power Sequence Control



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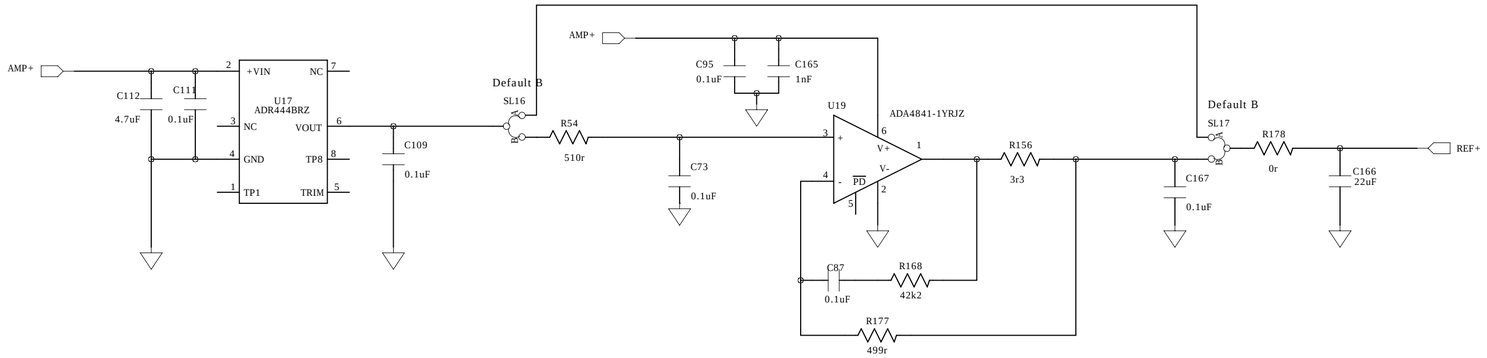
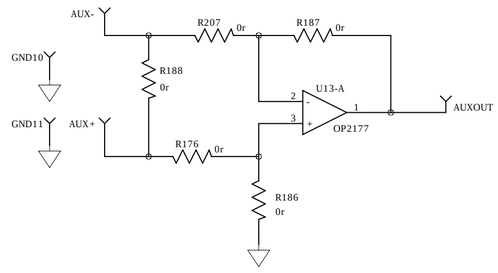
		SCALE: <Scale>	SHEET: 5 OF 7

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

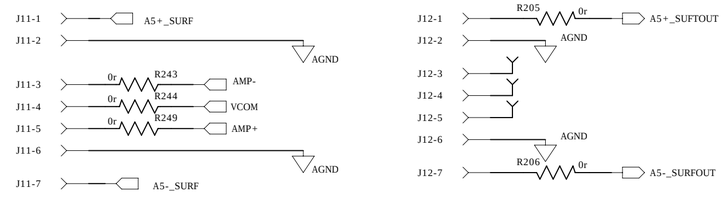
Precision Voltage Reference

REFERENCE BUFFER ADA4841-1

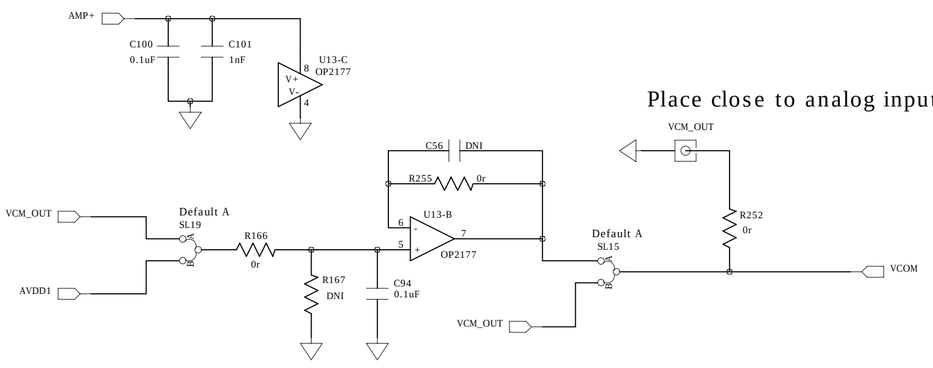




OPTIONAL HEADER CONNECTOR (Amplifier Mezzanine Card for Ch5)



Creating VCOM - Common Mode for ADC Analog Inputs



COMPANY: Analog Devices			
TITLE: EVAL-AD7768FMCZ			
DRAWN: Rob Finnerty	DATED: 24/11/2014	CODE: <Code>	SIZE: A2
CHECKED: Martin Madden	DATED: 24/11/2014	DRAWING NO: 02-0	REV: A
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 6 OF 7

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FMC-LPC Connector

P1-A
ASP-134604-01

C1			GND
C2			No Connect
C3			No Connect
C4			GND
C5			GND
C6			No Connect
C7			No Connect
C8			GND
C9			GND
C10	AK20	LA06_P	
C11	AK21	LA06_N	
C12			GND
C13			GND
C14	AJ24	LA10_P	
C15	AK25	LA10_N	
C16			GND
C17			GND
C18	AD21	LA14_P	
C19	AE21	LA14_N	
C20			GND
C21			GND
C22	AD27	LA18_P_CC	
C23	AD28	LA18_N_CC	
C24			GND
C25			GND
C26	AJ28	LA27_P	
C27	AJ29	LA27_N	
C28			GND
C29			GND
C30			SCL
C31			SDA
C32			GND
C33			GND
C34			GA0
C35			12P0V
C36			GND
C37			12P0V
C38			GND
C39			3P3V
C40			GND

RESET
RESET
DOUT1
FILTER_0
MODE_0
12V
+12V
GA0
3P3VAUX
U10
VCC
GA1
GA0
E0
E1
E2
SDA
SCL
WP
VSS
M24C02-WDW6TP
I2C address set by controller board
EEPROM required in VITA standard
I2C line pull-up resistors on FPGA board

P1-B
ASP-134604-01

D1			PG_C2M
D2			GND
D3			GND
D4			No Connect
D5			No Connect
D6			GND
D7			GND
D8	AE23	LA01_P_CC	
D9	AF23	LA01_N_CC	
D10			GND
D11	AG22	LA05_P	
D12	AH22	LA05_N	
D13			GND
D14	AK23	LA09_P	
D15	AK24	LA09_N	
D16			GND
D17	AB24	LA13_P	
D18	AC25	LA13_N	
D19			GND
D20	AB27	LA17_P_CC	
D21	AC27	LA17_N_CC	
D22			GND
D23	AH26	LA23_P	
D24	AH27	LA23_N	
D25			GND
D26	AK29	LA26_P	
D27	AK30	LA26_N	
D28			GND
D29			TCK
D30			TDI
D31			TDO
D32			3P3VAUX
D33			TMS
D34			TRST_L
D35			GA1
D36			3P3V
D37			GND
D38			3P3V
D39			GND
D40			3P3V

SCLK
SDP_MCLK
R97
0r
CS
SYNC_OUT
DOUT6
DOUT7
3P3VAUX
GA1

If Eval board does not use JTAG TDI and TDO then they must be shorted together (as shown) so as not to break JTAG chain

P1-C
ASP-134604-01

G1			GND
G2			CLK1_M2C_P
G3			CLK1_M2C_N
G4			GND
G5			GND
G6	AD23	LA00_P_CC	
G7	AE24	LA00_N_CC	
G8			GND
G9	AG20	LA03_P	
G10	AH20	LA03_N	
G11			GND
G12	AJ22	LA08_P	
G13	AJ23	LA08_N	
G14			GND
G15	AA20	LA12_P	
G16	AB20	LA12_N	
G17			GND
G18	AC22	LA16_P	
G19	AD22	LA16_N	
G20			GND
G21	AF26	LA20_P	
G22	AF27	LA20_N	
G23			GND
G24	AJ27	LA22_P	
G25	AK28	LA22_N	
G26			GND
G27	AC26	LA25_P	
G28	AD26	LA25_N	
G29			GND
G30	AE28	LA29_P	
G31	AF28	LA29_N	
G32			GND
G33	AD29	LA31_P	
G34	AE29	LA31_N	
G35			GND
G36	AC29	LA33_P	
G37	AC30	LA33_N	
G38			GND
G39			VADJ
G40			GND

DRDY
DOUT0
SDO
START
DOUT4
DOUT5

P1-D
ASP-134604-01
Board present pin

H1			No Connect
H2			PRSNT_M2C_L
H3			GND
H4	AF22	CLK0_M2C_P	
H5	AG23	CLK0_M2C_N	
H6			GND
H7	AF20	LA02_P	
H8	AF21	LA02_N	
H9			GND
H10	AH21	LA04_P	
H11	AJ21	LA04_N	
H12			GND
H13	AG25	LA07_P	
H14	AH25	LA07_N	
H15			GND
H16	AE25	LA11_P	
H17	AF25	LA11_N	
H18			GND
H19	AC24	LA15_P	
H20	AD24	LA15_N	
H21			GND
H22	AJ26	LA19_P	
H23	AK26	LA19_N	
H24			GND
H25	AG27	LA21_P	
H26	AG28	LA21_N	
H27			GND
H28	AG30	LA24_P	
H29	AH30	LA24_N	
H30			GND
H31	AE30	LA28_P	
H32	AF30	LA28_N	
H33			GND
H34	AB29	LA30_P	
H35	AB30	LA30_N	
H36			GND
H37	Y30	LA32_P	
H38	AA30	LA32_N	
H39			GND
H40			VADJ

DCLK
DOUT2
DOUT3
SYNC_IN
SDI
MODE_1
MODE_2
MODE_3

COMPANY:	Analog Devices	
TITLE:	EVAL-AD7768FMCZ	
DRAWN: Rob Finnerty	DATED: 24/11/2014	
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