Quick Start Guide for testing the AD6655 Dual IF Diversity Receiver Customer Evaluation Board Using the FPGA based Capture Board HSC-ADC-EVALCZ

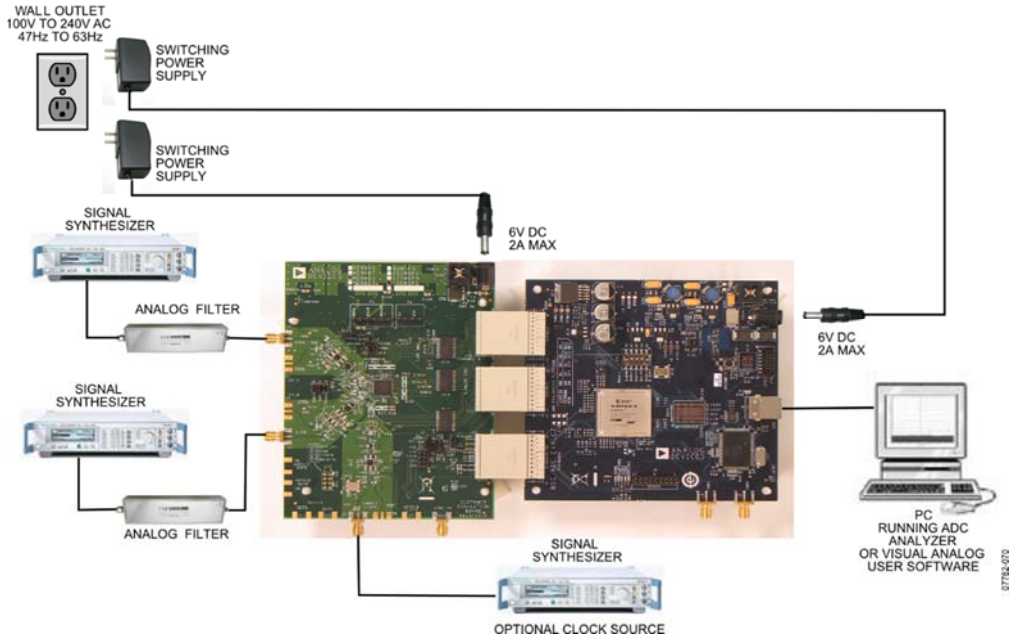

Figure 1: AD6655 Evaluation Board with HSC-ADC_EVALCZ Data Capture Board

Equipment Needed

- ► Analog signal source and anti-aliasing filter
- ► Analog Clock Source
- ► PC
- ► USB 2.0 port recommended (USB 1.1-compatible)
- ► AD6655 evaluation board
- ► HSC-ADC-EVALCZ FPGA Based Data Capture Board

Documents Needed

- ► AD6655 Datasheet
- ► Visual Analog Converter Evaluation Tool User Manual, AN-905
- ► High Speed ADC SPI Control Software User Manual, AN-878
- ► Interfacing to High Speed ADCs via SPI, AN-877

Software Needed

- ► Visual Analog
- ► SPIController

All documents and software are available at http://www.analog.com/fifo.
For any questions please send an email to highspeed.converters@analog.com.

Testing

1. Connect the AD6655 evaluation board and the HSC-ADC-EVALCZ board together as shown in Figure 1.
2. Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the AD6655 board.
3. Make sure a jumper is installed on header J9 at the 2.5V position on the HSC-ADC-EVALCZ evaluation board to set the FPGA I/O voltage to 2.5V. Connect one 6V, 2A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board to the PC with a USB cable. (Connect to J6.)
5. On the ADC evaluation board, make sure that jumpers are installed on headers J18, J9, J19, J5, and J21 for the default setup. Also make sure that jumpers are connected between pins 1-2 on J1 and J2. Refer to Figure 2 for placement of jumpers.

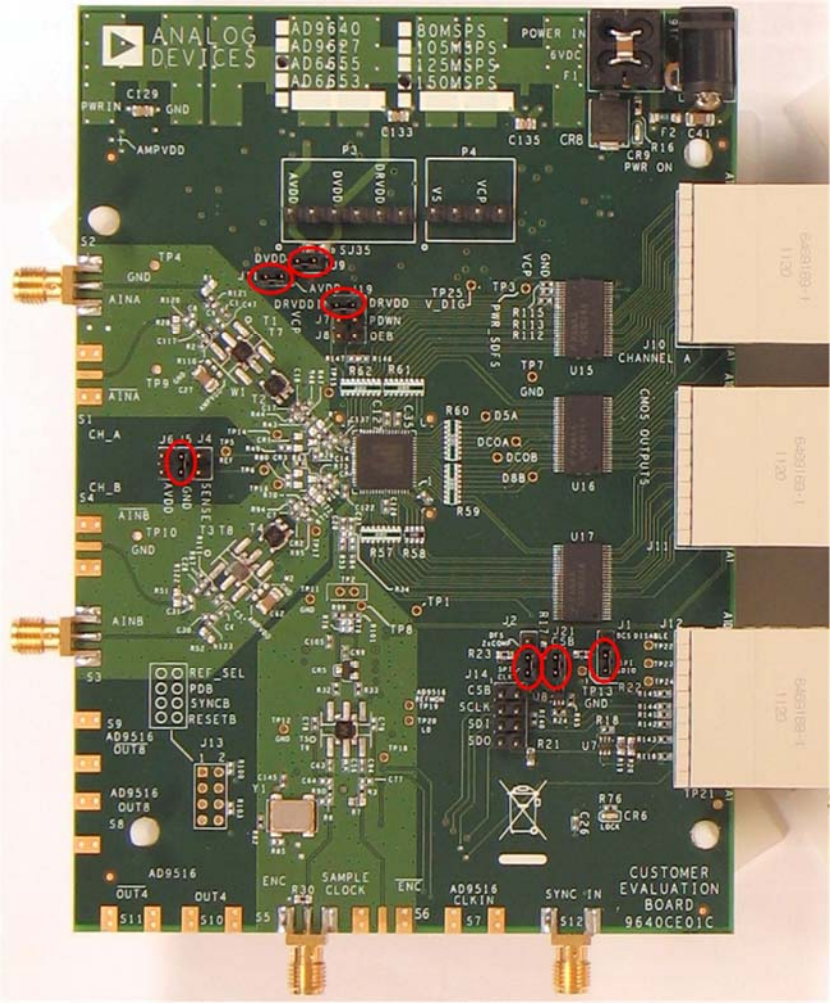

Figure 2. AD6655 Evaluation Board – Jumper Settings

6. On the ADC evaluation board, provide a clean, low jitter clock source to connector S5 at the desired ADC conversion rate. If the AD6655 input clock divider is used provide a clock into connector S5 at the appropriate rate which will be divided to your desired clock rate. The input clock level should be between 10dBm and 14dBm.

7. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at connector S2 (Channel A) and/or S3 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (ADI uses TTE, Allen Avionics, and K&L band-pass filters.) In order for the input level to be near the ADC's full scale, the generator level should be set to 6dBm to 10dBm – this level depends on the input frequency and any losses in bandpass filters.

8. Open Visual Analog on the PC. "AD6655" should be listed in the status bar of the "New Canvas" window (see Figure 3). Select the template that corresponds to the type of testing that you are performing. Select 'Yes' when Visual Analog prompts for programming the FPGA (see Figure 4). The 'DONE' LED should illuminate on the HSC-ADC-EVALCZ board indicating that the FPGA has been correctly programmed. (If Visual Analog does not prompt for programming the FPGA select the ADC Data Capture Settings window and click on the 'Capture Board' tab. In the FPGA box select program to configure the FPGA. – see Figure 5)

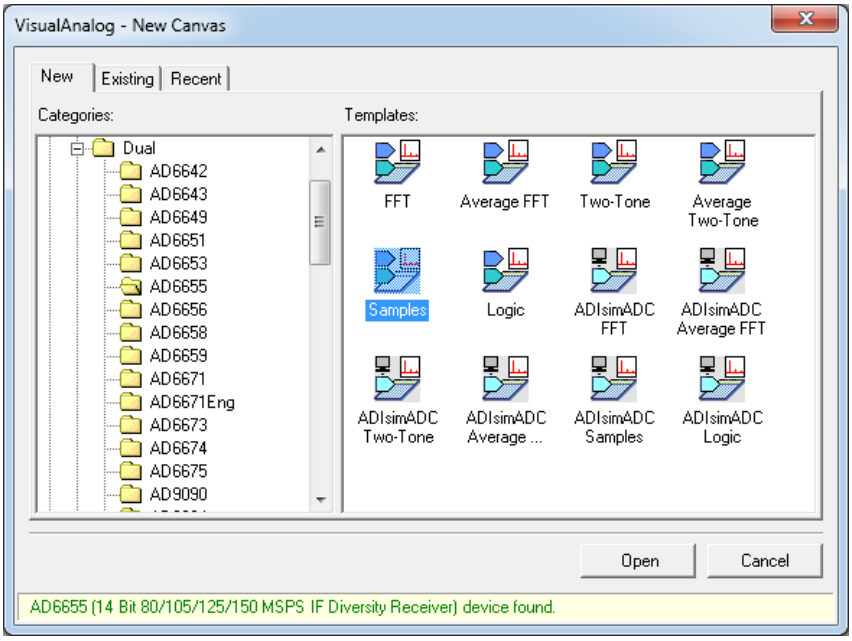

Figure 3. Visual Analog – New Canvas Selection

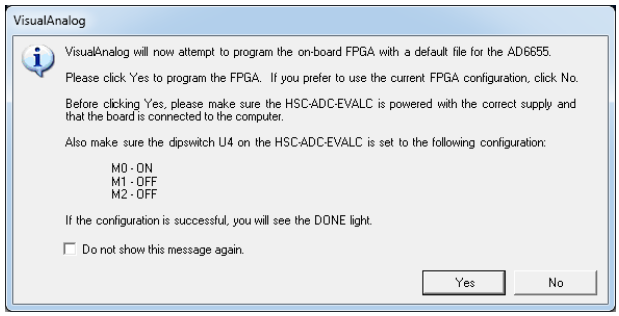

Figure 4. Auto-prompt For Programming FPGA

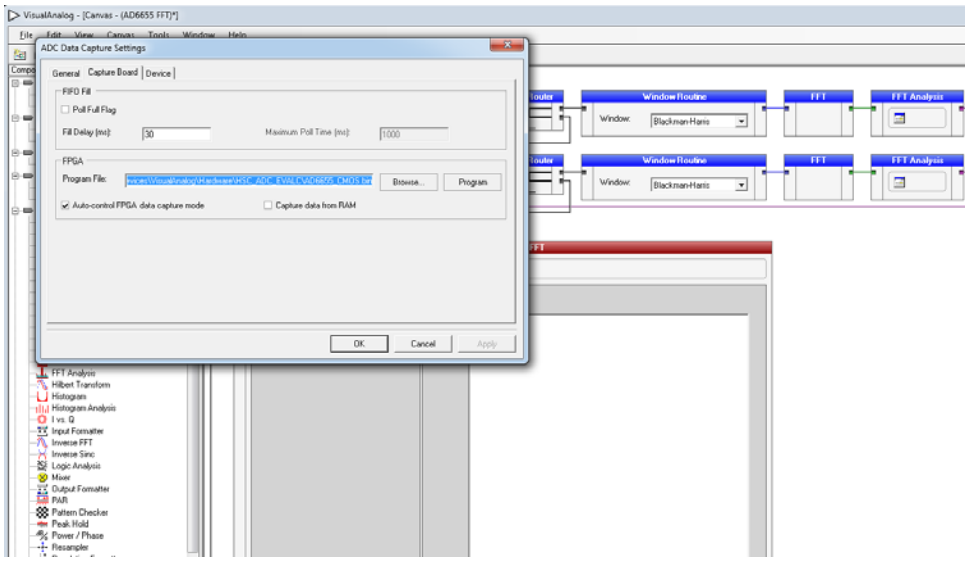

Figure 5. Manual Programming of FPGA (if necessary)

9. Next open the SPI Controller software. If prompted for a configuration file, select the configuration file titled AD6655_14Bit_***XXX***MSspiR03.cfg where ***XXX*** is the speed grade of the AD6655 device that is being used. If not, check the title bar of the window to see which configuration is loaded. If necessary, choose "Cfg Open" from the "File" menu and select one of the configuration files named above. Note that the CHIP ID(1) field may be filled whether the correct SPI Controller configuration file is loaded or not.

10. Click the New DUT button () in SPI Controller.

11. Set the DCO Clk Delay in the OUTPUT DELAY(17) panel on the ADCBase0 tab as shown below. Set the DCO Clk Delay register to '1.7ns' (see Figure 6). This setting aligns the output timing with the input timing on the capture FPGA.

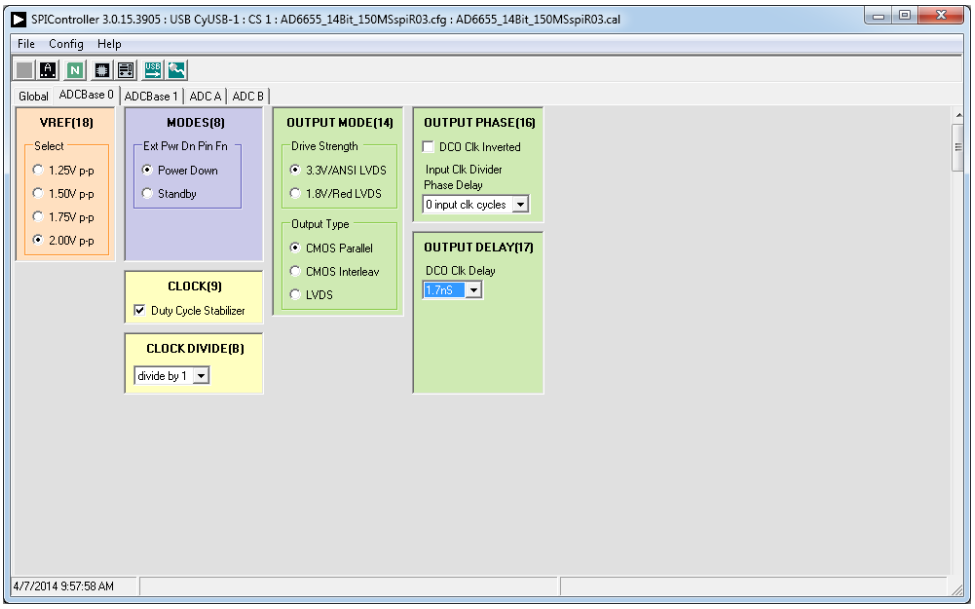

Figure 6. Set Output Delay

12. Click the Run button ( ) in Visual Analog.

13. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the "Fund Power" reading in the left panel of the Visual Analog FFT window. – see Figure 7)

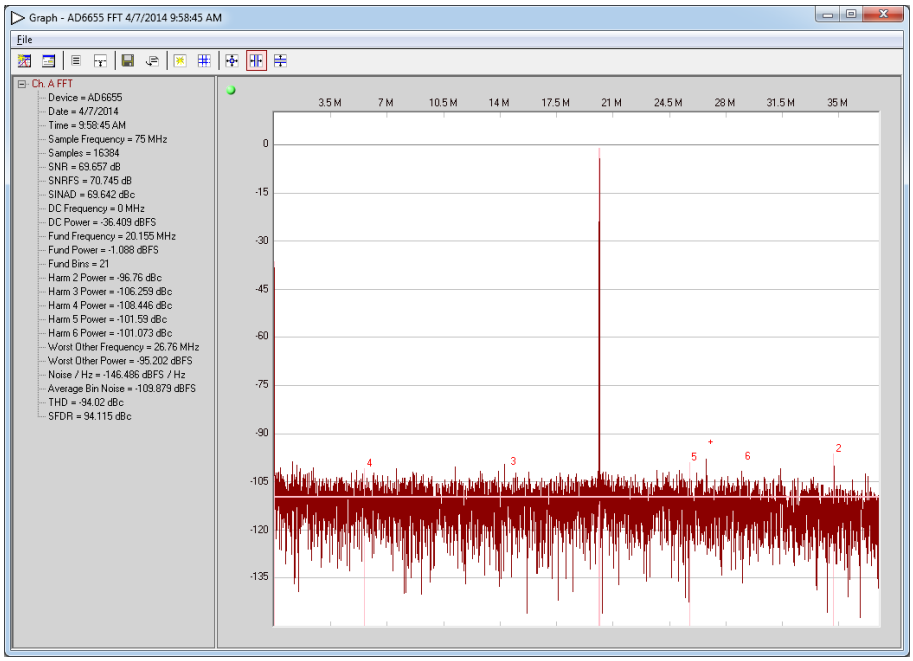

Figure 7. Example FFT from AD6655

14. If desired, click on File>Save Form as in the FFT window to save the FFT plot.

Troubleshooting

► *The FFT plot appears abnormal...*

- ✓ If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure you are not overdriving the ADC. Reduce input level if necessary.
- ✓ In Visual Analog, Click on the Settings button in the "Input Formatter" block. Check that "Number Format" is set to the correct encoding (2's compliment by default).

► *The FFT plot appears normal, but performance is poor.*

- ✓ Make sure you are using an appropriate filter on the analog input.
- ✓ Make sure the signal generators for the clock and the analog input are clean (low phase noise).
- ✓ If you are using non-coherent sampling, change the analog input frequency slightly.
- ✓ Make sure the SPI config file matches the product being evaluated.

► *The FFT window remains blank after the Run button is clicked.*

- ✓ Make sure the evaluation board is securely connected to the HSC-ADC-EVALCZ board
- ✓ Repeat steps 8 through 12.
- ✓ Make sure the FPGA has been programmed by verifying that the 'D6' LED is illuminated on the HSC-ADC-EVALCZ board.
- ✓ Make sure the correct FPGA program was installed.

► *Visual Analog indicates that the "FIFO capture timed out."*

- ✓ Make sure all power and USB connections are secure.
- ✓ Repeat steps 11 through 14.
- ✓ Double check that the encode clock source is present at connector J506.

Revision: 0 April 7, 2014