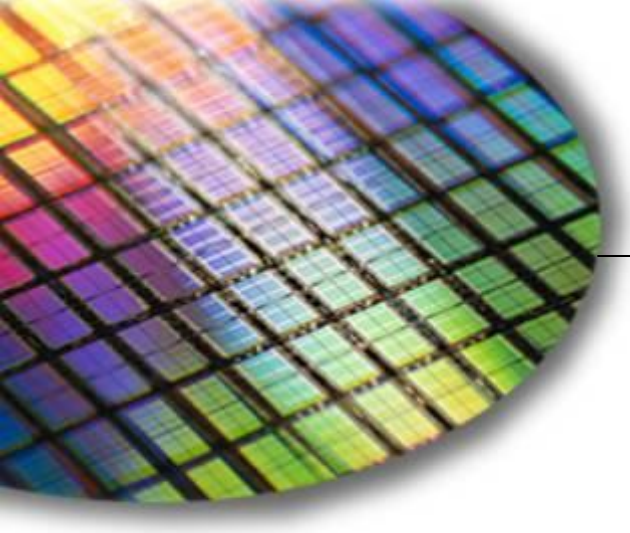


The World Leader in High Performance Signal Processing Solutions

ADV7510 to ADV7511Differences

September, 2010

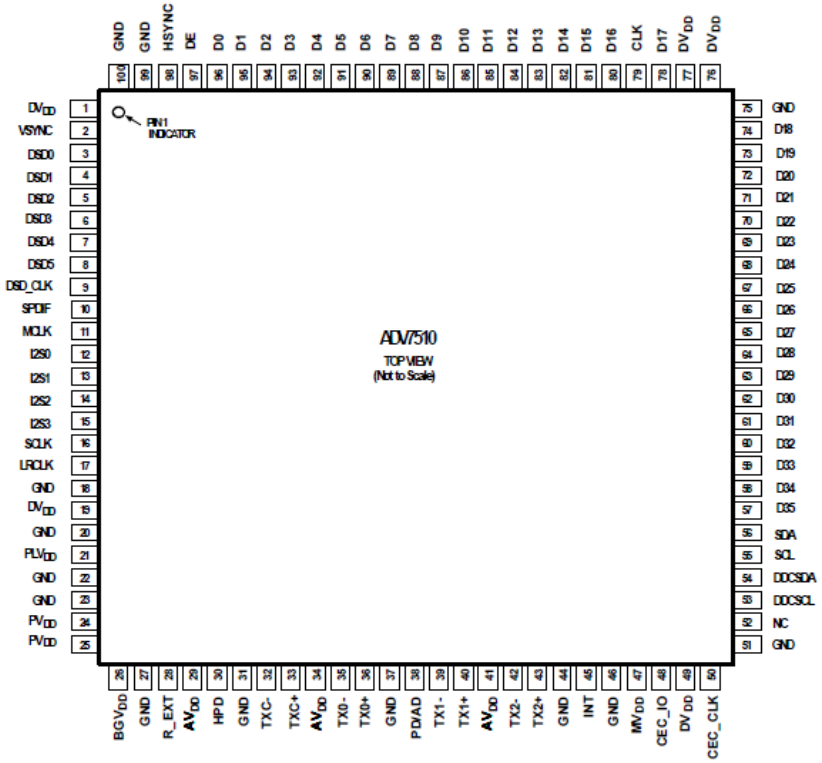
ANALOG DEVICES

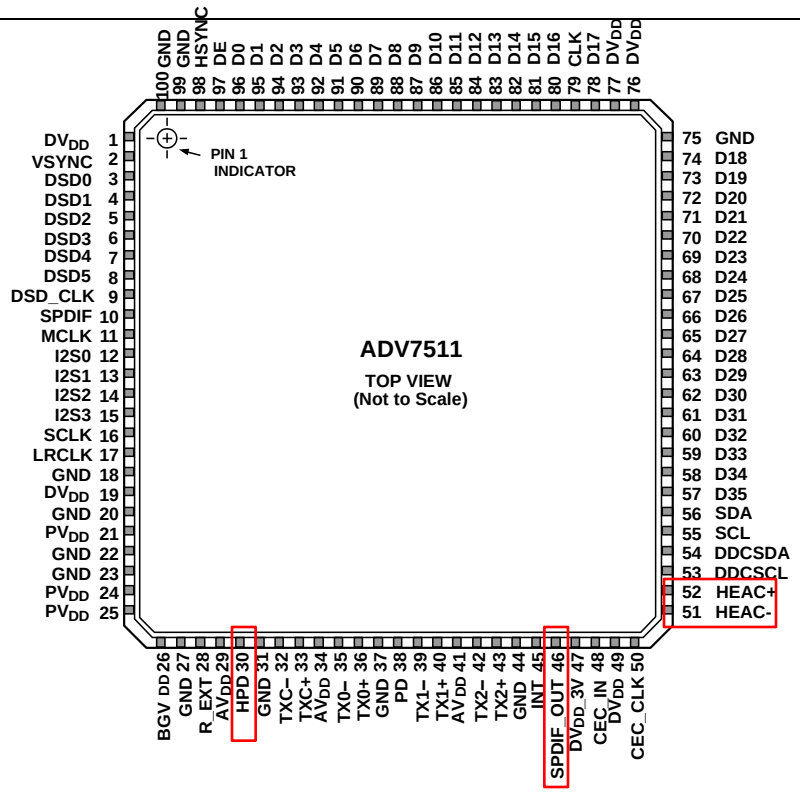
Overview

- Pin Out and other Hardware Changes
- Audio Return Channel
- 3D Format Support
- Improved Electrical Characteristics
- CEC
  - 3 Buffers
  - HDMI 1.4 CEC Features
- HDCP
- CSC and Packet Update Feature
- Video Input Detection
- Video Data Range Clipping
- Miscellaneous
  - Chip ID and Revision Registers
  - TMDS Clock Inversion
  - Internal HPD Pulldown
- Changes in Fixed Registers

Pinout Differences

- ADV7511 and ADV7510 share a “pin-similar” 100-pin LQFP package
- HEAC+/- and SPDIF_OUT pins added
  - Changed from GND and NC
- HPD pin now includes an internal pull-down resistor (see slide 24)

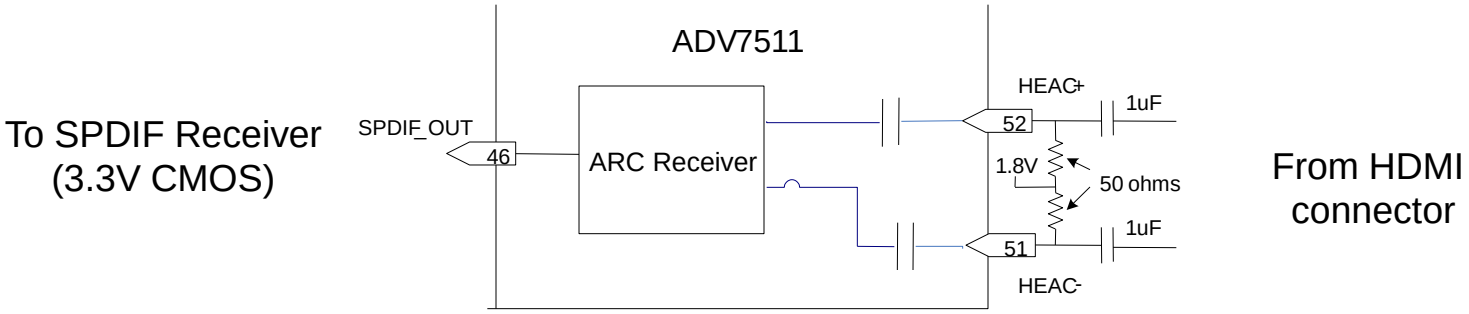




ANALOG DEVICES

Audio Return Channel

- **ADV7511 adds the ARC function from HDMI 1.4a**
- **PCB Change**
  - **Add the following circuit to incorporate the ARC function in hardware**



- **ARC Registers**

Table 75 Audio Return Channel (ARC) Related Registers (Main Map)

Address	Type	Bits	Default Value	Register Name	Function
0xDF	R/W	[7]	0*******	ARC Mode Select	ARC Single Ended or Common Mode Selection, ARC Disable 0 = Common Mode ARC Input 1 = Single Ended ARC Input
		[0]	*******1	ARC Power Down Control	ARC Power Down Control 0 = ARC Powered up 1 = ARC in Power Down

3D Format Support (1)

- ADV7510 does not work with all 3D structures at all resolutions
- ADV7511 works with all 3D structures at all video resolutions defined in CEA 861E, assuming the TMDS clock is within the allowable range for the ADV7511 (< 225 MHz)
- Registers for DE Generation, Embedded Sync Generation, and Sync Adjustment have been expanded in order to support all 3D modes. This is shown in the following tables:
  - DE Generation

Parameter	ADV7510	ADV7511
Hsync Delay	10 bit: (0x35[7:0],0x36[7:6])	11 bit: (0xFB[7],0x35[7:0],0x36[7:6])
Vsync Delay	6 bit: (0x36[5:0])	8 bit: (0xFB[6:5], 0x36[5:0]
Active Width	12 bit: (0x37[4:0],0x38[7:1])	13 bit: (0xFB[4], 0x37[4:0],0x38[7:1])
Active Height	12 bit: (0x39[7:0],0x3A[7:4])	13 bit: (0xFB[3], 0x39[7:0],0x3A[7:4])

3D Format Support (2)

- **Sync Adjustment**

Parameter	ADV7510	ADV7511
Hsync Placement	10 bit: (0xD7[7:0],0xD8[7:6])	13 bit: (0xFA[4:2],0xD7[7:0],0xD8[7:6])
Vsync Window	9 bit: (0xDC[4:0],0xDD[7:4])	11 bit: (0xFA[1:0],0xDC[4:0],0xDD[7:4])

- **Embedded Sync Decoding**

Parameter	ADV7510	ADV7511
Hsync Placement	10 bit: (0x30[7:0],0x31[7:6])	13 bit: (0xFA[7:5],0x30[7:0],0x31[7:6])

Improved Electrical Characteristics

- Rise time and fall time have been decreased for more margin on the 1080p 12-bit color eye diagram.
- The R_EXT sensitivity to noise has been decreased
- ESD protection has been improved on the R_EXT pin

CEC Section Functionality Changes

- 2 Rx message buffers added
- I2C Controls to handle 2 buffers are added (detailed in Register Changes section)
- Interrupts for user defined Op Codes are added
- Rx Enable is now a read only bit. It does not need to be written to enable the Rx.
- Tx Enable is no longer self clearing, and must be cleared manually

CEC Register Map Changes – CEC Rx (1)

- To make room for register controls for the additional CEC Rx buffers, the CEC timing related registers in the CEC Register Map were moved from 0x27-0x52 to 0x4B – 0x76

- ADV7510:

Address	Type	Bits	Register Name
0x27	R/W	[6:4]	Logical Address Mask
		[3]	Error Report Mode
		[2]	Error Detect Mode
		[1]	Force NACK
		[0]	Force Ignore
0x28	R/W	[7:4]	Logical Address1
		[3:0]	Logical Address0
0x29	R/W	[3:0]	Logical Address2
0x2A	R/W	[7:2]	Clock Divider
		[1:0]	Power Mode
0x2B	R/W	[5:0]	Glitch Filter Ctrl
0x2C	R/W	[0]	Soft Reset
0x2D-0x2E	R/W	[15:0]	St Total
0x2F-0x30	R/W	[15:0]	St Total Min
0x31-0x32	R/W	[15:0]	St Total Max
0x33-0x34	R/W	[15:0]	St Low
0x35-0x36	R/W	[15:0]	St Low Min
0x37-0x38	R/W	[15:0]	St Low Max
0x39-0x3A	R/W	[15:0]	Bit Total
0x3B-0x3C	R/W	[15:0]	Bit Total Min
0x3D-0x3E	R/W	[15:0]	Bit Total Max
0x3F-0x40	R/W	[15:0]	Bit Low One
0x41-0x42	R/W	[15:0]	Bit Low Zero
0x43-0x44	R/W	[15:0]	Bit Low Max
0x45-0x46	R/W	[15:0]	Sample Time
0x47-0x48	R/W	[15:0]	Line Error Time
0x49	R/W	[0]	Fixed
0x4A-0x4B	R/W	[15:0]	Rise Time
0x4C	R/W	[0]	Bit Low Detection Mode
0x4D-0x4E	R/W	[15:0]	Bit Low One Min
0x4F-0x50	R/W	[15:0]	Bit Low One Max
0x51-0x52	R/W	[15:0]	Bit Low Zero Min

- ADV7511:

Address	Type	Bits	Register Name
0x4B	R/W	[6:4]	Logical Address Mask
		[3]	Error Report Mode
		[2]	Error Detect Mode
		[1]	Force NACK
		[0]	Force Ignore
0x4C	R/W	[7:4]	Logical Address1
		[3:0]	Logical Address0
0x4D	R/W	[3:0]	Logical Address2
0x4E	R/W	[7:2]	Clock Divider
		[1:0]	Power Mode
0x4F	R/W	[5:0]	Glitch Filter Ctrl
0x50	R/W	[0]	Soft Reset
0x51-0x52	R/W	[15:0]	St Total
0x53-0x54	R/W	[15:0]	St Total Min
0x55-0x56	R/W	[15:0]	St Total Max
0x57-0x58	R/W	[15:0]	St Low
0x59-0x5A	R/W	[15:0]	St Low Min
0x5B-0x5C	R/W	[15:0]	St Low Max
0x5D-0x5E	R/W	[15:0]	Bit Total
0x5F-0x60	R/W	[15:0]	Bit Total Min
0x61-0x62	R/W	[15:0]	Bit Total Max
0x63-0x64	R/W	[15:0]	Bit Low One
0x65-0x66	R/W	[15:0]	Bit Low Zero
0x67-0x68	R/W	[15:0]	Bit Low Max
0x69-0x6A	R/W	[15:0]	Sample Time
0x6B-0x6C	R/W	[15:0]	Line Error Time
0x6D	R/W	[0]	Fixed
0x6E-0x6F	R/W	[15:0]	Rise Time
0x70	R/W	[0]	Bit Low Detection Mode
0x71-0x72	R/W	[15:0]	Bit Low One Min
0x73-0x74	R/W	[15:0]	Bit Low One Max
0x75-0x76	R/W	[15:0]	Bit Low Zero Min

CEC Register Map Changes – CEC Rx (2)

- 2 new CEC Rx buffers have been added
- The 3 buffers are named 1, 2, and 3
- The Length, Header, and Data for buffer 1 are the same as the controls for the buffer on ADV7510 (0x15-0x25)
  - Added Message Length for buffers 2 and 3 (0x37[4:0] and 0x48[4:0])
  - Added Message Header for buffers 2 and 3 (0x27 and 0x38)
  - Added Message Data [14:0] for buffers 2 and 3 (0x28-0x36 and 0x39-47)

- ADV7510 and ADV7511 (buffer 1 registers):

Address	Type	Bits	Register Name
0x15	RO	[7:0]	Rx Frame Header (Buffer 1)
0x16	RO	[7:0]	Rx Frame Data0 (Buffer 1)
0x17	RO	[7:0]	Rx Frame Data1 (Buffer 1)
0x18	RO	[7:0]	Rx Frame Data 2 (Buffer 1)
0x19	RO	[7:0]	Rx Frame Data3 (Buffer 1)
0x1A	RO	[7:0]	Rx Frame Data4 (Buffer 1)
0x1B	RO	[7:0]	Rx Frame Data5 (Buffer 1)
0x1C	RO	[7:0]	Rx Frame Data6 (Buffer 1)
0x1D	RO	[7:0]	Rx Frame Data7 (Buffer 1)
0x1E	RO	[7:0]	Rx Frame Data8 (Buffer 1)
0x1F	RO	[7:0]	Rx Frame Data9 (Buffer 1)

CEC Register Map Changes – CEC Rx (3)

- **Added on ADV7511 (buffer 2 and buffer 3 registers):**

Address	Type	Bits	Register Name
0x27	RO	[7:0]	Rx Frame Header (Buffer 2)
0x28	RO	[7:0]	Rx Frame Data0 (Buffer 2)
0x29	RO	[7:0]	Rx Frame Data1 (Buffer 2)
0x2A	RO	[7:0]	Rx Frame Data 2 (Buffer 2)
0x2B	RO	[7:0]	Rx Frame Data3 (Buffer 2)
0x2C	RO	[7:0]	Rx Frame Data4 (Buffer 2)
0x2D	RO	[7:0]	Rx Frame Data5 (Buffer 2)
0x2E	RO	[7:0]	Rx Frame Data6 (Buffer 2)
0x2F	RO	[7:0]	Rx Frame Data7 (Buffer 2)
0x30	RO	[7:0]	Rx Frame Data8 (Buffer 2)
0x31	RO	[7:0]	Rx Frame Data9 (Buffer 2)
0x32	RO	[7:0]	Rx Frame Data10 (Buffer 2)
0x33	RO	[7:0]	Rx Frame Data11 (Buffer 2)
0x34	RO	[7:0]	Rx Frame Data12 (Buffer 2)
0x35	RO	[7:0]	Rx Frame Data13 (Buffer 2)
0x36	RO	[7:0]	Rx Frame Data14 (Buffer 2)
0x37	RO	[4:0]	Rx Frame Length (Buffer 2)

Address	Type	Bits	Register Name
0x38	RO	[7:0]	Rx Frame Header (Buffer 3)
0x39	RO	[7:0]	Rx Frame Data0 (Buffer 3)
0x3A	RO	[7:0]	Rx Frame Data1 (Buffer 3)
0x3B	RO	[7:0]	Rx Frame Data 2 (Buffer 3)
0x3C	RO	[7:0]	Rx Frame Data3 (Buffer 3)
0x3D	RO	[7:0]	Rx Frame Data4 (Buffer 3)
0x3E	RO	[7:0]	Rx Frame Data5 (Buffer 3)
0x3F	RO	[7:0]	Rx Frame Data6 (Buffer 3)
0x40	RO	[7:0]	Rx Frame Data7 (Buffer 3)
0x41	RO	[7:0]	Rx Frame Data8 (Buffer 3)
0x42	RO	[7:0]	Rx Frame Data9 (Buffer 3)
0x43	RO	[7:0]	Rx Frame Data10 (Buffer 3)
0x44	RO	[7:0]	Rx Frame Data11 (Buffer 3)
0x45	RO	[7:0]	Rx Frame Data12 (Buffer 3)
0x46	RO	[7:0]	Rx Frame Data13 (Buffer 3)
0x47	RO	[7:0]	Rx Frame Data14 (Buffer 3)
0x48	RO	[4:0]	Rx Frame Length (Buffer 3)

CEC Register Map Changes – CEC Rx (4)

- **The Rx Enable bit was also removed (R0x26[0])**
  - **The ADV7511's CEC Rx is ready to receive messages upon power-up**
- **Added three 2-bit Time Stamp registers for Buffers 3, 2, and 1 (0x26[5:4],0x26[3:2],0x26[1:0])**
  - **Specifies the order in which the message in the current buffer was received relative to the other buffers**
    - 00 – no valid message
    - 01 – first received of current buffered messages
    - 10 – second received of current buffered messages
    - 11 – third received of current buffered messages
- **Added on ADV7511:**

Address	Type	Bits	Register Name
0x26	R/W	[5:4]	Rx 3 Time Stamp
		[3:2]	Rx 2 Time Stamp
		[1:0]	Rx 1 Time Stamp

CEC Register Map Changes – CEC Rx (5)

- **Added Rx Ready (0x49[2], 0x49[1], and 0x49[0]) and Clear Rx Ready (0x4A[2], 0x4A[1], and 0x4A[0]) for buffers 3, 2, and 1**
  - **Status register and clearing register for available messages**
- **Added Use All Buffers (0x4A[3])**
  - **Selects between 1 message buffering and 3 message buffering mode**
    - **Added on ADV7511:**

Address	Type	Bits	Register Name
0x49	R/W	[2]	Rx 3 Ready
		[1]	Rx 2 Ready
		[0]	Rx 1 Ready
0x4A	R/W	[3]	Use All Buffers
		[2]	Clear Rx 3 Ready
		[1]	Clear Rx 2 Ready
		[0]	Clear Rx 1 Ready

CEC Register Map Changes – Op Code Interrupts

- **Added eight one byte "Wake Up Op Code" registers (0x77 – 0x7E)**
  - **These registers set op codes to trigger interrupts (found in register 0x92 and 0x93 of the main register map)**
  - **Standard CEC op codes requiring a response are the default**
  - **The user can customize the op codes using I2C writes**

Added on ADV7511 (CEC Map):

Address	Type	Bits	Register Name
0x77	RO	[7:0]	Wake Up Op Code 1
0x78	RO	[7:0]	Wake Up Op Code 2
0x79	RO	[7:0]	Wake Up Op Code 3
0x7A	RO	[7:0]	Wake Up Op Code 4
0x7B	RO	[7:0]	Wake Up Op Code 5
0x7C	RO	[7:0]	Wake Up Op Code 6
0x7D	RO	[7:0]	Wake Up Op Code 7
0x7E	RO	[7:0]	Wake Up Op Code 8

Main Register Map Changes (for CEC)

- **CEC Interrupt Registers**
  - Added Interrupt Enables for Opcode Wakeup (0x92)
  - Added Interrupts for Opcode Wakeup (0x93)
  - Added Interrupt Enables for Rx Ready 2-0 (0x95[2:0])
  - Added Interrupts for Rx Ready 2-0 (0x97[2:0])

- **Added on ADV7511 (Main Map):**

Address	Type	Bits	Register Name
0x92	R/W	[7]	Wake Up Op Code 1 Interrupt Enable
		[6]	Wake Up Op Code 2 Interrupt Enable
		[5]	Wake Up Op Code 3 Interrupt Enable
		[4]	Wake Up Op Code 4 Interrupt Enable
		[3]	Wake Up Op Code 5 Interrupt Enable
		[2]	Wake Up Op Code 6 Interrupt Enable
		[1]	Wake Up Op Code 7 Interrupt Enable
		[0]	Wake Up Op Code 8 Interrupt Enable
0x93	R/W	[7]	Wake Up Op Code 1 Interrupt
		[6]	Wake Up Op Code 2 Interrupt
		[5]	Wake Up Op Code 3 Interrupt
		[4]	Wake Up Op Code 4 Interrupt
		[3]	Wake Up Op Code 5 Interrupt
		[2]	Wake Up Op Code 6 Interrupt
		[1]	Wake Up Op Code 7 Interrupt
		[0]	Wake Up Op Code 8 Interrupt
0x95	R/W	[2]	Rx Ready 3 Interrupt Enable
		[1]	Rx Ready 2 Interrupt Enable
		[0]	Rx Ready 1 Interrupt Enable
0x97	R/W	[2]	Rx Ready 3 Interrupt
		[1]	Rx Ready 2 Interrupt
		[0]	Rx Ready 1 Interrupt

CEC CDC HPD and Arbitration

- In HDMI 1.4, special rules for CDC message arbitration were defined
- ADV7511 can either enable or disable this special arbitration using CDC Arbitration Enable Register 0x7F[7] in the CEC Register Map
- Added HPD Control Register 0xD6[7:6] in the Main Register Map
  - 00 = HPD is from both HPD pin and CDC HPD
  - 01 = HPD is from CDC HPD
  - 10 = HPD is from HPD pin
  - 11 = HPD is always high

CEC CDC HPD and Arbitration

New Registers in CEC Map

Address	Type	Bits	Default Value	Register Name	Function
0x7F	R/W	[7]	1*******	CDC Arbitration Enable	Controls whether to do special CDC messsage arbitration upon receiving CDC messsage 1 = enable 0 = disable
		[6]	*1******	CDC HPD Response Enable	Controls whether to toggle internal HPD signals when receving CDC HPD messsage 1 = enable 0 = disable
0x80	R/W	[15:0]	00000000	CEC Physical Address	Physical address of CEC device
0x81			00000000		
0x82	R/W	[7:0]	00000001	CDC HPD Timer Count	Controls the time CDC HPD stays low when receiving CDC HPD toggle message. HPD low = CDC_HPD_Timer_Count * CEC_CLK. CEC_CLK is 760KHz by default.
0x83	RO	[7]	0*******	CDC HPD	HPD signal from CEC interface

HDCP Adjustments Added

- Delay can be controlled throughout each step of the HDCP authentication procedure
- New Registers
  - HDCP Ri Checking Frequency 0xFC[7:6]
  - HDCP Ri Checking Position Delay 0xFC[5:3]
  - HDCP BCAPS Read Delay 0xFC[2:0]
  - HDCP An Write Delay 0xFD[7:5]
  - HDCP AKSV Write Delay 0xFD[4:2]
  - HDCP Start Delay 0xFE[7:5]

HDCP New Registers

Address	Type	Bits	Default Value	Register Name	Function
0xFC	R/W	[7:6]	00******	Ri Checking Freqyency	Ri Checking Freqyency 00 = 128 frames 10 = 64 frames 10 = 32 frames 11 = 16 frames
		[5:3]	**000***	Ri Checking Position Delay	Ri Checking Position Delay in Units of Hsync 0 = no delay 1 = 8 Hsyncs 2 = 16 Hsyncs 3 = 32 Hsyncs 4 = 64 Hsyncs 5 = 128 Hsyncs 6 = 256 Hsyncs 7 = 512 Hsycns
		[2:0]	*****000	BCAPS Read Delay	Delay Between Reading of BKSV and BCAPs 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFD	R/W	[7:5]	000*****	An Write Delay	Delay Between Reading of BCAPS and Writing of An 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
		[4:2]	***000**	ASKV Write Delay	Delay Between Writing of An and Writing of AKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms
0xFE	R/W	[7:5]	000*****	HDCP Start Delay	Delay Between Setting Enable HDCP Register 0xAF[7] = 1 and Reading of BKSV 000 = no delay 001 = 1ms 010 = 2ms 011 = 5ms 100 = 10ms 101 = 25ms 110 = 50ms 111 = 100ms

CSC and Packet Update Feature

- To avoid sending partially updated packets, a packet update features has been added for CSC and all HDMI packets
- The packet/CSC update bit should be set to 1 before updating registers related to the packet or CSC, then set to 0 when updating is complete
- CSC
  - Added CSC Coefficient Update register –0x1A[5]
  - The CSC Coefficient Update includes timing control to ensure that the coefficients are updated during the blanking period
    - Does not include the “scaling factor” bits (R0x18[6:5]) – changes to these bits take effect immediately

CSC and Packet Update Feature

- **Note: Since Packet Update Memory is shared, only one packet can use the feature at one time**

Packet Type	Control Bits
AVI InfoFrame	Main map 0x4A[6]
Audio InfoFrame	Main Map 0x4A[5]
General Control Packet	Main Map 0x4A[4]
Source Product Description Packet	Packet Memory 0x1F[7]
MPEG InfoFrame	Packet Memory 0x3F[7]
Audio Content Protection Packet	Packet Memory 0x5F[7]
ISRC 1 Packet	Packet Memory 0x7F[7]
ISRC 2 Packet	Packet Memory 0x9F[7]
Gamut Metadata Packet	Packet Memory 0xBF[7]
Spare Packet 1	Packet Memory 0xDF[7]
Spare Packet 2	Packet Memory 0xFF[7]

Video Input Detection

- Added Low Refresh Rate (VID Detection) – Register 0xFB[2:1]
  - 00 = Non Low Refresh Rate
  - 01 = 24Hz
  - 10 = 25Hz
  - 11 = 30Hz
- Removed Low Refresh Rate Video Register (0x48[7])

Video Data Range Clipping

- **Video Data Range Clipping registers were moved from 0x53-0x5A in the CEC map to 0xC0-0xC7 in the CEC Map**

ADV7510

Address	Type	Bits	Default Value	Register Name	Function
0x53	R/W	[11:0]	****0000	Y or RGB Minimum	Minumum value for Y or RGB for video data clipping.
0x54			00000000		
0x55	R/W	[11:0]	****1111	Y or RGB Maximum	Maximum value for Y or RGB for video data clipping.
0x56			11111111		
0x57	R/W	[11:0]	****0000	CbCr Minimum	Minimum value for Cb/Cr for video data clipping
0x58			00000000		
0x59	R/W	[11:0]	****1111	CbCr Maximum	Maximum value for Cb/Cr for video data clipping.

ADV7511

Address	Type	Bits	Default Value	Register Name	Function
0xC0	R/W	[11:0]	****0000	Y or RGB Minimum	Minumum value for Y or RGB for video data clipping.
0xC1			00000000		
0xC2	R/W	[11:0]	****1111	Y or RGB Maximum	Maximum value for Y or RGB for video data clipping.
0xC3			11111111		
0xC4	R/W	[11:0]	****0000	CbCr Minimum	Minimum value for Cb/Cr for video data clipping
0xC5			00000000		
0xC6	R/W	[11:0]	****1111	CbCr Maximum	Maximum value for Cb/Cr for video data clipping.

Miscellaneous Changes

- **Chip ID**
  - Added Chip ID 0xF5-0xF6 = 0x7511
  - Added Chip ID Suffix 0xF7 = 0x00
- **Added TMDS Clock Inversion bit 0xDE[3]**

Address	Type	Bits	Default Value	Register Name	Function
0xDE	R/W	[3]	****0***	TMDS Clock Inversion	TMDS Clock Inversion 0 = Normal TMDS Clock 1 = Inverted TMDS Clock

- **Added Internal HPD Pull-down Resistor**
  - Allows user to remove recommended 10k pull-down
  - Controlled by register 0xE0[0]

Address	Type	Bits	Default Value	Register Name	Function
0xE0	R/W	[0]	*******0	HPD Pull Down	HPD Pull Down 0 = No Internal HPD Pulldown 1 = Weak Internal HDP Pulldown Active

Fixed Register Changes

- **The following tables reflect changes to the “fixed” registers and their recommended settings**

Register	ADV7510 Setting	ADV7511 Setting
0x9A[7:1]	Default	Set to 0b1110000
0xDE	Set 0x9C	Default
0xE0	Default	Set to 0xD0
0xF9	Default	Set to 0x00