Evaluation Board for 12-/10-Bit, 4-Channel ADCs with a Parallel Interface

EVAL-AD7933/AD7934

FEATURES

Full-featured evaluation board for the AD7933/AD7934
EVAL-CONTROL-BRD2 compatible
Standalone capability
On-board analog buffering and voltage reference
On-board single-ended-to differential conversion
Various linking options
PC software for control and data analysis when used with evaluation board controller

GENERAL DESCRIPTION

This data sheet describes the evaluation board used for the AD7933/AD7934, which are 10-bit/12-bit, high speed, low power successive approximation analog-to-digital converters (ADCs). These parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS. They can operate with four single-ended analog inputs, two fully differential analog inputs, or two pseudo differential analog inputs.

Full details about the parts are available in the AD7933/AD7934 data sheets from Analog Devices, Inc. It should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include

- One AD780, a pin-programmable, 2.5 V or 3 V ultrahigh precision band gap reference
- One AD713 quad op amp
- One AD8022 dual op amp
- Six AD8021 single op amps
- Two AD8138 differential amplifiers
- One P174FCT digital buffer

Various link options are explained in Table 1.

Interfacing to this board is accomplished through a 96-way connector that is compatible with the EVAL-CONTROL-BRD2 from Analog Devices. External sockets are provided for a number of signals, including the V_{REF} input, the analog inputs, and the digital inputs and outputs.

FUNCTIONAL BLOCK DIAGRAM

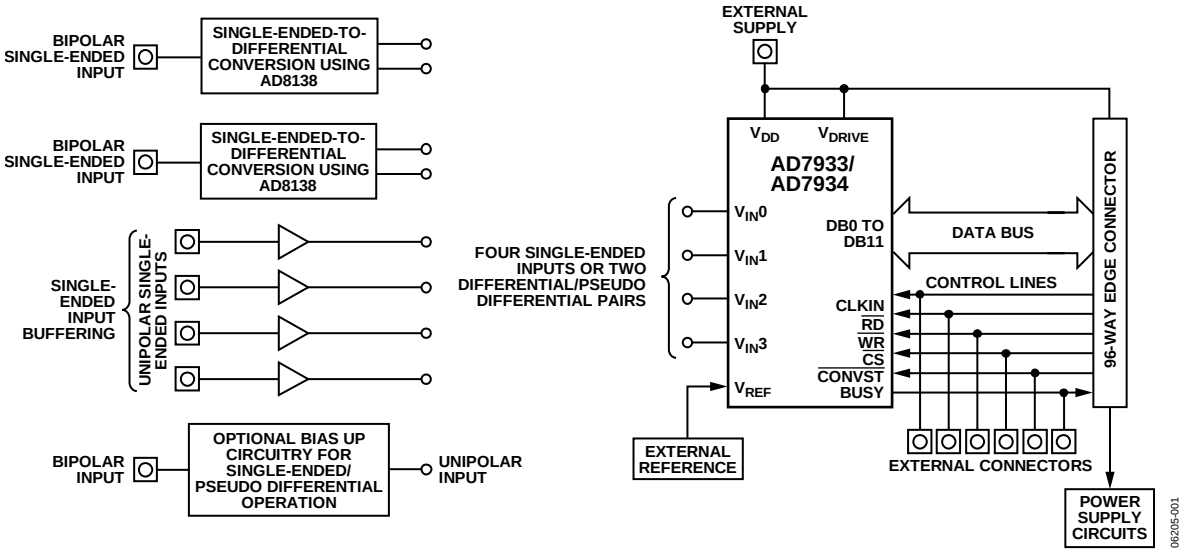

Figure 1.

Rev. 0

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REVISION HISTORY

8/07—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CONTROL-BRD2, all supplies are provided from the EVAL-CONTROL-BRD2 through the 96-way connector.

When using the board as a standalone unit, external supplies must be provided. This evaluation board has five power supply inputs:

- V_{DD} EXT for the ADC
- +5 V and −5 V for the AD8138 differential amplifiers
- +12 V and −12 V for the op amps
- VCC for the digital devices
- V_{DRIVE} for the ADC digital interface

The supplies are decoupled to the relevant ground plane with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors at the point where they enter the board. The supply pins of all op amps and the reference are also decoupled to AGND with a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. The AD7933/AD7934 V_{DD} supply pin is decoupled to AGND with 10 µF tantalum and 0.1 µF multilayer ceramic capacitors.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, AGND and DGND. These are connected at one location close to the AD7933/AD7934 ADC.

LINK OPTIONS

There are 46 link options that must be set for the required operating setup before using the evaluation board. The functions of these options are outlined in Table 1. The required settings for different operating modes are detailed in Table 2, Table 3, Table 4, Table 5, and Table 6.

Table 1. Link Option Functions

Link No.	Function
LK1	This link option selects the source of the V_{DD} +5 V supply used to supply the AD8138 differential amplifiers. In Position A, V_{DD} is supplied from the EVAL-CONTROL-BRD2. In Position B, V_{DD} must be supplied from an external source through the power connector, J4.
LK2	This link option selects the source of the V_{SS} −5 V supply used to supply the AD8138 differential amplifiers. In Position A, V_{SS} is supplied from the EVAL-CONTROL-BRD2. In Position B, V_{SS} must be supplied from an external source through the power connector, J4.
LK3	This link option selects the source of the V_{DD} supply for the AD7934/AD7933 ADC. In Position A, V_{DD} is supplied from the EVAL-CONTROL-BRD2. In Position B, V_{DD} must be supplied from an external source through J2. For V_{DD} < 3 V operation, V_{DD} must be supplied from an external source through J3.
LK4	This link option selects the source of the V_{DRIVE} supply for the AD7934/AD7933 ADC digital interface. In Position A, V_{DRIVE} is tied to V_{DD}. In Position B, V_{DRIVE} is supplied via the EVAL-CONTROL-BRD2. In Position C, V_{DRIVE} must be supplied from an external source through J3.
LK5	This link selects the source of the $\overline{WR}$ input to the ADC. In Position A, $\overline{WR}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{WR}$ must be supplied from an external source through P16.
LK6	This link selects where the BUSY output from the ADC appears. In Position A, BUSY output may be read by the EVAL-CONTROL-BRD2. In Position B, BUSY may be read via the external socket, P15.
LK7	This link selects the source of the $\overline{CONVST}$ input to the ADC. In Position A, $\overline{CONVST}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{CONVST}$ must be supplied from an external source through P14.
LK8	This link selects the source of the $\overline{RD}$ input to the ADC. In Position A, $\overline{RD}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{RD}$ must be supplied from an external source through P13.
LK9	This link selects the source of the $\overline{CS}$ input to the ADC. In Position A, $\overline{CS}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{CS}$ must be supplied from an external source through P12.

Link No.	Function
LK10	This link selects the state of the W/$\overline{B}$ input. In Position A, W/$\overline{B}$ is tied low. In Position B, W/$\overline{B}$ is tied to V_{CC}.
LK11	This link selects the source of the CLKIN input to the ADC. In Position A, CLKIN is supplied by the EVAL-CONTROL-BRD2. In Position B, CLKIN must be supplied from an external source through P11.
LK12	If an external reference is being used, this link should be placed in Position A. If the internal reference is being used, this link should be placed in Position B.
LK13	This link selects the analog input to be applied to the buffer, U8, which is used when operating in single-ended mode and when using $V_{IN}3$. If the single-ended input applied to $V_{IN}3$ is unipolar, this link should be in Position A, and the analog input should be applied at P10 with LK15 in Position B. If the single-ended input applied to $V_{IN}3$ is bipolar, this link should be in Position B and the analog input should be biased up, using the bias circuit by applying it to P18.
LK14	This link option adds a 50 Ω termination to AGND at the $V_{IN}3$ socket (P10) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK15	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}3$ is part of a differential pair with $V_{IN}2$, LK15 should be in Position A because this input is applied to the AD8138 differential amplifier. If the analog input applied to $V_{IN}3$ is a single-ended analog input, LK15 should be in Position B because this input is applied to the op amp buffer.
LK16	This link selects the input to the −IN input of the AD8138 differential amplifier (U7). If the user applies a fully differential signal to $V_{IN}2$ and $V_{IN}3$, and only requires buffering of this signal before it is applied to the ADC, then Link 16 should be in Position A. If the user is applying a single-ended input to $V_{IN}2$ and requires the use of the AD8138 to perform single-ended-to-differential conversion, then this link should be in Position B. In this case, no input is applied to $V_{IN}3$.
LK17	This link selects the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U7). In Position A, an external common-mode input must be applied via P8. In Position B, V_{REF} is applied to the common-mode input. In Position C, $V_{REF}/2$ is applied to the common-mode input.
LK18	This link option adds a 50 Ω termination to AGND at the $V_{IN}2$ socket (P7) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK19	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}2$ is a single-ended analog input, LK19 should be in Position A, because this input is applied to the op amp buffer. If the analog input applied to $V_{IN}2$ is part of a differential pair with $V_{IN}3$, LK19 should be in Position B because this input is applied to the AD8138 differential amplifier (U7).
LK20	This link selects the analog input to be applied to the buffer, U6, which is used when operating in single-ended mode or pseudo differential mode and when using $V_{IN}2$. If the single-ended input applied to $V_{IN}2$ is unipolar, this link should be in Position A and the analog input should be applied at P7 with LK19 in Position B. If the single-ended input applied to $V_{IN}2$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK21	This link selects the analog input to be applied to the buffer, U5, which is used when operating in single-ended mode and when using $V_{IN}1$. If the single-ended input applied to $V_{IN}1$ is unipolar, this link should be in Position A and the analog input should be applied at P3 with LK23 in Position A. If the single-ended input applied to $V_{IN}1$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK22	This link option adds a 50 Ω termination to AGND at the $V_{IN}1$ socket (P3) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.

Link No.	Function
LK23	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}1$ is a single-ended analog input, LK23 should be in Position A because this input is applied to the op amp buffer. If the analog input applied to $V_{IN}1$ is part of a differential pair with $V_{IN}0$, LK23 should be in Position B because this input is applied to the AD8138 differential amplifier.
LK24	This link selects the input to the VIN− input of the AD8138 differential amplifier (U4). If the user applies a fully differential signal to $V_{IN}0$ and $V_{IN}1$ and only requires buffering of this signal before it is applied to the ADC, LK24 should be in Position A. If the user is applying a single-ended input to $V_{IN}0$ and requires the use of the AD8138 to perform single-ended-to-differential conversion, this link should be in Position B. In this case, no input is applied to $V_{IN}1$.
LK25	This link selects the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4). In Position A, an external common-mode input must be applied through P2. In Position B, V_{REF} is applied to the common-mode input. In Position C, $V_{REF}/2$ is applied to the common-mode input.
LK26	This link option adds a 50 Ω termination to AGND at the $V_{IN}0$ socket (P1) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK27	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}0$ is a single-ended analog input, LK27 should be in Position A because this input is applied to the op amp buffer. If the analog input applied to $V_{IN}0$ is part of a differential pair with $V_{IN}1$, LK27 should be in Position B because this input is applied to the AD8138 differential amplifier (U4).
LK28	This link selects the analog input to be applied to the buffer, U2, which is used when operating in single-ended mode or pseudo differential mode and when using $V_{IN}0$. If the single-ended input applied to $V_{IN}0$ is unipolar, this link should be in Position A and the analog input should be applied at P1 with LK27 in Position A. If the single-ended input applied to $V_{IN}0$ is bipolar, this link should be in Position B and the analog input should be biased up, using the bias circuit by applying it to P18.
LK29	This link option selects the source of the $V_{IN}0$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}0$. In Position B, $V_{IN}0$ is supplied from the positive output of the AD8138 (U4) differential amplifier to provide half a differential pair with $V_{IN}1$. In Position C, an external $V_{IN}0$ is applied to the ADC through P4. In Position D, $V_{IN}0$ is tied to AGND. This should occur when $V_{IN}0$ is not being used and when power supplies are first applied to the board.
LK30	This link option selects the source of the $V_{IN}1$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}1$. In Position B, $V_{IN}1$ is supplied from the negative output of the AD8138 (U4) differential amplifier to provide half a differential pair with $V_{IN}0$. In Position C, an external $V_{IN}1$ is applied to the ADC through P5. In Position D, $V_{IN}1$ is tied to AGND. This should occur when $V_{IN}1$ is not being used and when power supplies are first applied to the board.
LK31	This link option selects the source of the $V_{IN}2$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}2$. In Position B, $V_{IN}2$ is supplied from the positive output of the AD8138 (U7) differential amplifier to provide half a differential pair with $V_{IN}3$. In Position C, an external $V_{IN}2$ is applied to the ADC through P6. In Position D, $V_{IN}2$ is tied to AGND. This should occur when $V_{IN}2$ is not being used and when power supplies are first applied to the board.
LK32	This link option selects the source of the $V_{IN}3$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}3$. In Position B, $V_{IN}3$ is supplied from the negative output of the AD8138 (U7) differential amplifier to provide half a differential pair with $V_{IN}2$. In Position C, an external $V_{IN}3$ is applied to the ADC through P9. In Position D, $V_{IN}3$ is tied to AGND. This should occur when $V_{IN}1$ is not being used and when power supplies are first applied to the board.
LK45	Always insert.

Link No.	Function
LK46	Always insert.
LK55	This link is used to configure the bias up circuit. In Position A, REF is buffered to supply V_{REF} to the common-mode voltage of the differential amplifier and to the bias-up circuit. In Position A, REF is divided down by two then buffered to supply $V_{REF}/2$ to the common-mode voltage of the AD8138 differential amplifier.
LK56	When $V_{REF}/2$ is not being used, LK56 should be inserted so the inputs to U13C are not floating.
LK57	This link chooses the source of an external reference input. In Position A, an external reference should be applied via P17. In Position B, the output of the AD780 reference chip is applied to the V_{REF} pin. In Position C, ¾ of the AD780 output is applied to the V_{REF} pin. The resistors R35 and R52 can be changed if the user requires an alternative reference input.
LK58	This link determines whether the output of the AD780 reference chip is applied directly to LK57 or if it is divided down before being applied to LK57. In Position A, the output of the AD780 is applied to LK57. In Position B, the output of the AD780 is divided down before being applied to LK57.
LK59	This link option controls the program pin of the AD780 reference. When this pin is inserted, the AD780 output voltage is set to 3 V. When this pin is removed, the AD780 output voltage is set to 2.5 V.
LK60	This link option determines the source of the VCC (+5 V) digital supply. When inserted, VCC is supplied via the EVAL-CONTROL-BRD2. When removed, VCC must be supplied to the external connector, J5.
LK61	This link selects the dc voltage to be applied to the bias-up circuit that is used when a single-ended, bipolar signal needs to be converted to a unipolar signal. In Position A, V_{REF} is applied to the bias-up circuit. In Position B, the dc input to the bias-up circuit is tied to AGND. This should be done if the bias up circuit is not being used.
LK62	This link selects what portion of the V_{REF} input is applied to the bias-up circuit. The choice depends on the nature of the user's analog input signal. In Position A, ¼ of the reference is applied to the bias-up circuit In Position B, ½ of the reference is applied to the bias-up circuit. If the bias-up circuit is not used, this link can be removed.
LK63	This link option adds a 50 Ω termination to AGND at the VIN S.E. socket (P18) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK64	This link option selects the source of the +12 V power supply. In Position A, the +12 V is supplied by the EVAL-CONTROL-BRD2. In Position B, the +12 V must be supplied from an external source via J6.
LK65	This link option selects the source of the −12 V power supply. In Position A, the −12 V is supplied via the EVAL-CONTROL-BRD2. In Position B, the −12 V must be supplied from an external source via J6.
LK66	When the reference output of the AD780 is not being divided down, this link should be inserted so that the input of U10 is not floating.

SETUP CONDITIONS

Before applying power and signals to the evaluation board, care must be taken to ensure that all link positions are set up in accordance with the required operating mode. There are a few different modes in which to operate the evaluation board. The user can either operate the board with the EVAL-CONTROL-BRD2 or use it as a standalone board. The board can be set up to accept four single-ended inputs, two differential inputs, or two pseudo differential inputs. The link settings for the different modes of operation are detailed in Table 2, Table 3, Table 4, Table 5, and Table 6.

The AD7933/AD7934 can accept two fully differential analog input pairs. These can either be applied as two pairs to P1, P3 and P7, P10; or a single-ended-to-differential conversion can be performed on a single-ended input applied to P1 and P7. The link positions in Table 2 are required for operating the evaluation board in differential mode. These are the link positions when the board is shipped. The board is shipped with the assumption that the evaluation board is going to operated with the EVAL-CONTROL-BRD2. The links are set so that all power supplies and control signals are supplied by the EVAL-CONTROL-BRD2. Initially, all analog inputs are tied to ground to ensure that they are not floating on power-up. The user must change these link positions, depending on which analog inputs are in use.

Table 2. Differential Mode—Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	A	V_{DD} for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK2	A	V_{SS} for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK3	A	V_{DD} for the AD7934/AD7933 ADC is supplied by the EVAL-CONTROL-BRD2.
LK4	B	V_{DRIVE} is supplied by the EVAL-CONTROL-BRD2.
LK5	A	$\overline{WR}$ is supplied by the EVAL-CONTROL-BRD2.
LK6	A	BUSY is read by the EVAL-CONTROL-BRD2.
LK7	A	$\overline{CONVST}$ is supplied by the EVAL-CONTROL-BRD2.
LK8	A	$\overline{RD}$ is supplied by the EVAL-CONTROL-BRD2.
LK9	A	$\overline{CS}$ is supplied by the EVAL-CONTROL-BRD2.
LK10	B	ADC is set up to operate in WORD mode.
LK11	A	CLKIN is supplied by the EVAL-CONTROL-BRD2.
LK12	A	An external reference is supplied to the V_{REFIN}/V_{REFOUT} pin from the AD780.
LK13	B	The input to U8 is tied to V_{BIASED} so it is not floating.
LK14	Inserted	On power-up, the inputs to the op amp is tied to ground so that it is not floating. Once a signal is applied to P10, LK14 can be removed if a 50 Ω termination is not required.
LK15	Removed	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}2$ (P7). This link should be placed in Position A if half a differential input is applied to P10.
LK16	B	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}2$ (P7). This link should be placed in Position A if half a differential input is applied to P10.
LK17	B	V_{REF} is applied to the V_{OCM} pin of the AD8138 differential amplifer to set up the common-mode voltage.
LK18	Inserted	On power-up, the inputs to the op amp is tied to ground so it is not floating. Once a signal is applied to P7, LK18 can be removed if a 50 Ω termination is not required.
LK19	A	If either a single-ended input or half a differential input is applied to $V_{IN}2$ (P7).
LK20	B	The input to U6 is tied to V_{BIASED} so that it is not floating.
LK21	B	The input to U5 is tied to V_{BIASED} so that it is not floating.
LK22	Inserted	On power-up, the inputs to the op amp is tied to ground so that it is not floating. Once a signal is applied to P3, LK26 can be removed if a 50 Ω termination is not required.
LK23	Removed	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}0$ (P1). This link should be placed in Position B if half a differential input is applied to P3.
LK24	B	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}0$ (P1). This link should be placed in Position A if half a differential input is applied to P3.
LK25	B	V_{REF} is applied to the V_{OCM} pin of the AD8138 differential amplifier to set up the common-mode voltage.
LK26	Inserted	On power-up, the inputs to the op amp is tied to ground so that it is not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	B	If either a single-ended input or half a differential input is applied to $V_{IN}0$ (P1).
LK28	B	The input to U3 is tied to V_{BIASED} so that it is not floating.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK29 in Position B.

Link No.	Position	Function
LK30	D	On power-up, the analog input applied to $V_{IN}1$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied, $V_{IN}1$ of the ADC should be connected to the negative output of the AD8138 amplifier by placing LK30 in Position B.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK31 in Position B.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied, $V_{IN}3$ of the ADC should be connected to the negative output of the AD8138 amplifier by placing LK32 in Position B.
LK45	Inserted	Always insert.
LK46	Inserted	Always insert.
LK55	A and B	The inputs to U13-A-and U13-B are not floating.
LK56	Inserted	The input to U13-C is not floating.
LK57	B	V_{REF} is supplied by the AD780 reference chip.
LK58	A	The output of the AD780 supplies the reference to the ADC.
LK59	Removed	The output of the AD780 is 2.5 V.
LK60	Inserted	VCC is supplied by the EVAL-CONTROL-BRD2.
LK61	B	DC input to the bias-up circuit is tied to AGND because it is not used in this mode.
LK62	Removed	A bias-up circuit not used in this mode.
LK63	Inserted	Analog input to the bias-up circuit is tied to AGND because it is not used in this mode.
LK64	A	+12 V is supplied by the EVAL-CONTROL-BRD2.
LK65	A	−12 V is supplied by the EVAL-CONTROL-BRD2.
LK66	Inserted	The output of the AD780 is not divided down so the input to U10 is tied to AGND.

The AD7933/AD7934 can operate with four single-ended analog inputs. To operate the evaluation board in single-ended mode, the link positions must be changed, as shown in Table 3. All other link positions are as shown in Table 2. Initially, all analog inputs are tied to ground to ensure that on power-up, they are not floating. The user must change these link positions, depending on the analog inputs in use.

Table 3. Single-Ended Mode—Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	Removed	No power supply is connected to V_{DD} of the AD8138 differential amplifiers because they are not used in single-ended mode.
LK2	Removed	No power supply is connected to V_{SS} of the AD8138 differential amplifiers because they are not used in single-ended mode.
LK13	A	A single-ended, unipolar input must be supplied to $V_{IN}3$ (P10) and is buffered by U8.
LK14	Inserted	On power-up, the input to the op amp is tied to ground so it is not floating. Once a signal is applied to P10, LK14 can be removed if a 50 Ω termination is not required.
LK15	B	The analog input signal applied to P10 is applied to a single buffer (U8).
LK16	B	The negative input to the AD8138 is tied to AGND.
LK17	Removed	The AD8138 is not being used, so no common-mode voltage needs to be applied.
LK18	Inserted	On power-up, the input to the op amp is tied to ground so that it is not floating. Once a signal is applied to P7, LK18 can be removed if a 50 Ω termination is not required.
LK19	B	The analog input signal applied to P7 is applied to the single buffer (U6).
LK20	A	A single-ended, unipolar input must be supplied to $V_{IN}2$ (P7) and is buffered by U6.
LK21	A	A single-ended, unipolar input must be supplied to $V_{IN}1$ (P3) and is buffered by U5.
LK22	Inserted	On power-up, the input to the op amp is tied to ground so it is not floating. Once a signal is applied to P3, LK22 can be removed if a 50 Ω termination is not required.
LK23	A	The analog input signal applied to P3 is applied to the single buffer (U5).
LK24	B	The negative input to the AD8138 is tied to AGND.
LK25	Removed	The AD8138 is not being used, so no common-mode voltage needs to be applied.
LK26	Inserted	On power-up, the input to the op amp is tied to ground so it is not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	A	The analog input signal applied to P1 is applied to the single buffer (U3).
LK28	A	A single-ended, unipolar input must be supplied to $V_{IN}1$ (P1) and is buffered by U3.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ of the ADC is tied to AGND so that it is not floating. Once a single-ended analog input signal is applied to P1, LK29 should be placed in Position A.

Link No.	Position	Function
LK30	D	On power-up, the analog input applied to $V_{IN}1$ of the ADC is tied to AGND so that it is not floating. Once a single-ended analog input signal is applied to P3, LK30 should be placed in Position A.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ of the ADC is tied to AGND so that it is not floating. Once a single-ended analog input signal is applied to P7, LK31 should be placed in Position A.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ of the ADC is tied to AGND so that it is not floating. Once a single-ended analog input signal is applied to P10, LK32 should be placed in Position A.

The AD7933/AD7934 can accept two pseudo differential analog input pairs. The links in Table 4 should be changed for pseudo differential mode. All other links are as shown in Table 2.

Table 4. Pseudo Differential Mode—Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	Removed	No power supply is connected to V_{DD} of the AD8138 differential amplifiers because they are not used in pseudo differential mode.
LK2	Removed	No power supply is connected to V_{SS} of the AD8138 differential amplifiers because they are not used in differential mode.
LK13	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}3$.
LK15	B	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}3$.
LK19	B	The ac portion of the pseudo differential input applied to P7 is connected to the buffer U6 before being applied to $V_{IN}2$ of the ADC.
LK20	A	The ac portion of the pseudo differential input applied to P7 is connected to the buffer U6 before being applied to $V_{IN}2$ of the ADC.
LK21	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}1$.
LK23	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}1$.
LK27	A	The ac portion of the pseudo differential input applied to P1 is connected to the buffer U3 before being applied to $V_{IN}0$ of the ADC.
LK28	A	The ac portion of the pseudo differential input applied to P1 is connected to the buffer U3 before being applied to $V_{IN}0$ of the ADC.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ of the ADC should be connected to the positive output of the buffer by placing LK29 in Position A.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ of the ADC is tied to AGND so that it is not floating. Following power-up, the user can either keep $V_{IN}-$ of the pseudo differential pair tied to AGND, or an external dc voltage can be applied directly to P4 or to P3 and buffer it before it is applied to $V_{IN}1$ (Position B or Position C).
LK31	D	On power-up, the analog input applied to $V_{IN}2$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ of the ADC should be connected to the positive output of the buffer by placing LK31 in Position A.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ of the ADC is tied to AGND so that it is not floating. Following power-up, the user can either keep $V_{IN}-$ of the pseudo differential pair tied to AGND, or an external dc voltage can either be applied directly to P4 or applied to P3 and buffered before it is applied to $V_{IN}3$ (Position B or Position C).

The bias-up circuit can be used to bias up single-ended, bipolar signals to an appropriate dc voltage to make them unipolar to comply with the input requirements of the ADC.

Table 5. Using the Bias-Up Circuit in Single-Ended or Pseudo Differential Mode

Link No.	Position	Function
LK13	B	When operating in single-ended mode, if the user is applying a bipolar input signal to the bias-up circuit, it is applied to Buffer U8 through LK13.
LK20	B	When operating in single-ended mode or pseudo differential mode, if the user is applying a bipolar input signal to the bias-up circuit, it is applied to Buffer U6 via LK20.
LK21	B	When operating in single-ended mode, if the user is applying a bipolar input signal to the bias up circuit, it is applied to Buffer U5 through LK21.
LK28	B	When operating in single-ended mode or pseudo differential mode, if the user is applying a bipolar input signal to the bias-up circuit, it is applied to Buffer U8 through LK28.
LK61	A	V_{REF} is applied to the bias-up circuit to set up the dc bias voltage.
LK62	A or B	Position A or Position B depends on what bias voltage is required.

The AD7933/AD7934 evaluation board can be operated as a standalone evaluation board. The user must supply all power supplies and control signals. The link options shown in Table 1 are for standalone operation with single-ended unipolar inputs. Change the links appropriately for differential or pseudo differential inputs and when using the bias-up circuit. Any unused ADC analog input should be tied to AGND. To write to or read from the ADC data bus in standalone mode, use the 96-way connector (see Figure 2 and Table 8).

Table 6. Standalone Operation—Single-Ended, Unipolar Input Mode

Link No.	Position	Function
LK1	Removed	No supply is required for the AD8138 differential amplifiers because they are not used.
LK2	Removed	No supply is required for the AD8138 differential amplifiers because they are not used.
LK3	B	An external supply is required to power the ADC through J2 (V_{DD}_EXT).
LK4	A or B	V_{DRIVE} is taken from V_{DD}, or an external V_{DRIVE} should be applied through J3 (V_{DRIVE}).
LK5	B	The $\overline{WR}$ control input should be applied through P16.
LK6	B	The BUSY output should be read through P15.
LK7	B	The $\overline{CONVST}$ control input should be applied through P14.
LK8	B	The $\overline{RD}$ control input should be applied through P13.
LK9	B	The $\overline{CS}$ control input should be applied through P12.
LK10	B	ADC set to operate in Word mode.
LK11	B	The CLKIN should be applied through P11.
LK12	A	V_{REF} is supplied by the AD780 reference chip.
LK13	A	A single-ended unipolar input is applied to the buffer, U8.
LK14	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P10, LK14 can be removed if a 50 Ω termination is not required.
LK15	B	The single-ended, unipolar, analog input applied to P10 is connected to the buffer, U8.
LK16	B	The negative input to the AD8138 is connected to AGND because it is not used.
LK17	Removed	No common-mode voltage need be applied to the AD8138 because it is not used.
LK18	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P7, LK18 can be removed if a 50 Ω termination is not required.
LK19	B	The single-ended, unipolar, analog input applied to P7 is connected to the buffer, U6.
LK20	A	A single-ended unipolar input is applied to the buffer, U6.
LK21	A	A single-ended unipolar input is applied to the buffer, U5.
LK22	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P3, LK22 can be removed if a 50 Ω termination is not required.
LK23	A	The analog input applied to P3 is connected to the buffer, U5.
LK24	B	The negative input to the AD8138 is connected to AGND because it is not used.
LK25	Removed	No common-mode voltage need be applied to the AD8138 because it is not used.
LK26	Inserted	On power-up, the inputs to the opamps are tied to ground so they are not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	A	The single-ended, unipolar, analog input applied to P1 is connected to the buffer, U3.
LK28	A	A single-ended, unipolar input is applied to the buffer, U3.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ of the ADC should be connected to the positive output the buffer by placing LK29 in Position A. Alternatively, the user can apply an analog input signal directly to P4; in this case, LK29 should be in Position C.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P3, $V_{IN}1$ of the ADC should be connected to the positive output of the buffer by placing LK30 in Position A. Alternatively, the user can apply an analog input signal directly to P5. In this case, LK30 should be in Position C.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ of the ADC should be connected to the positive output of the buffer by placing LK31 in Position A. Alternatively, the user can apply an analog input signal directly to P6. In this case, LK31 should be in Position C.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P10, $V_{IN}3$ of the ADC should be connected to the positive output of the buffer by placing LK32 in Position A. Alternatively, the user can apply an analog input signal directly to P9. In this case, LK31 should be in Position C.

Link No.	Position	Function
LK55 and 56	Insert	Bias-up circuit not being used.
LK57	A or B	The user should apply an external reference through P17, or the reference is supplied by the AD780.
LK58		See Table 1.
LK59		See Table 1.
LK60	Remove	An external 5 V supply for VCC should be applied through J5.
LK61, 62, 63		See Table 1.
LK64	B	An external +12 V supply should be applied through J6 to supply the op amps and the voltage reference.
LK65	B	An external −12 V supply should be applied through J6 to supply the op amps and the voltage reference.

INTERFACING TO THE EVAL-CONTROL-BRD2

Interfacing to the EVAL-CONTROL-BRD2 is through a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2. Table 7 describes the pins on the 96-way connector used to interface between the EVAL-CONTROL-BRD2 and the EVAL-AD7933/AD7934. Table 8 lists the pin designations.

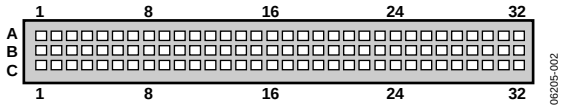

Figure 2. Pin Configuration for the 96-Way Connector

Table 7. 96-Way Connector Pin Descriptions

Pin	Description
D0 to D11	Data Bit 0 to Data Bit 11. Three-state TTL I/O pins used to read conversion data and to write data to the internal registers of the ADC. D11 is the MSB and D0 the LSB for the AD7934, and D2 is the LSB for the AD7933.
SCLK0	Serial Clock. This continuous clock is connected to the CLKIN pin of the AD7933/AD7934 through LK11.
+5V	Digital +5 V supply. This is used to provide a digital supply to the board for the digital logic.
$\overline{RD}$	Read. This is an active low logic input connected to the $\overline{RD}$ pin of the AD7933/AD7934 through LK8.
$\overline{WR}$	Write. This is an active low logic input connected to the $\overline{WR}$ pin of the AD7933/AD7934 through LK5.
$\overline{CS}$	Chip Select. This is an active low logic input connected to the $\overline{CS}$ pin of the AD7934/33 through LK9.
FL0	Flag Zero. This logic input is connected to the $\overline{CONVST}$ input of the AD7933/AD7934 through LK7.
$\overline{IRQ2}$	Interrupt Request 2. This is a logic output that is connected to the BUSY output of the AD7933/AD7934.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board, allowing the user to provide a digital power supply through the connector along with other digital signals.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
AVDD	Analog +5 V Supply. These lines are connected to the AVDD supply line on the evaluation board via LK1 to provide 5 V to the AD8138 differential amplifiers. They are also connected to the V_{DD} supply of the AD7933/AD7934 via LK3.
AV_{SS}	Analog −5 V Supply. These lines are connected to the AV_{SS} supply line on the evaluation board through LK2 to supply −5 V to the AD8138 differential amplifiers.
±12 V	±12 V Supply. These lines are connected to the ±12 V supply lines on the evaluation board through LK64 and LK65 to supply the AD713, the AD8021s, the AD8022, and the AD780.

Table 8. 96-Way Connector Pin Functions[1]

Pin	Row A	Row B	Row C
1			
2		D0	
3		D1	
4	DGND	DGND	DGND
5		D2	
6		D3	
7	SCLK0	D4	SCLK0
8	+5V	+5V	+5V
9	$\overline{RD}$	D5	$\overline{WR}$
10		D6	$\overline{CS}$
11		D7	
12	DGND	DGND	DGND
13		D8	
14		D9	
15		D10	
16	DGND	DGND	DGND
17		D11	$\overline{IRQ2}$
18			
19			
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30	−12 V	AGND	+12 V
31	AV_{SS}	AV_{SS}	AV_{SS}
32	AVDD	AVDD	AVDD

[1] The unused pins of the 96-way connector are not shown.

SOCKETS

There are 18 SMB input sockets relevant to the operation of the AD7933/AD7934 on this evaluation board. All of these sockets are used to apply an externally generated signal to the evaluation board. When operating the board with the EVAL-CONTROL-BRD2, the only necessary external sockets are used to supply the analog inputs to the ADC (that is, P1, P3, P7, and P10).

All the other sockets are optional and, if they are not used, their signals are supplied by the EVAL-CONTROL-BRD2. Most of these sockets are used when operating the board as a standalone unit because all the required signals are supplied from external sources. The functions of these sockets are outlined in Table 9.

Table 9. Socket Functions

Socket	Function	Description
P1	$V_{IN}0$	Subminiature BNC socket for a single-ended unipolar analog input to be applied to the $V_{IN}0$ input of the ADC in single-ended mode; or for a bipolar single-ended analog input to be applied to the AD8138 for single-ended-to-differential conversion in differential mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P2	COM1	Subminiature BNC socket for the dc analog input to the V_{OCM} pin on the AD8138 differential amplifier.
P3	$V_{IN}1$	Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}1$ input of the ADC in single-ended mode or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P4	Ext_$V_{IN}0$	Subminiature BNC socket for a signal to be applied directly to $V_{IN}0$ input of the ADC.
P5	Ext_$V_{IN}1$	Subminiature BNC socket for a signal to be applied directly to $V_{IN}1$ input of the ADC.
P6	Ext_$V_{IN}2$	Subminiature BNC socket for a signal to be applied directly to $V_{IN}2$ input of the ADC.
P7	$V_{IN}2.S$	Subminiature BNC socket for a single-ended unipolar analog input to be applied to the $V_{IN}2$ input of the ADC in single-ended mode; or for a bipolar single-ended analog input to be applied to the AD8138 for single-ended-to-differential conversion in differential mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P8	COM2	Subminiature BNC socket for the dc analog input to V_{OCM} pin on the AD8138 differential amplifier.
P5	Ext_$V_{IN}3.S$	Subminiature BNC socket for a signal to be applied directly to $V_{IN}3$ input of the ADC.
P10	$V_{IN}3$	Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}3$ input of the ADC in single-ended mode or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P11	CLKIN	Subminiature BNC socket for an external clock input.
P12	$\overline{CS}$	Subminiature BNC socket for an external $\overline{CS}$ input.
P13	$\overline{RD}$	Subminiature BNC socket for an external $\overline{RD}$ input.
P14	$\overline{CONVST}$	Subminiature BNC socket for an external $\overline{CONVST}$ input.
P15	BUSY	Subminiature BNC socket for an external BUSY input.
P16	$\overline{WR}$	Subminiature BNC socket for an external $\overline{WR}$ input.
P17	V_{REF}	Subminiature BNC socket for an external V_{REF} input.
P18	VIN S.E.	Subminiature BNC socket for the bipolar single-ended or pseudo differential analog input to the bias-up circuit.

CONNECTORS

There are six connectors on the AD7933/AD7934 evaluation board, as outlined in Table 10.

Table 10. Connector Functions

Connector	Function
J1	96-way connector for the digital interface and power supply connections.
J2	External V_{DD} power connector for the ADC.
J3	External V_{DRIVE} power connector.
J4	External AVDD, AV_{SS}, and AGND power connector.
J5	External digital 5 V power connector.
J6	External +12 V, −12 V, and AGND power connector.

TEST POINTS

There are nine test points on the inputs to the AD7933/AD7934 on the evaluation board. These enable the user to have easy access to these signals for probing, evaluation, and debugging.

EVAL-CONTROL-BRD2 OPERATION

The evaluation board can be operated as a standalone unit or in conjunction with the EVAL-CONTROL-BRD2. The EVAL-CONTROL-BRD2 is available from Analog Devices under the order entry EVAL-CONTROL BRD2.

When interfacing the EVAL-AD7933/AD7934 directly to the EVAL-CONTROL-BRD2, all supplies and control signals to operate the AD7933/AD7934 board are provided by the EVAL-CONTROL-BRD2.

Due to the nature of the DSP interface on the EVAL-CONTROL-BRD2, AD7933/AD7934 sampling rates greater than 800 kSPS are not supported when interfacing this evaluation board directly to the EVAL-CONTROL-BRD2.

Software to communicate with the EVAL-CONTROL-BRD2 and AD7933/AD7934 is provided with the AD7933/AD7934 evaluation board package (see the Evaluation Board Software section). This EVAL-CONTROL-BRD2 also operates with all Analog Devices evaluation boards ending with the letters CB.

The 96-way connector on the EVAL-AD7933/AD7934CB plugs directly into the 96-way connector on the EVAL-CONTROL-BRD2. The EVAL-CONTROL-BRD2 provides all the supplies for the evaluation board. It is powered from a 12 V ac transformer. Suitable transformers are available from Analog Devices as an accessory under the following part numbers:

- EVAL-110VAC-US (for use in the U.S. or Japan)
- EVAL-220VAC-UK (for use in the U.K.)
- EVAL-220VAC-EU (for use in Europe)

These transformers are also available from other suppliers, including Digi-Key Corporation (U.S.) and Campbell Collins Ltd. (U.K.).

Connection between the EVAL-CONTROL-BRD2 and the serial port of a PC is via a standard Centronics printer port cable that is provided with the EVAL-CONTROL-BRD2. Refer to the manual accompanying the EVAL-CONTROL-BRD2 for more details.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7933/AD7934 kit includes a CD-ROM containing software that controls and evaluates the performance of the AD7933/AD7934 when it is operated with the EVAL-CONTROL-BRD2. When you insert the CD into a PC, an installation program automatically begins. This program installs the evaluation software onto your machine and installs the data sheet for the evaluation board, as well as the data sheet for the AD7933/AD7934 and the data sheet for the EVAL-CONTROL-BRD2. All literature on the CD is in Adobe® portable documentation format and requires Acrobat Reader™ to be viewed or printed. The user interface on the PC is a dedicated program written especially for the AD7933/AD7934 when operating with the EVAL-CONTROL-BRD2.

SETTING UP THE EVALUATION BOARD/ EVAL-CONTROL-BRD2

This section describes how the evaluation board, the EVAL-CONTROL-BRD2, and the software should be set up for the user to begin using the complete system.

1. Connect the EVAL-CONTROL-BRD2 and evaluation board together, using the 96-way connector.
2. Apply power to the EVAL-CONTROL-BRD2 via a 12 V ac transformer.
3. At this stage, the red LED on the EVAL-CONTROL-BRD2 should be flashing, indicating that the EVAL-CONTROL-BRD2 is functional and ready to receive instructions.

Be sure to install the software before connecting the printer port cable between the EVAL-CONTROL-BRD2 and the PC. This ensures that the printer port initializes properly. You can then connect the printer port cable between the PC and the EVAL-CONTROL-BRD2.

USING THE SOFTWARE

When the software runs, the window shown in Figure 3 appears. Its main function is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain.

The upper third of the window contains the menu bar, the control buttons, the selection options, and the busy status.

Menu Bar

The menu bar consists of **File**, **Config**, **Channel,** and **About**.

File Menu

The options from this menu include the following:

1. **Load Raw Data.** Selecting this option allows you to load data that was saved by the software during a previous session.
2. **Save Raw Data.** Selecting this option allows you to save the current set of sample data points. The data can be reloaded to the EVAL-CONTROL-BRD2 software or can be used by other programs for further analysis.
3. **Save Binary Data.** Selecting this option allows you to save the current set of sample data points. The data is saved in binary format as a text file. This method can be useful for examining code flicker, looking for stuck bits, and more.
4. **Exit.** Selecting this option quits the program.

Config Menu

The **Config** menu allows you to set up certain operating conditions in the ADC control register, such as power management, output coding, internal or external reference, and the analog input range.

Channel Menu

The **Channel** menu allows you to choose analog input type (single-ended, differential, or pseudo differential), which analog input to convert on, and whether the on-chip sequencer is used.

About Menu

The **About** menu gives you information about the version of the software.

Control Buttons

The control buttons allow you to take samples, reset the board, exit the program, and open the load configuration window (see Figure 4) to load a configuration file by clicking on **Device Select**.

Busy Status, Selection Windows, and Codes/Volts

The **Busy Status** indicates when the evaluation board is busy.

The selection windows allow you to change the sampling frequency, the number of samples to upload, and the data display from code to volts.

The **Codes/Volts** button**,** located to the right of the **Num Samples** drop-down list box, determines whether the data is displayed in volts or codes. It switches from **Code** to **Volts** or **Volts** to **Code** when it is clicked.

Digital Storage Oscilloscopes

The middle third of the window is a digital storage oscilloscope (DSO) that allows you to display a waveform, a histogram, or an FFT. When samples are uploaded from the EVAL-CONTROL-BRD2, they are displayed here. The samples can be displayed either as integer values or as voltages. At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a particular sample, if required. The right side of the middle section contains information about the samples taken, for example, mininum/maximum code or voltage, the spread, the standard deviation, and the mean.

The lower third of the window is also a DSO that lets you display a waveform, a histogram, or an FFT. The FFT (the default option) is typically used when you are concerned with examining the performance of the ADC in the frequency domain. The histogram gives an indication of ADC performance with dc signals.

The option displayed can be changed by double clicking on the waveform, histogram, and FFT buttons. The right side of the lower section contains information about the samples taken, for example, ac specifications.

Taking Samples

When you click **Sample**, the software instructs the EVAL-CONTROL-BRD2 to take the required number of samples at the required frequency from the evaluation board. The AD7933/AD7934 evaluation board runs up to 800 kSPS, so you can choose the sampling frequency up to this rate. You can also choose the number of samples to be taken.

The maximum sampling frequencies, as described in the AD7933/AD7934 data sheets, can be achieved only when operating the evaluation board as a standalone unit. This is a software limitation.

The samples taken are then uploaded and displayed. An FFT and a histogram are also calculated and displayed. If you click **Continuous**, the software repeats the process indefinitely until you click **Stop**. (The **Continuous** buttom switches to **Stop** when clicked.)

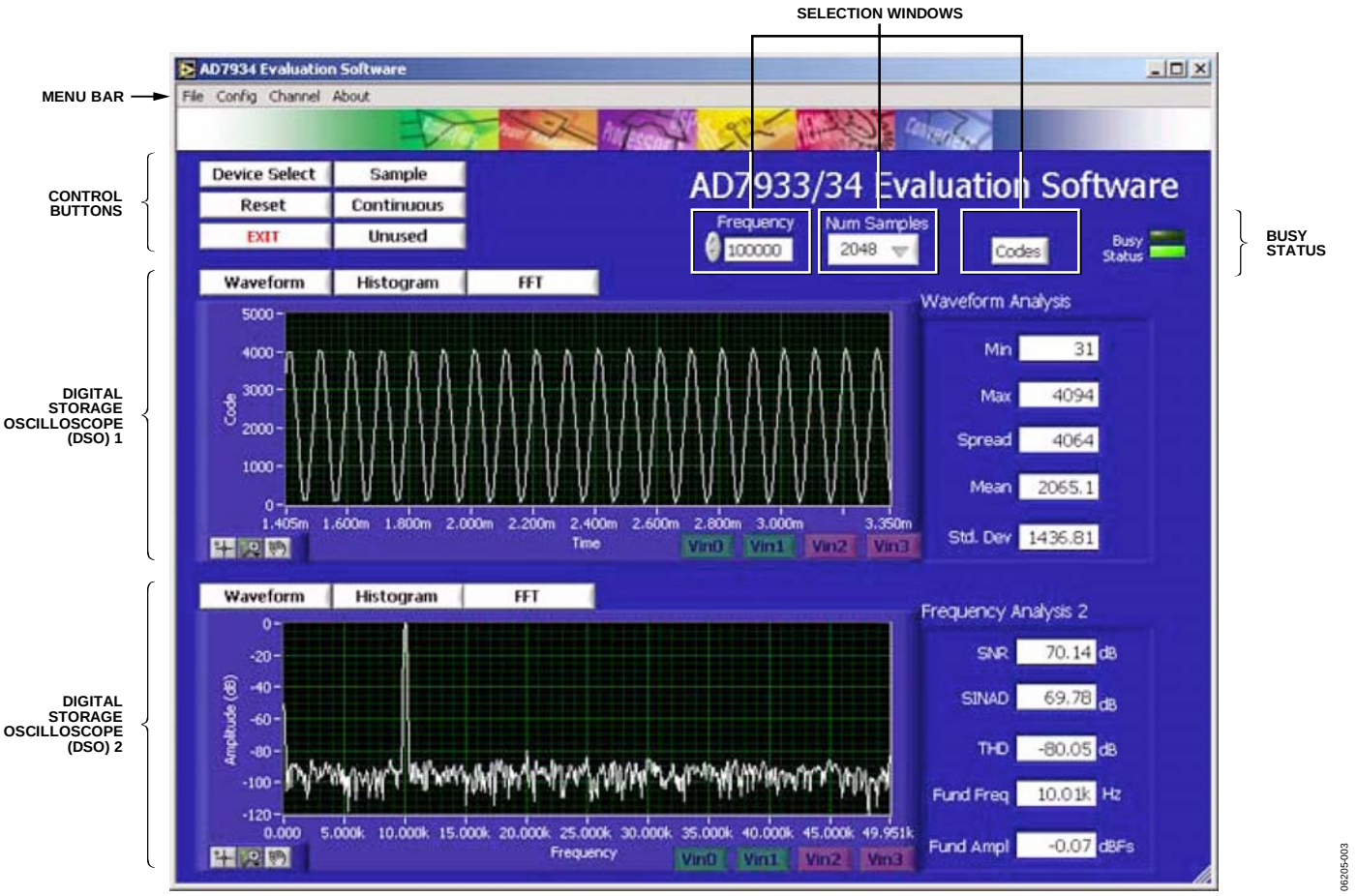

Figure 3. AD7933/AD7934 Main Window

CONFIGURING THE BOARDS

For the AD7933/AD7934 evaluation board and the EVAL-CONTROL-BRD2 to communicate with the software, the required configuration files must be loaded using the load configuration screen (see Figure 4). The list box on the top left of the configuration window shows the available configuration files, which are text-based files containing information about the particular evaluation board to be tested.

The configuration files give the EVAL-CONTROL-BRD2 software information on how the software and hardware should perform, including the part name, number of samples to take, default and maximum sampling frequency, power supply settings, the name of the DSP program to download, and other parameters.

When using the AD7933, load the **AD7933.cfg** file; and when using the AD7934, load the **AD7934.cfg** file.

1. Click the **Device Select** button on the main window (see Figure 3). This brings up the load configuration window.
2. Select the relevant configuration file and click **OK**.
3. The EVAL-CONTROL-BRD2 is reset, and the DSP program is downloaded. When the download is complete, the power supply settings indicated in the configuration file are set and you may hear some of the relays clicking.
4. The selection options (for example, number of samples and sampling frequency) are set to the default values specified by the configuration file; you can change these at will.

Typical Software Configuration File

The following is a typical software configuration file (*.cfg):

```
EVAL-CONTROL BOARD]
partname:AD7934
programname:ad7934.PRG

samplefrequency:100000
maxsamplefrequency:800000
samples:2048

+/-15V:on
dvdd:5:on
avdd:5:on
bus:on
;options 2scomp, binary
dataformat:binary
numberofbits:12
inputVmax:5
inputVmin:0
[endofconfig]
```

Operating with Different Voltage Reference Inputs

The functionality of the AD7933/AD7934 allows a variable reference input in the range 100 mV to V_{DD}. The allowable reference input depends on the power supply and the analog input type to ensure the maximum ratings of the device are not exceeded. For 5 V operation, the standard reference on the evaluation board is 2.5 V, which corresponds to a differential input of 5 V.

This maximum input voltage is set up in the configuration file (see the **inputVmax: 5** in the configuration file in the Typical Software Configuration File section). As you change the reference input, you must be sure to adjust the **inputVmax** figure in the configuration file to ensure that accurate data is displayed in the software.

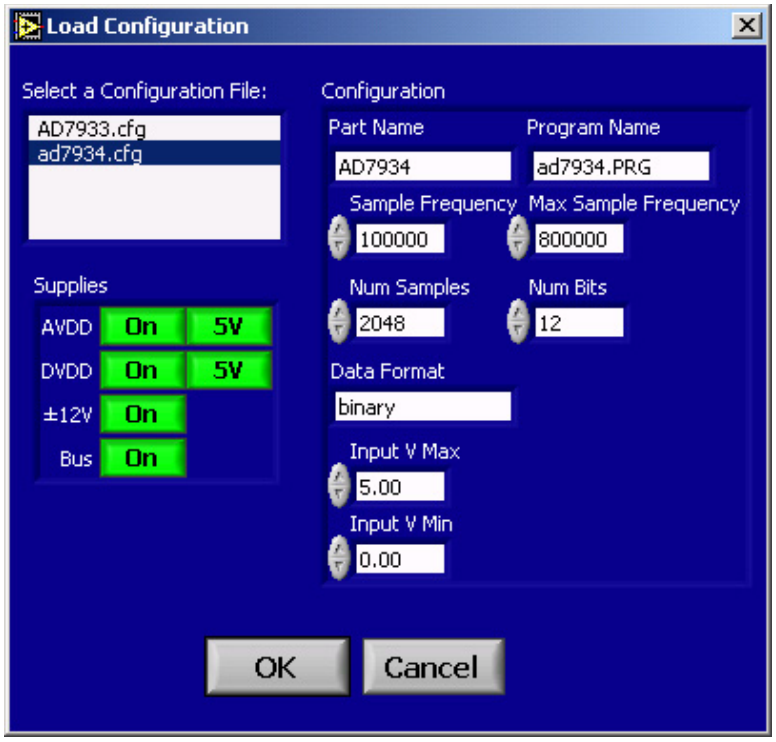

Figure 4. AD7933/AD7934 Load Configuration Window

EVALUATION BOARD SCHEMATICS AND ARTWORK

Evaluation board schematics and artwork are shown in Figure 5 to Figure 11.

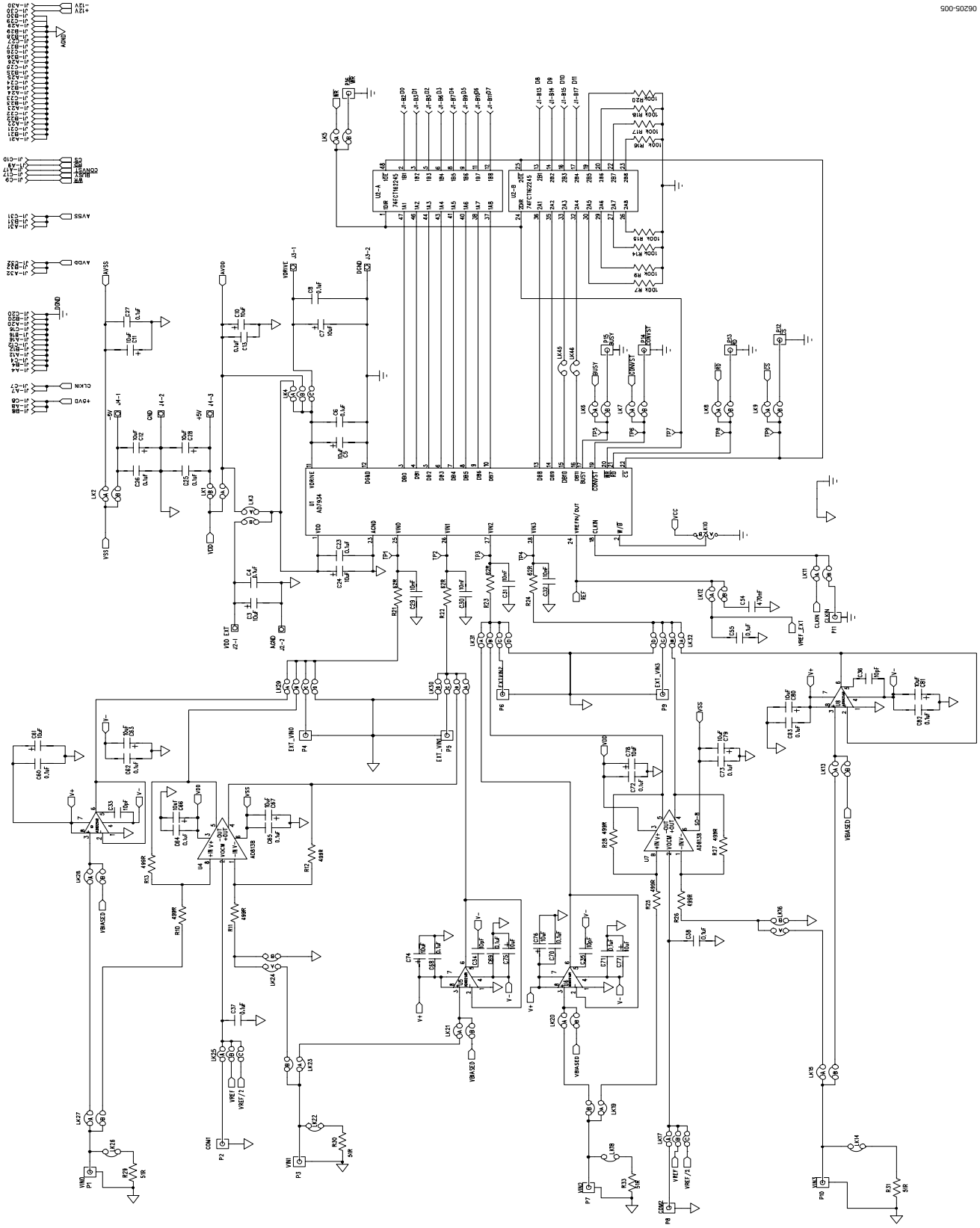

Figure 5. AD7933/AD7934 Evaluation Board Circuit Diagram, Page 1

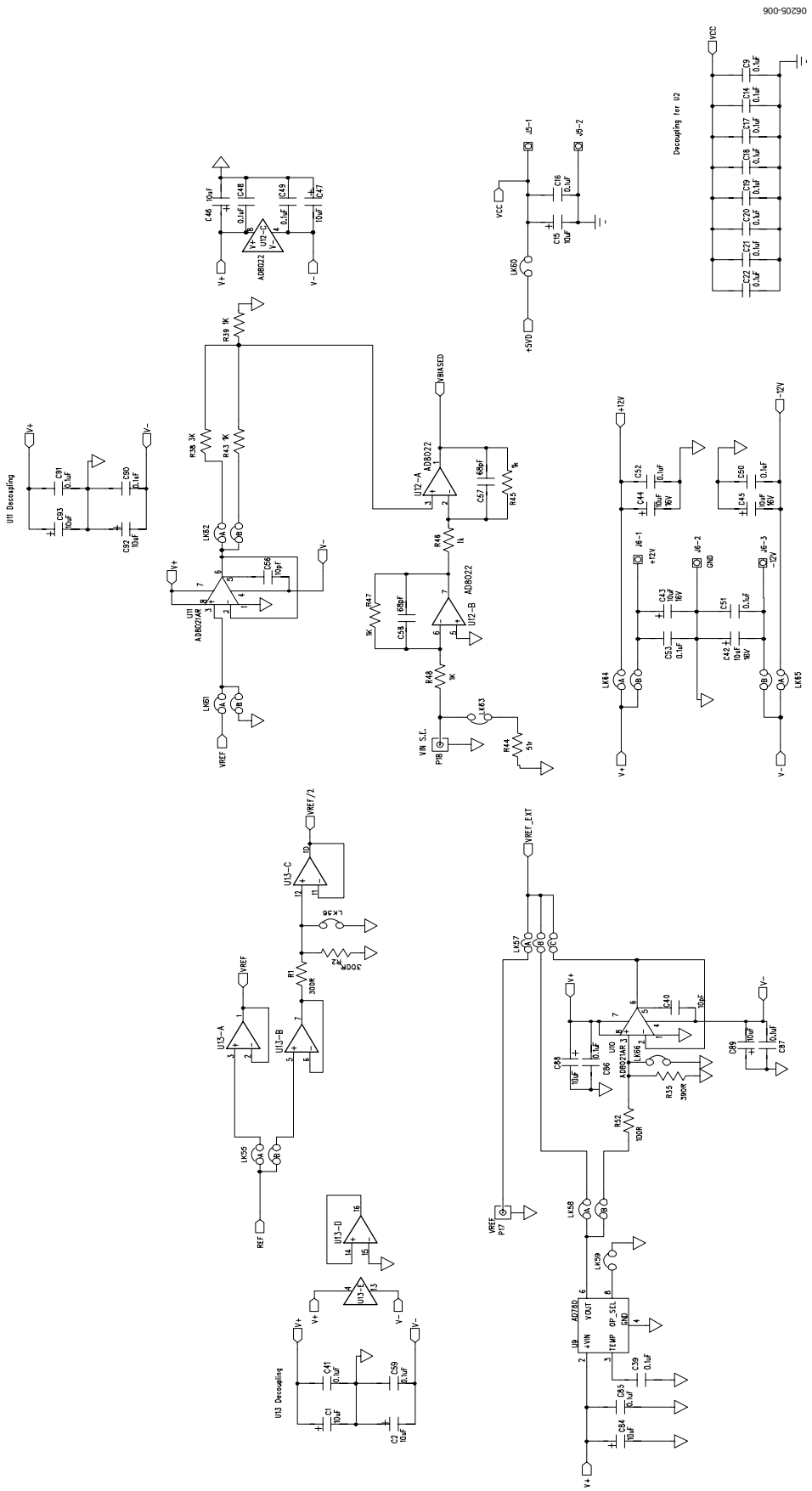

Figure 6. AD7933/AD7934 Evaluation Board Circuit Diagram, Page 2

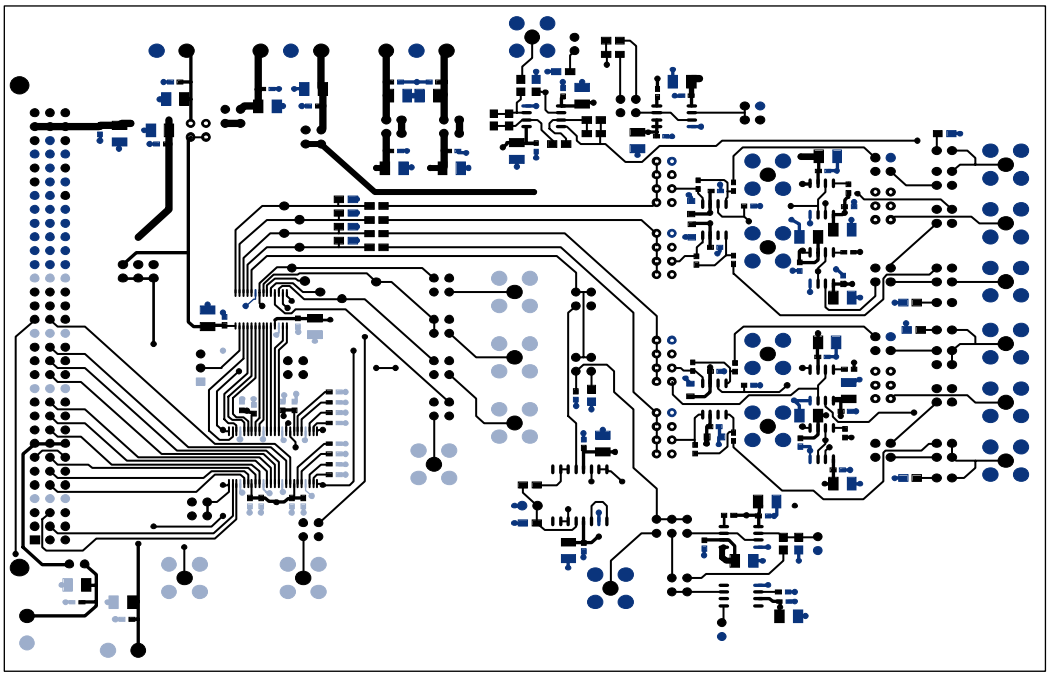

Figure 7. AD7933/AD7934 Evaluation Board—Component Side Artwork

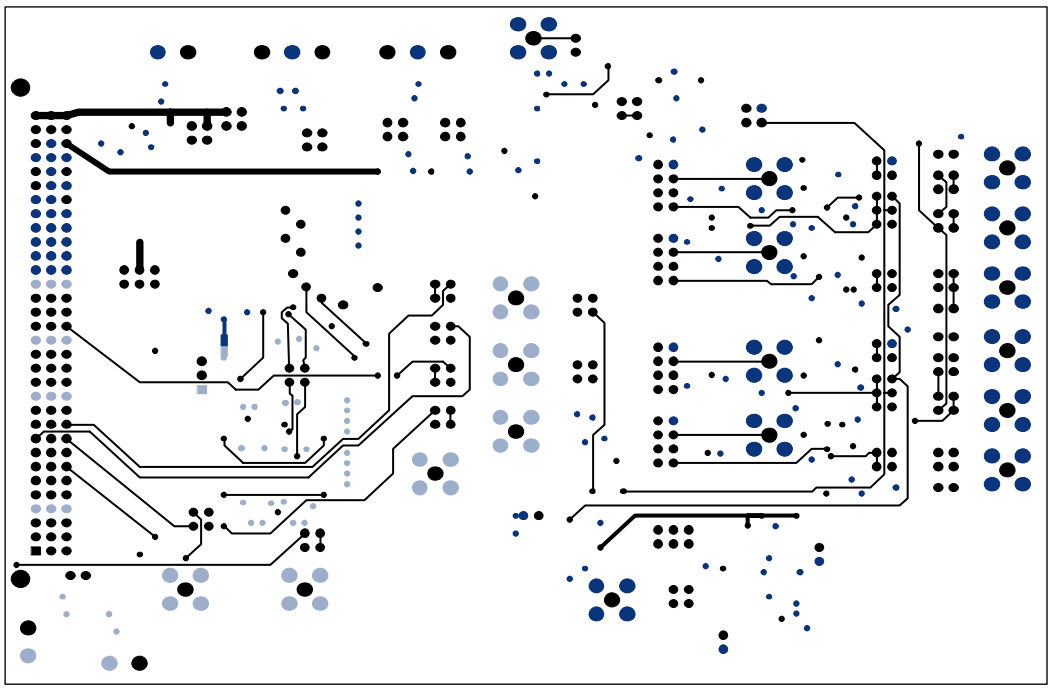

Figure 8. AD7933/AD7934 Evaluation Board—Solder Side Artwork

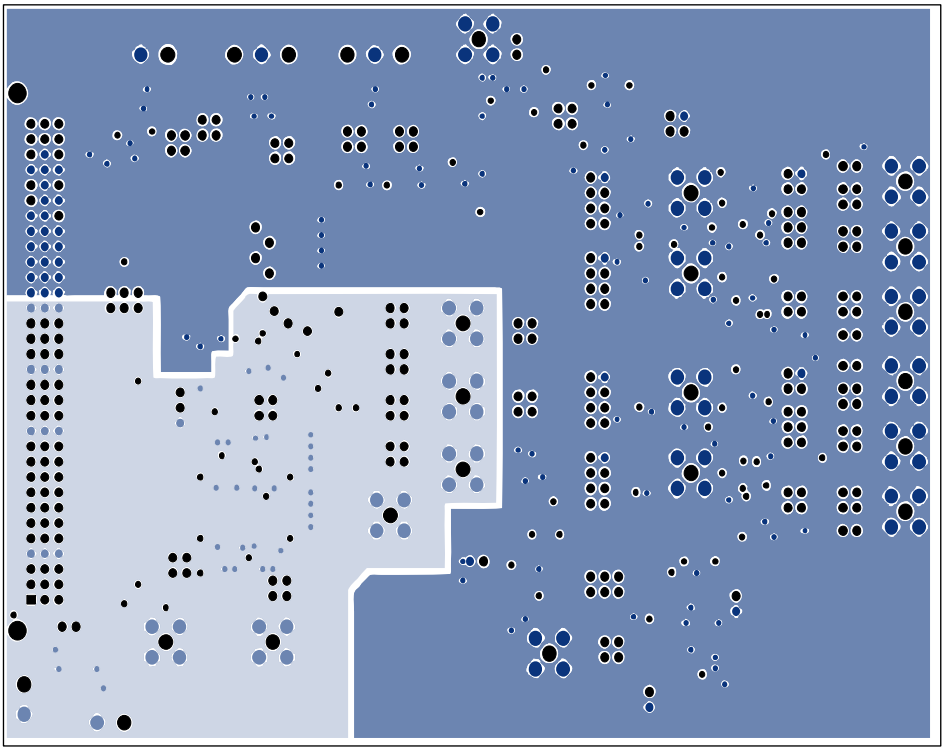

Figure 9. AD7933/AD7934 Evaluation Board—Layer 2

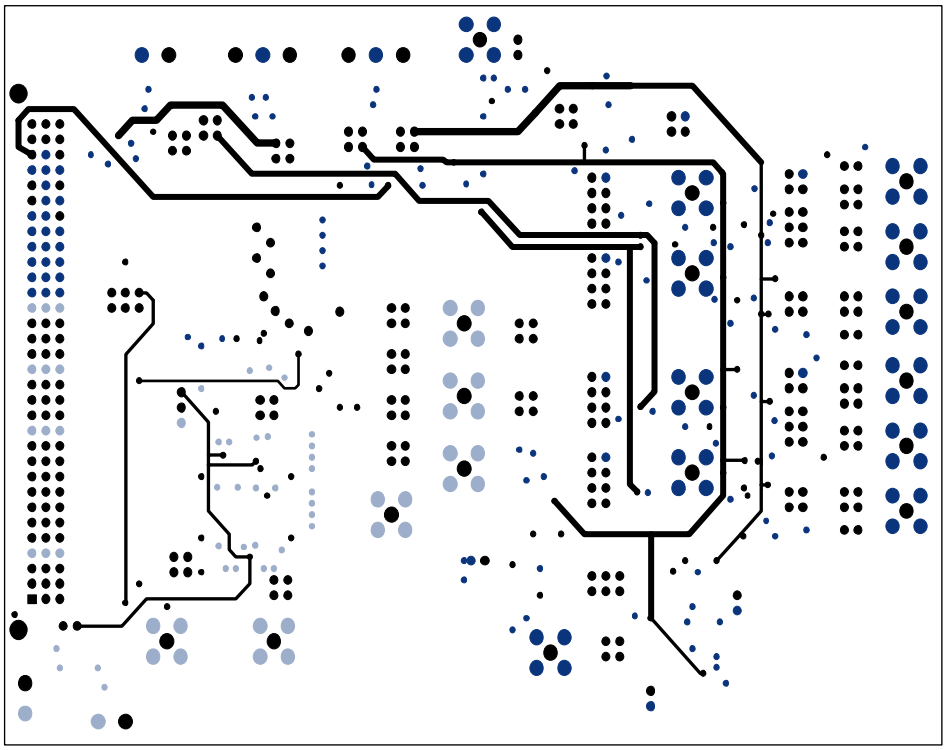

Figure 10. AD7933/AD7934 Evaluation Board—Layer 3

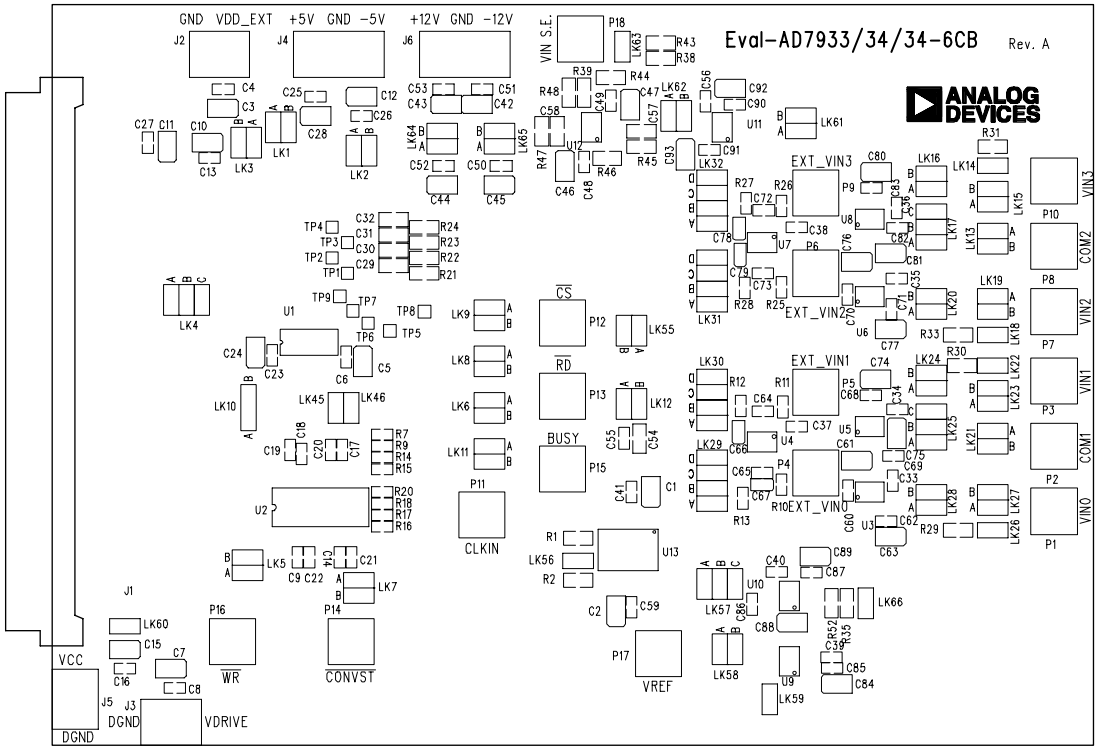

Figure 11. AD7933/AD7934 Evaluation Board—Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 11.

Qty	Reference Designator	Description	Manufacturer/ Distributor	Order Number
1	U1	AD7934/AD7933	Analog Devices	AD7934BRU/AD7933BRU
1	U2	74FCT162245		IDT74FCT
6	U3, U5, U6, U8, U10, U11	AD8021	Analog Devices	AD8021AR
2	U4, U7	AD8138	Analog Devices	AD8138AR
1	U9	AD780	Analog Devices	AD780AN
1	U12	AD8022	Analog Devices	AD8022AR
1	U13	AD713	Analog Devices	AD713JR-16
30	C1 to C3, C5, C7, C10 to C12, C15, C24, C28, C42 to C47, C61, C63, C74 to C77, C80, C81, C84, C88, C89, C92, C93	10 µF tantalum capacitor, 16 V	Farnell	FEC 197-427[1]
46	C4, C6, C8, C9, C13, C14, C16 to C23, C25 to C27, C37 to C39, C41, C48 to C53, C55, C59, C60, C62, C64, C65, C68 to C73, C82, C83, C85 to C87, C90, C91	0.1 µF ceramic capacitor, SMD 0603	Farnell	FEC 317-287[1]
4	C29 to C32	10 nF ceramic capacitor, SMD 0805	Farnell	FEC 499-225[1]
6	C33 to C36, C40, C56	10 pF ceramic capacitor, SMD 0603	Farnell	FEC 751-078[1]
1	C54	470 nF ceramic capacitor, SMD0805		
2	C57, C58	68 pF ceramic capacitor, SMD0805	Farnell	FEC 722-066[1]
3	C66, C67, C79	10 µF tantalum capacitor, 10 V	Farnell	FEC 331-3888[1]
9	R7, R9, R14 to R18, R20	100 kΩ resistor, SMD0805	Farnell	FEC 771-272[1]
8	R10 to R13, R25 to R28	499 Ω resistor, SMD0603	Farnell	FEC 422-2726[1]
4	R21 to R24	62 Ω resistor, SMD0805	Farnell	FEC 321-7917[1]
6	R29 to R31, R33, R44	51 Ω resistor, SMD0805	Farnell	FEC 321-7905[1]
1	R35	390 Ω resistor, SMD0805	Farnell	FEC 613-046[1]
1	R38	3 kΩ resistor, SMD0805	Farnell	FEC 771-399[1]
6	R39, R43, R45 to 48	1 kΩ resistor, SMD0805	Farnell	FEC 613-095[1]
1	R52	100 Ω resistor, SMD0805	Farnell	FEC 911-732[1]
1	J1	CON\41612\96 Connector	Siemens	FEC 225-393[1]
2	J4 and J6	3-pin terminal block	Lumberg	FEC 304-4980[1]
3	J2, J3, J5	2-pin terminal block	Lumberg	FEC 304-4889[1]
11	LK14, LK18, LK22, LK26, LK45, LK46, LK56, LK59, LK60, LK63, LK66	1-way jumper (2 × 1)	Harwin	FEC 511-791[1]
26	LK1 to LK3, LK5 to LK9, LK11 to LK13, LK15, LK16, LK19 to LK21, LK23, LK24, LK27, LK28, LK55, LK58, LK61, LK62, LK64, LK65	2-way jumper (2 × 2)	Harwin	FEC 511-791[1]
5	LK4, LK17, LK25, LK27, LK57	3-way jumper (2 × 3)	Harwin	FEC 511-780[1]
4	LK29 to LK32	4-way jumper (2 × 4)	Harwin	FEC 511-791[1]
1	LK10	2-way jumper, SIP3	Harwin	FEC 329-1698[1]
46	LK1 to LK46	Shorting link	Berg	FEC 150-411[1]
18	P1 to P18	Gold 50_ SMB jack	M/ACom	FEC 310-682[1]
9	TP1 to TP9	Test point	William Hughes	FEC 240-333[1]
4	Each corner	Stick-on feet	3M	FEC 148-922[1]

[1] FEC = Farnell Electronics.

ORDERING GUIDE

Model	Package Description
EVAL-AD7933CB	AD7933 Evaluation Board
EVAL-AD7934CB	AD7934 Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

EB06205-0-8/07(0)