ANALOG DEVICES

AN-368
APPLICATION NOTE

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Evaluation Board for the AD7701/AD7703 Sigma Delta A/D Converters

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INTRODUCTION

This application note describes the evaluation board for the AD7701 and AD7703 A/D converters. These converters utilize sigma delta techniques to offer exceptional performance. The AD7701 is a 16-bit device with 0.0015% FSR INL error and no missing codes. The AD7703 is a 20-bit device with 0.0003% FSR INL error and no missing codes. Both parts (which are pin compatible) have a self-calibration mode which removes internal offset and gain errors and a system calibration mode which removes external circuit offset and gain errors. Both devices have a flexible synchronous serial interface which allows the ADCs to connect directly to digital signal processors and microcontrollers. In addition, the AD7701 has an asynchronous interface for use with UARTs. Full data on the AD7701 and AD7703 is available in data sheets from Analog Devices and should be consulted in conjunction with this application note when using the evaluation board.

The board has been designed to enable all the features of the converters to be fully evaluated. These features include analog input range, calibration mode, interface mode selection, master clock rate and output data rates.

The board operates from +5 volt and −5 volt power supplies. On-board components include a 2.5 V reference, clock generation circuitry, a decimation counter and parallel interface circuitry. The three different interface options are as follows: a parallel output port suitable for μC (microcontroller) and DSP (digital signal processor) interfacing, an asynchronous RS-232 interface (AD7701 only), a synchronous serial interface suitable for the serial ports of both microcontroller and DSP machines.

A full circuit diagram for the board is shown in Figure 5. The board layout and silkscreen are given in Figures 7, 8 and 9.

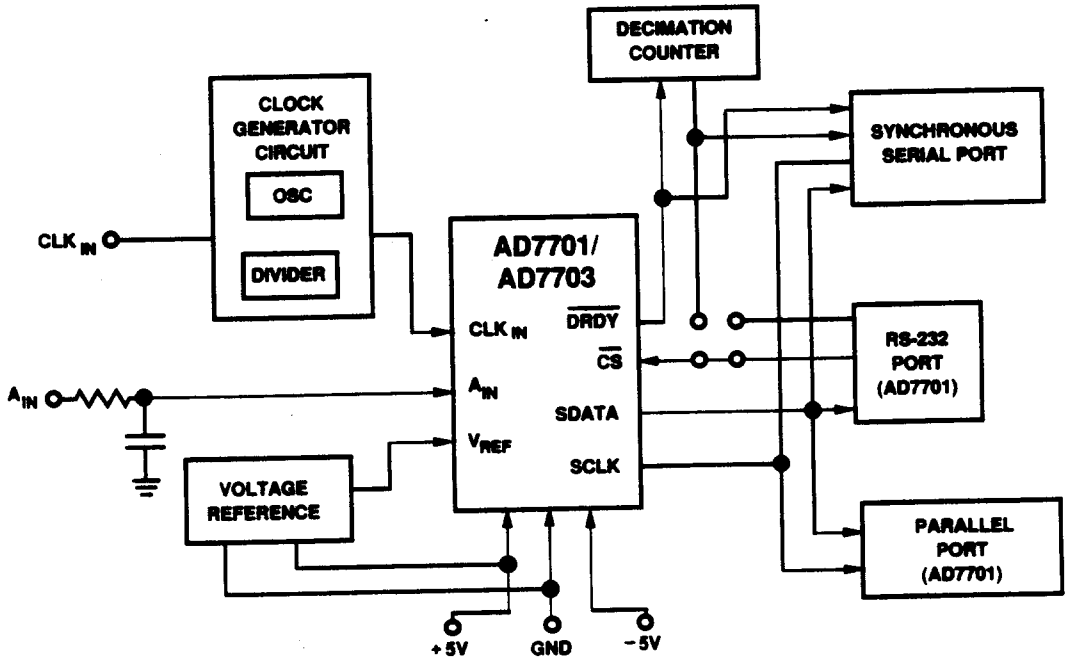

Figure 1. Evaluation Board Block Diagram

LINK OPTIONS

The evaluation board has several link options available and these are summarized in Table I below.

Link No.	Function
LK1	This link selects either the on-board oscillator (INT) or an external clock source (EXT) as the input to the clock generator section.
LK2	This allows any of the divider output rates to be used as the input clock to the AD7701/AD7703.
LK3	This is the baud rate selector when the AD7701 is in the AC (Asynchronous Communications) interface mode. Baud rates between 1200 and 19200 are available.
LK4	This link sets the divide ratio of the decimation counter.
LK5	This selects one of the three interface modes of the AD7701 and one of two modes of the AD7703.
LK6	This allows the calibration and sleep modes to be selected. It also selects the analog input range and determines whether the device does a self-calibration or a system calibration.
LK7	In the parallel interface mode for the board, this link configures the Data Acknowledge Signal (DACK) to be either active high or active low.
LK8	This link allows the $\overline{CS}$ input of the device to be controlled either by the output of the decimation counter or by the DTR input from the RS-232 interface.
LK9	This connects the on-board-generated baud clock to the device SCLK input.

Table I. Link Options

POWER SUPPLIES AND GROUNDING

The board is powered from a ±5 V supply. Both supplies are decoupled to ground with 10 μF tantalum and 0.1 μF ceramic disc capacitors. Power for the digital section of the board and the DV_{DD} pin of the AD7701/AD7703 is routed separately from the power for the analog section and AV_{DD} on the AD7701/AD7703. These analog and digital power lines are joined together only at one point which is at the input to the board. The four supply pins of the AD7701/AD7703 are each decoupled with 0.1 μF capacitors.

The evaluation board uses extensive ground planing to minimize any high frequency noise interference from the on-board clocks or any other sources. Once again, the ground planing for the analog section is kept separate from that for the digital section and they are joined only at the board input.

BOARD INITIALIZATION

On power-up, the first step is to calibrate the device and set up the operating conditions. The evaluation board offers two options here. The control pins (CAL, SC1, SC2, BP/$\overline{UP}$ and $\overline{SLEEP}$) can be set either by the DIP switch, SW1, and the CAL pushbutton switch, SW2, or directly by LK6. If the board is operating in a stand-alone mode, the DIP switch, SW1, and the CAL pushbutton switch, SW2, set up the operating conditions and do the calibration. The truth table for the DIP switch settings is shown in Table II. Table III then shows the key for these settings. When SW2 is activated, it will initiate a calibration cycle in accordance with the SW1-1 and SW1-2 settings. The CAL pin should be activated whenever power is applied to the board or whenever the calibration mode is changed on SW1. If a processor is being used to control the board, LK6 can be driven by a port to set up the operating conditions and do the calibration. The DIP switches should be in the off position if LK6 is being used to drive the control pins.

Switch	ON	OFF
SW1-1	SC1 = 0	SC1 = 1
SW1-2	SC2 = 0	SC2 = 1
SW1-3	Unipolar Input	Bipolar Input
SW1-4	Sleep Mode	Normal Mode

Table II. SW1 Settings

AD7701/AD7703 INTERFACE MODE SELECTION

The AD7701 may be set up for one of three serial interface modes, and the AD7703 has two serial interface modes. These are controlled on the evaluation board by link option LK5. The modes are as follows:

1. The Synchronous Self-Clocking (SSC) mode which is intended for interfacing to digital signal processors and serial-to-parallel shift registers. In this case, data is clocked out on the falling edge of the internally generated SCLK.
2. The Synchronous External Clocking (SEC) mode, which is intended for interfacing to microcontrollers

CAL	SC1	SC2	CAL TYPE	ZERO REFERENCE	FS REFERENCE	SEQUENCE
⎍	0	0	Self-Cal	AGND	V_{REF}	One Step
⎍	1	1	System Offset	A_{IN}	–	1st Step
⎍	0	1	System Gain	–	A_{IN}	2nd Step
⎍	1	0	System Offset	A_{IN}	V_{REF}	One Step

Table III. Calibration Truth Table

such as the 8051 and 68HC11. In this case an external SCLK is applied to the AD7701/AD7703, and data is clocked out on its falling edge.

3. The Asynchronous Communications (AC) mode is present on the AD7701 only and is intended for interfacing to UARTs. In this mode, no clock is used. Data is clocked out in two serial bytes. Each byte has one start bit and two stop bits.

LK5 Position	Interface Mode
SSC	Synchronous Self-Clocking
SEC	Synchronous External Clocking
AC	Asynchronous Communication

Table IV. Interface Mode Selection

Table IV gives the link option positions for the various interface modes.

ANALOG INPUT SECTION

The analog input to the board is applied to the miniature BNC connector labelled A_{IN}. R12 and C22 provide filtering of any high frequency noise which may be present on the analog input. R12 also provides current limiting in the event of an input signal which exceeds the AV_{DD} supply.

The reference for the AD7701/AD7703 is provided by IC5 (the AD580, 2.5 V reference). This is decoupled with 10 μF and 0.1 μF to signal ground. The RC combination at the reference output act as a filter for any high frequency noise present. In addition, the AD580 output is buffered by IC12 (TLC271) and is available at V_{REFS} and V_{REFF} so that it can be used as a reference for other elements in the system.

CLOCK GENERATION

The evaluation board Clock Generator section is comprised of X1 (4.9152 MHz crystal), IC1, IC2 and associated passive components. Link option LK1 allows the user to choose between an externally supplied clock and that generated on the board. With LK1 in the EXT position, the input applied at the BNC connector labelled CLKIN is applied to the input of the counter IC2. This input should be +5 V CMOS compatible. Link option LK2 then selects a sub-multiple of this to drive the AD7701/AD7703 CLKIN pin. If LK1 is in the INT position, then the on-board 4.9152 MHz oscillator is selected as the counter input.

Counter IC2 (74HC4040) divides the input clock by 2^n where n = 0, 1, . . . 7. Table V shows the resulting CLKIN frequency for the various link positions when the on-board 4.9152 MHz oscillator is the counter input.

The AD7701/AD7703 has its own on-chip oscillator which needs only an external crystal or ceramic resonator to operate. Note however that ceramic resonators and low frequency crystals will need loading capacitors to operate correctly.

LK2 Position	CLKIN Frequency
0	4.9152 MHz
1	2.4576 MHz
2	1.2288 MHz
3	614.4 kHz
4	307.2 kHz
5	153.6 kHz
6	76.8 kHz
7	38.4 kHz

Table V. Choosing CLKIN Frequency for the AD7701/AD7703

The evaluation board allows operation with the on-chip oscillator. The desired crystal should be inserted in the X2 slot on the board. This crystal is now directly connected between the CLKIN pin and CLKOUT pin of the AD7701/AD7703. In addition, the wire link located directly above TP8 should be removed to disconnect the clock coming from IC2. Note that in addition to the X2 slot, there is also provision made for loading capacitors on the board. The space for these is located directly above X2.

DECIMATION COUNTER

Each time a data word is available for output from the AD7701/AD7703, the $\overline{DRDY}$ line goes low. If the $\overline{DRDY}$ line is tied directly to the device $\overline{CS}$ input, it will output data every time a data word is presented to the output pin. The output update rate is $f_{CLKIN}/1024$. Thus, for a CLKIN frequency of 4.096 MHz, the output update rate and output data rate will both be 4 kHz. Some applications will not require such a high output data rate and it is possible to reduce this by simply dividing down the $\overline{DRDY}$ signal before driving $\overline{CS}$. This function is known as decimation and is performed on the evaluation board by IC3, IC8a and Link Options LK4 and LK8. With a link inserted in LK8, Position A, the output of the counter IC3 drives the AD7701/AD7703 $\overline{CS}$ input. In this case, the counter accumulates 2^n counts (where n = 0 to 11) at which time the selected output enables the $\overline{CS}$ input of the AD7701/AD7703. The D input to flip-flop IC8a is enabled to a "1" at the same time as $\overline{CS}$ goes low. When $\overline{DRDY}$ returns high, IC8a is toggled and resets the counter IC3 which terminates the $\overline{CS}$ enable. Table VI gives the divide ratios for the LK4 settings and also gives the resulting output data rate, for a 4.096 MHz CLKIN.

EVALUATION BOARD INTERFACING

The board offers three separate interfaces: a synchronous serial port; an RS-232 port and a 16-bit parallel port.

Synchronous Serial Port

The synchronous serial port is available at the subminiature D connector, SKT1. The pin configuration for this is given in Figure 2. The port can be used in both the

LK4 Position	Divide Ratio	Output Rate (CLKIN = 4.096 MHz)
0	1	4 kHz
1	2	2 kHz
2	4	1 kHz
3	8	500 Hz
4	16	250 Hz
5	32	125 Hz
6	64	62.5 Hz
7	128	31.1 Hz
8	256	15.6 Hz
9	512	7.8 Hz
10	1024	3.9 Hz
11	2048	1.9 Hz

Table VI. Setting AD7701/AD7703 Output Data Rate

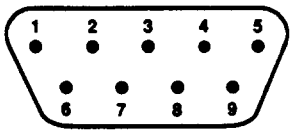

Figure 2. Pin Configuration for SKT1, Synchronous Serial Port

Synchronous Self-Clocking Mode and the Synchronous External Clocking mode. The port has six lines which are described below.

DGND Ground reference point

$\overline{CS}$ This buffered input controls the AD7701/AD7703 $\overline{CS}$ input

DR This buffered output is the $\overline{DRDY}$ signal from the AD7701/AD7703

SD This is the buffered SDATA output of the AD7701/AD7703

SCO Serial Clock Output. When the device is operating in the SSC mode, the serial clock from the AD7701/AD7703 is buffered and available at this pin. The output three state buffer is controlled by the MODE pin of the device. If the MODE pin is low (indicating SEC mode), the three state buffer is disabled.

SCI Serial Clock Input. When the device is operating in the SEC mode, the external serial clock is applied to this terminal and goes via the three state buffer to the SCLK pin. If the AD7701/AD7703 MODE pin is high (indicating SSC mode), then the three state buffer is disabled.

In the SSC mode serial data and serial clock are output from the AD7701/AD7703 whenever the $\overline{CS}$ line is activated. In order to control this by a processor port connected at SKT1, it is important to place the jumper in LK8 in position C (No Connection). This removes the decimation counter output from controlling the $\overline{CS}$ line.

In the SEC mode serial data is clocked out on the falling edge of the externally supplied serial clock whenever the $\overline{CS}$ line is activated. In order to have full control with a processor in this mode, the jumper in LK8 must be placed in position C and the jumper in LK9 must be placed in position B. These are both "No Connection" positions and disable the Decimation Counter control of $\overline{CS}$ and the Baud Rate Generator control of SCLK.

RS-232 Port (AD7701 Only)

The RS-232 port is available at the subminiature D connector, SKT2. The pin configuration for this is given in Figure 3.

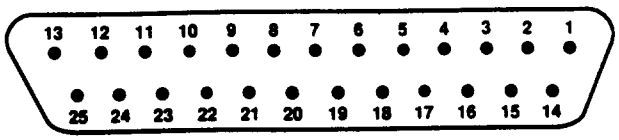

Figure 3. Pin Configuration for SKT2, RS-232 Port

When the AD7701 is set up for the AC (Asynchronous Communications) mode by tying the MODE pin to −5 V, data is transmitted in two serial bytes in UART-compatible format. An external SCLK sets the baud rate. On the evaluation board, this clock is derived from the counter IC2. Its frequency is set by the link option, LK3. The baud rates corresponding to the link positions are given in Table VII. Note that if the on-board baud clock is to be used, the jumper on LK9 should be in position A. This makes the connection between the output of IC2 and the AD7701 SCLK input. Alternatively, the baud clock can be controlled by a clock input to the SCI input at SKT1. In this case the jumper on LK9 should be in position B.

LK3 Position	Baud Rate Clock (CLKIN = 4.9152 MHz)
8	19.2 kHz
9	9.6 kHz
10	4.8 kHz
11	2.4 kHz
12	1.2 kHz

Table VII. Baud Rate Settings

The $\overline{DRDY}$ output from the AD7701 signals the CTS (Clear To Send) line of the RS-232 interface when data is available. The remote terminal then responds with a DTR (Data Terminal Ready) signal. When LK8 is set to position B, the DTR signal drives the $\overline{CS}$ input of the AD7701 and initiates the data transfer.

IC11, the MC145406 RS-232 Interface chip converts the TTL levels from the AD7701 to the required ±5 V signals to drive the remote terminal or takes the ±5 V signals and converts them into TTL levels. The RS-232 interface on the evaluation board is fully functional but does not comply with all the requirements of the EIA RS-232 standard. When the MC145406 receiver/driver chip is operated from ±5 V supplies rather than ±6 V, its driver output swing is reduced below the EIA specified limits. In practical applications this signal swing limitation only reduces the length of cable the circuit is capable of driving.

Parallel Port (AD7701 Only)

The 16-bit Parallel Port is available at two sockets on the board, SKT3 and SKT4. The Eurocard Connector, SKT3, allows this board to be connected directly to the evaluation board for the ADSP-2100 Digital Signal Processor, which is available from Analog Devices. SKT4 provides a general purpose socket for interfacing to any other parallel systems. The pinout for SKT3 and SKT4 is given in Figure 4.

When using the parallel interface, the AD7701 should be set up to operate in the SSC mode (LK5 set at SSC). Activation of the $\overline{CS}$ input on the AD7701 will determine the rate at which it attempts to update the output shift registers IC9 and IC10. $\overline{CS}$ can be controlled by the decimation counter output (LK8 in position A) or remotely at

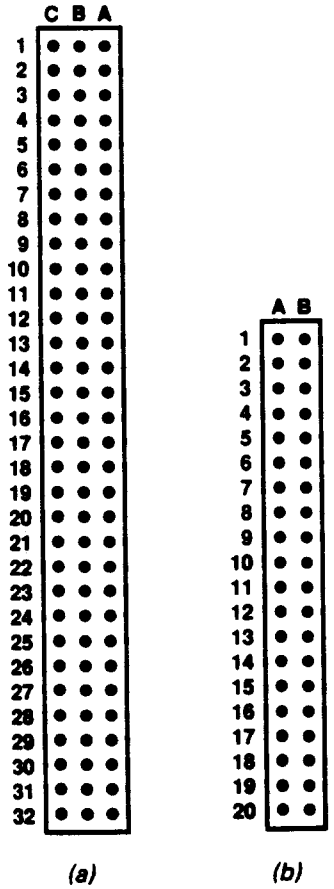

Figure 4. Pin Configurations for SKT3 (a) and SKT4 (b)

SKT1. If it is controlled remotely, LK4 must be in position 0 to ensure that the output register update and the remote $\overline{CS}$ occur at the same rate. When $\overline{CS}$ goes low, the 16-bit output data is clocked into the two 8-bit shift registers, IC9 and IC10. These are set up for shift right operation (S0 = 1, S1 = 0), and their three-state outputs are available at SKT3 and SKT4. A rising edge on Pin 2 of IC6 indicates that the output registers have been updated. This signal clocks the D-type flip-flop, IC8b to set its $\overline{Q}$ output low and indicate to the remote reading device that the registers have been updated and can be read. This is called the $\overline{PDR}$ (Parallel Data Ready) signal. The $\overline{PDR}$ signal also controls the S0 input of IC9 and IC10. When it goes low, the shift register outputs are held until a Data Acknowledge (DACK) signal is received from the remote device and resets flip-flop IC8b. In the ADSP-2100 interface, $\overline{PDR}$ drives an interrupt line in the processor. The service routine reads the 16-bit data by bringing $\overline{PCS}$ low and A0 high. When the data has been read it sends back a DACK signal to reenable the output shift registers. Note that LK7 allows the DACK signal to be either active high or low. If DACK is true when high, then LK7 should be in position A; whereas if DACK is true when low, LK7 should be in position B.

IC9 and IC10 are set up to be read in 16-bit parallel fashion with the low byte in IC9 and the high byte in IC10. They can also be configured to be read separately as two 8-bit bytes on an 8-bit bus. To do this, the Byte Wide Jumpers must be soldered in place. In addition, for proper "one byte at a time" address selection, the connections at Pin 10 of IC6 on the circuit board must be altered to control which register is to be read when A0 is a 1 and which is to be read when it is 0. This can be seen in Figure 5. For example, if the most significant byte is to be read when A0 is 0, IC10 should be enabled and IC9 disabled. The link between 4 and 5 on the board must be broken, and 1 must be joined to 4.

Link/ Switch	Position	Function
LK1	INT	On-board oscillator selected as input to clock generator section
LK2	0	IC2 counter divider ratio set at 1.
LK3	NC*	Baud rate selector not used.
LK4	0	Decimation counter divide ratio set at 1.
LK5	SSC	Synchronous self clocking interface mode selected.
LK6	NC*	Not used. SW1 sets the calibration mode.
LK7	A	DACK signal set to be active low.
LK8	A	Decimation counter output controls the $\overline{CS}$ input of the AD7701/AD7703..
LK9	B (NC*)	SCLK not controlled by the baud clock.
SW1-1	ON	Sets SC1 input at 0.
SW1-2	ON	Sets SC2 input at 0. With SC1, SC2 both set to 0, the device calibration mode is self-calibration of zero and full scale.
SW1-3	ON	Unipolar input range selected.
SW1-4	OFF	Normal mode (i.e., not low power Sleep mode) selected.

*NC = No Connection

Table VIII. Link and Switch Settings

SETUP CONDITIONS

In order to initially set up and verify that the evaluation board is functional, it is useful to set all the link and switch settings for a particular mode of operation. The settings, given in Table VIII, will set the board for the following: On-board 4.9152 MHz clock; unipolar analog input range; Self-calibration mode; 4.8 kHz output update rate; SSC Interface Mode. To obtain specified offset and full-scale performance, the CAL switch, SW2 should be depressed immediately after power-up. Figure 6 gives the link and switch positions on the board in order to ease setup.

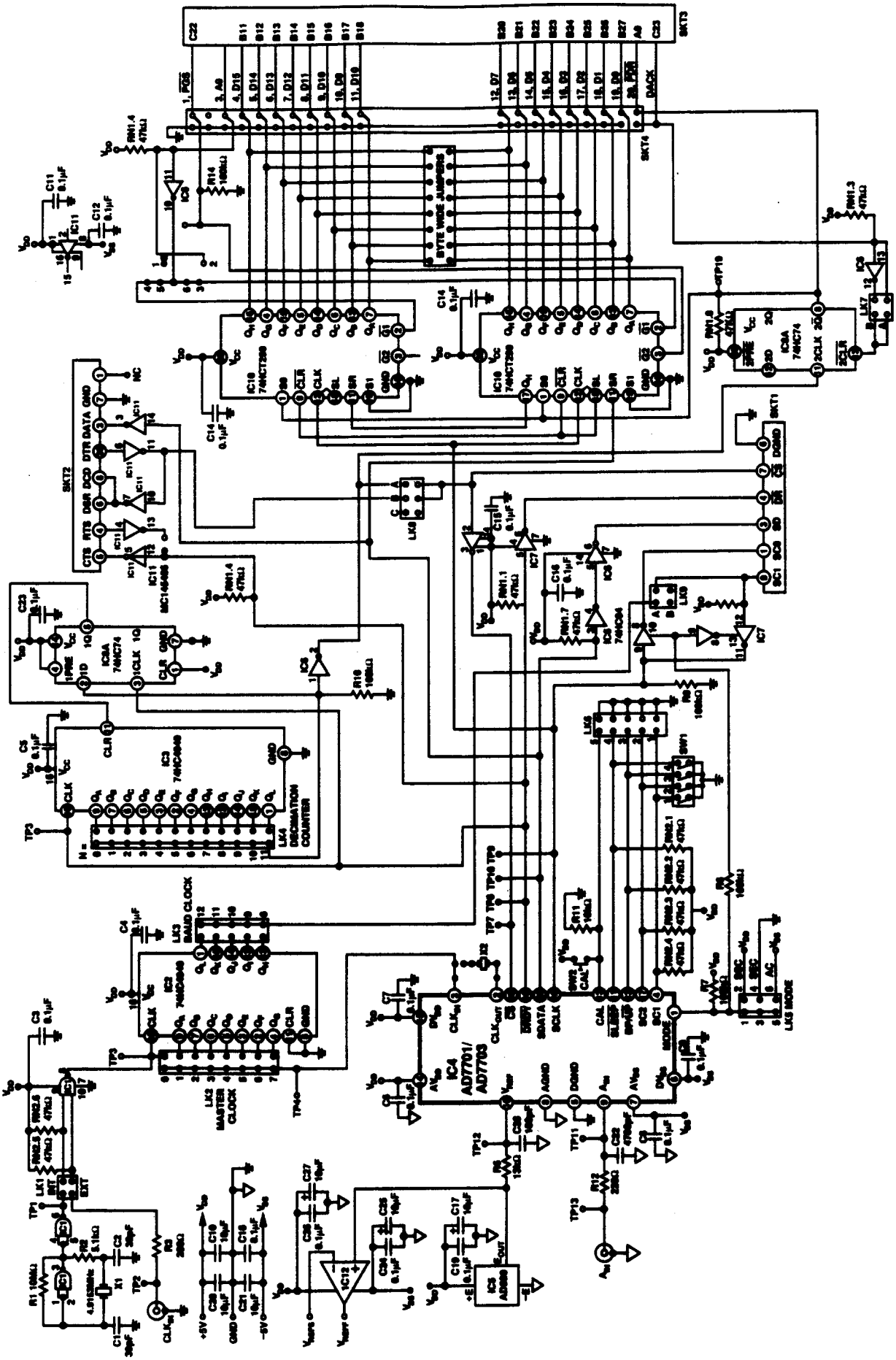

Figure 5. Evaluation Board Circuit Diagram

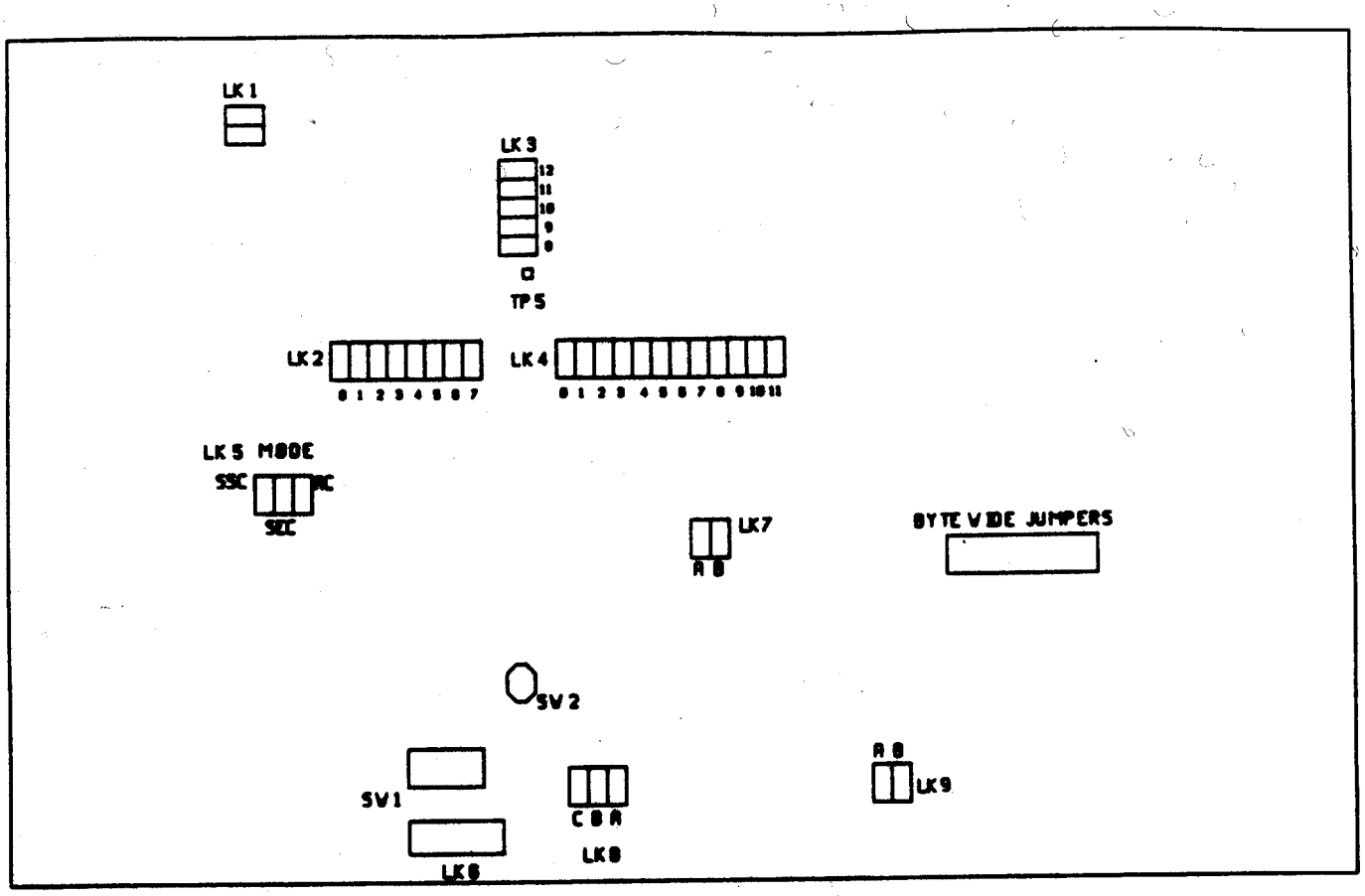

Figure 6. Positioning of Links and Switches on the Evaluation Board

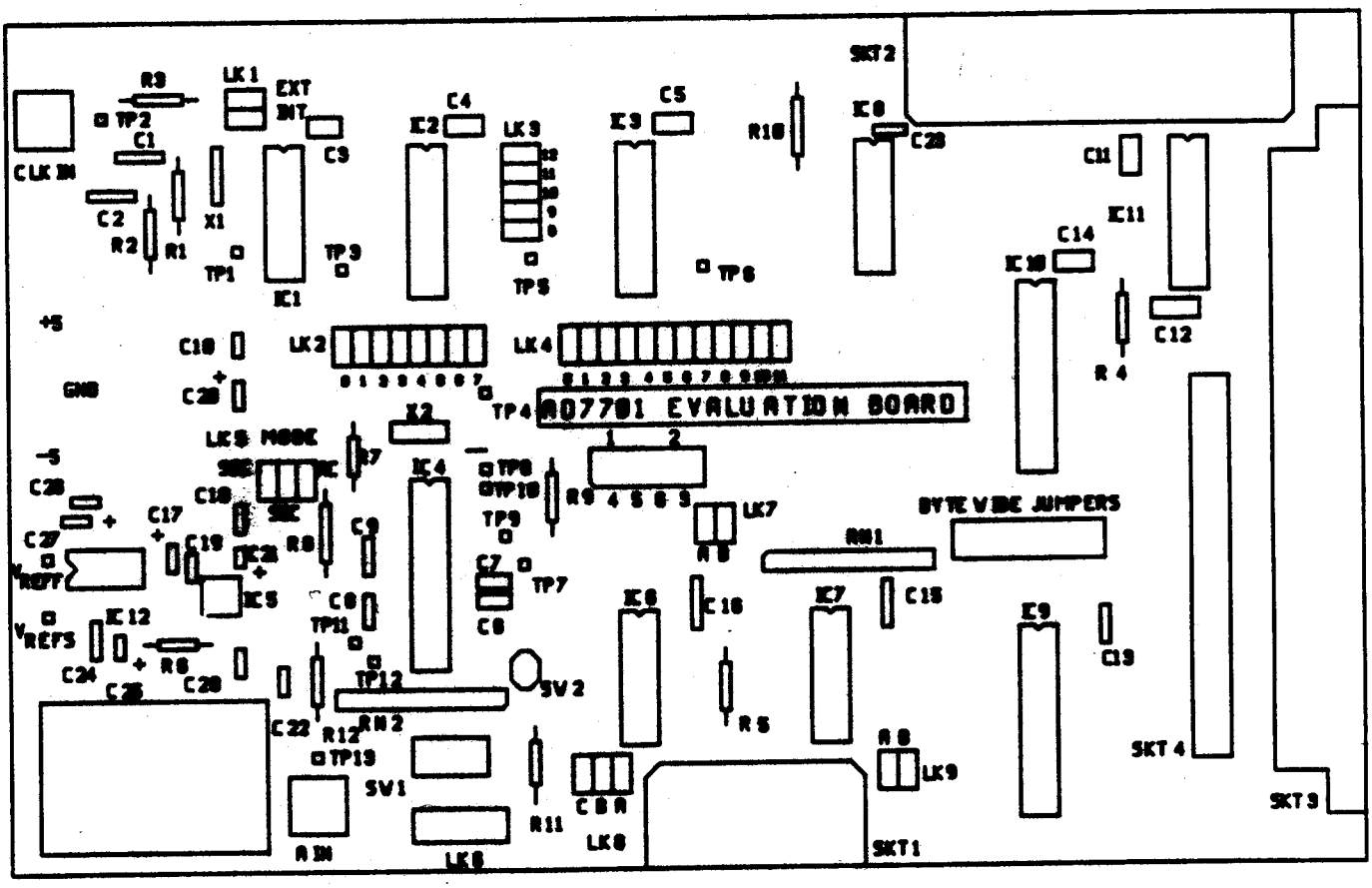

Figure 7. AD7701/AD7703 Evaluation Board Component Layout

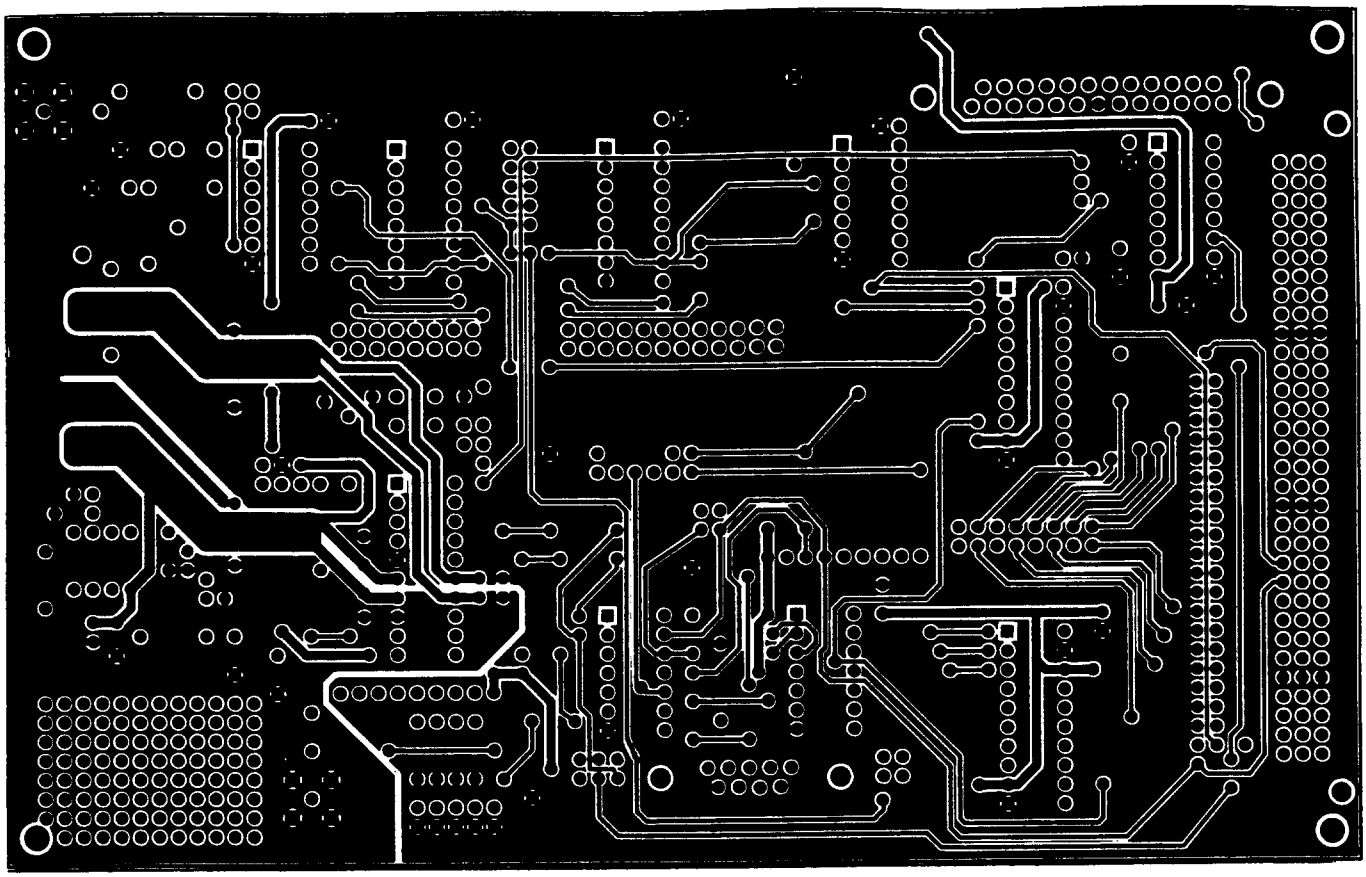

Figure 8. AD7701/AD7703 Evaluation Board Component Side Layout

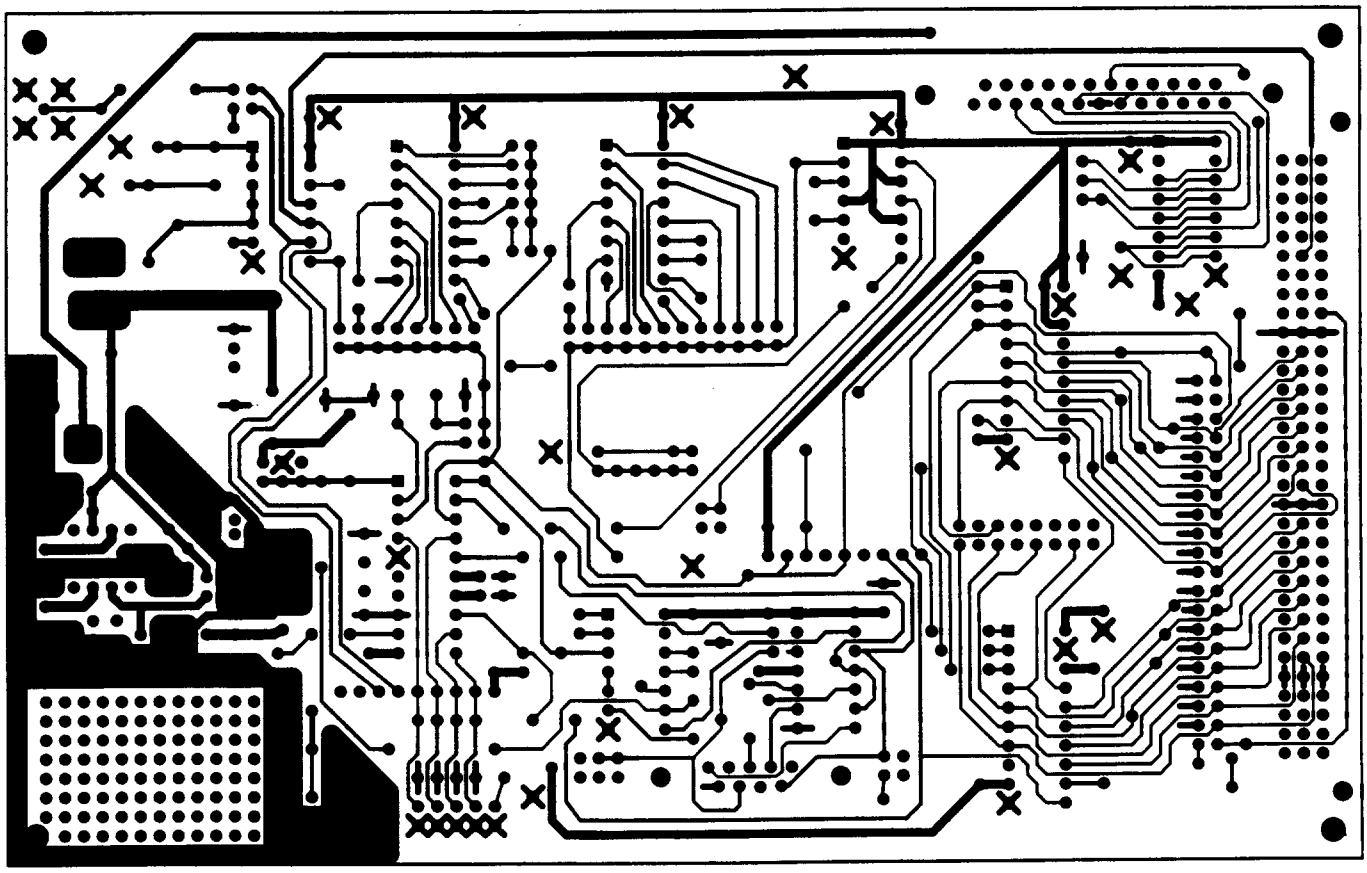

Figure 9. AD7701/AD7703 Evaluation Board Solder Side Layout