NOTES:

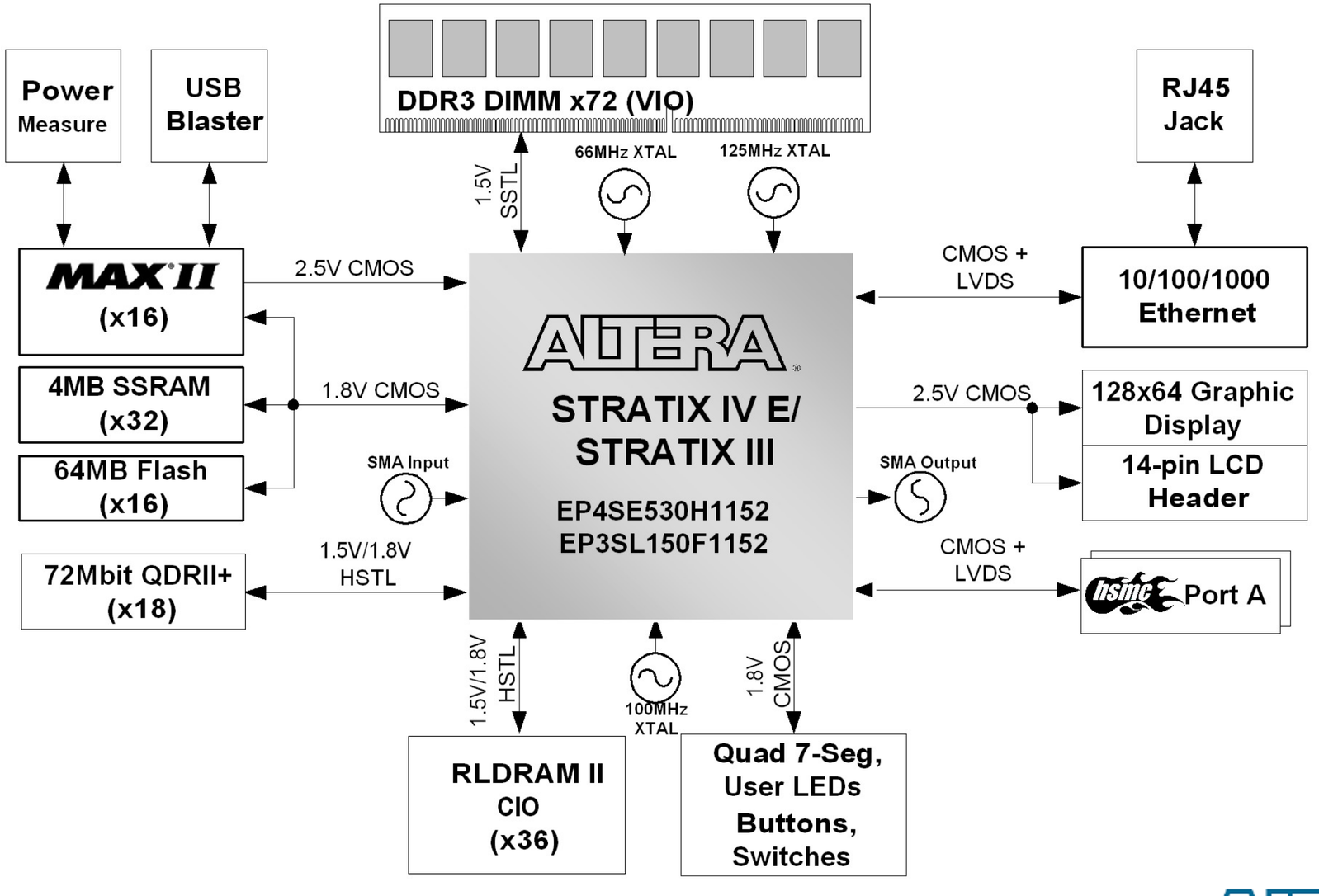
1. Project Drawing Numbers:

Raw PCB	100-0310904-C1
Gerber Files	110-0310904-C1
PCB Design Files	120-0310904-C1
Assembly Drawing	130-0310904-C1
Fab Drawing	140-0310904-C1
Schematic Drawing	150-0310904-C1
PCB Film	160-0310904-C1
Bill of Materials	170-0310904-C1
Schematic Design Files	180-0310904-C1
Functional Specification	210-0310904-C1
PCB Layout Guidelines	220-0310904-C1
Assembly Rework	320-0310904-C1

2. 1093 Parts, 80 Library Parts, 1068 Nets, 6228 Pins

REV	DATE	PAGES	DESCRIPTION
B	7/24/09	All	Released Rev B
C-1	5/26/2011	1,26	Change bias voltages V1,V2,V3,V4,V5 to positive voltages and remove -12V regulator circuit. LCD changed from F-51852 series to F-55472 series.

Stratix IV E FPGA Development Kit Board
Block Diagram



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	S4E FPGA Package Top
3	Power 1
4	Power 2
5	Power 3
6	Power 4
7	Power 5
8	Power & Temp Sense
9	Stratix IV E Power
10	Stratix IV E Clocks
11	Clock Circuitry
12	Stratix IV E Configuration
13	Embedded USB Blaster
14	Stratix IV E Banks 1 & 2
15	Stratix IV E Banks 3 & 4
16	Stratix IV E Banks 5 & 6
17	Stratix IV E Banks 7 & 8
18	DDR3 SDRAM DIMM
19	QDRII+ SRAM
20	RLDRAM II CIO
21	RLDRAM II CIO & QDRII TERMINATIONS
22	SSRAM & FLASH
23	MAX II
24	10/100/1000 Ethernet
25	User IO & Connector
26	Speaker, LCD connectors
27	HSM Connectors
28	Decoupling 1
29	Decoupling 2

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Stratix IV E FPGA Package Top

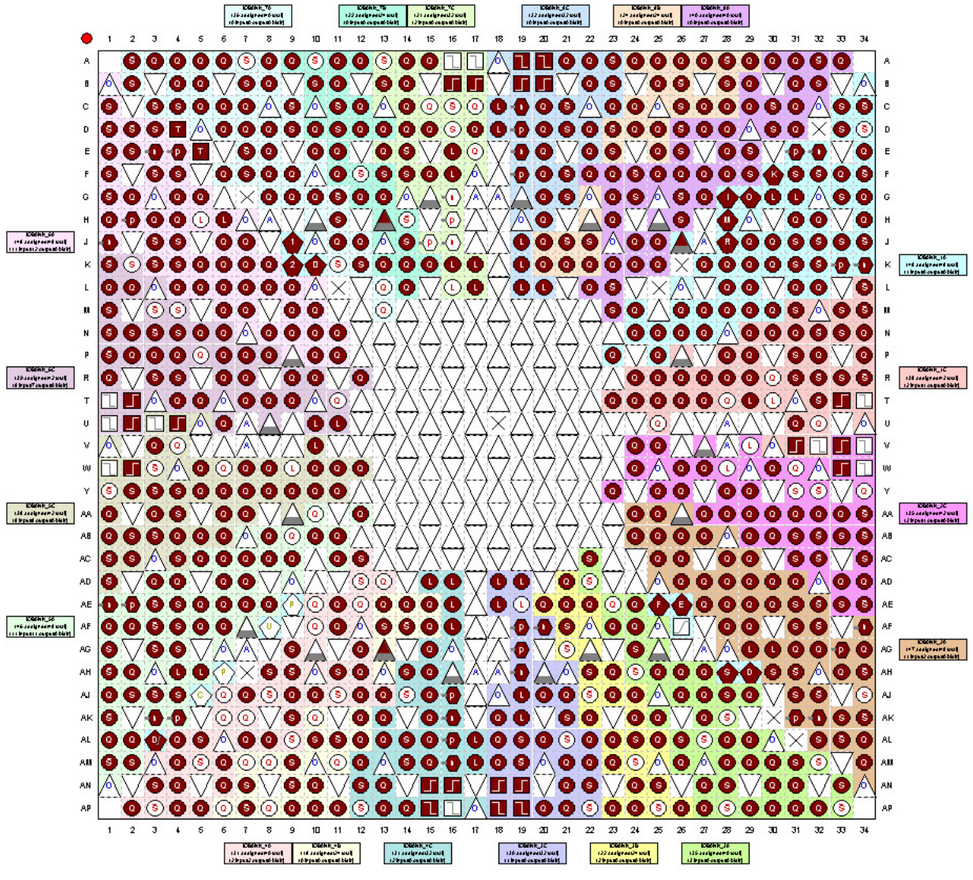
Notes:

1. FPGA Schematic Symbol Breakdown:
   - (A) Bank 1 - DISPLAY, USB, ETHERNET
   - (B) Bank 2 - RLDRAM II CIO
   - (C) Bank 3 - DDR3 SDRAM DIMM
   - (D) Bank 4 - DDR3 SDRAM DIMM, LCD, USER 7-SEGMENT DISPLAY
   - (E) Bank 5 - HSMC PORT A
   - (F) Bank 6 - HSMC PORT B
   - (G) Bank 7 - QDR II+ SRAM, USER PB
   - (H) Bank 8 - FLASH, SSRAM
   - (I) Some Clocks
   - (J) Configuration
   - (K) VCC, VCCD_PLL, VCCA_PLL, VCCPT, VCCAUX
   - (L) VCCIO, VREF
   - (M) Ground and NCs
   - (N) Ground

BANKS 7A, 7B, 7C
VCCIO = 1.5V/1.8V
QDR II+ SRAM
USER PB

BANKS 8A, 8B, 8C
VCCIO = 2.5V
FLASH
SSRAM
MAX II
USER DIPSWITCH, PUSH BUTTONS

BANKS 6A, 6C
VCCIO = 2.5V
HSMC PORT B



BANKS 1A 1C
VCCIO = 2.5V
GRAPHIC DISPLAY
ETHERNET

BANKS 5A, 5C
VCCIO = 2.5V
HSMC PORT A

BANKS 2A, 2C
VCCIO = 1.5V/1.8V
RLDRAM II CIO

BANK 4B
VCCIO = 2.5V
LCD DISPLAY
USER 7-SEGMENT DISPLAY

BANKS 4A, 4C
VCCIO = 1.5V
DDR3 SDRAM DIMM

BANKS 3A, 3B, 3C
VCCIO = 1.5V
DDR3 SDRAM DIMM

Pin Legend

Symbol	Pin Type
	User I/O
	User Assigned I/O
	Fitter Assigned I/O
	User and Fitter Assigned I/O
	Unbonded Pad
	Reserved Pin
C	Other Configuration
E	DEV_OE
R	DEV_CLR
I	DIFF_n
P	DIFF_p
Q	DQ
S	DQS
L	Other PLL
D	Other Dual Purpose
	CLK_n
	CLK_p
0	MSEL0
1	MSEL1
2	MSEL2
3	MSEL3
D	CONF_DONE
E	nCE
F	nCONFIG
T	TDI
K	TCK
M	TMS
O	TDO
S	nSTATUS
	VREF
	VCCP/VCCR/VCCT
A	VCCA
I	VCCINT
O	VCCIO
	GND
A	GNDA_PLL

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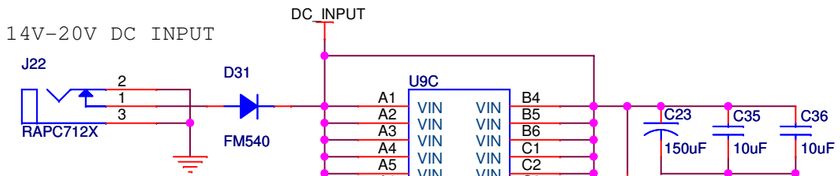
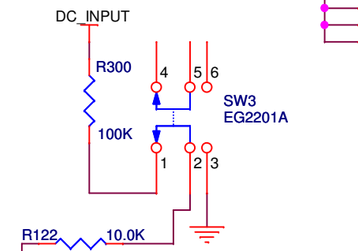
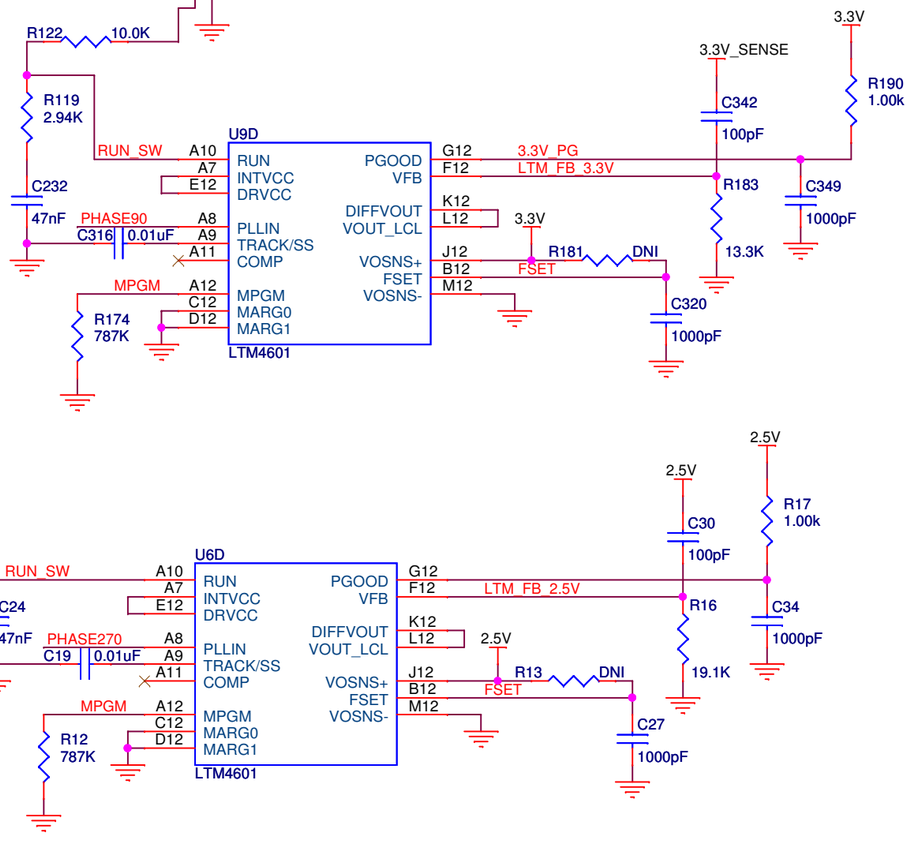
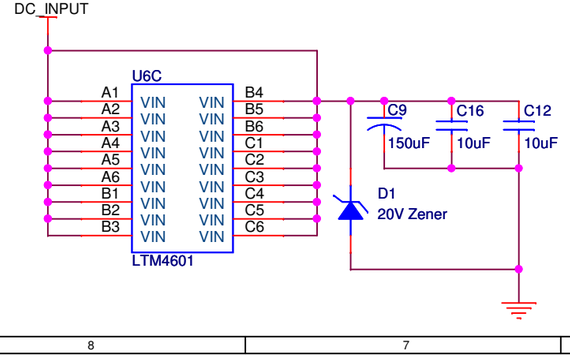
Power 1, (3.3V and 2.5V)

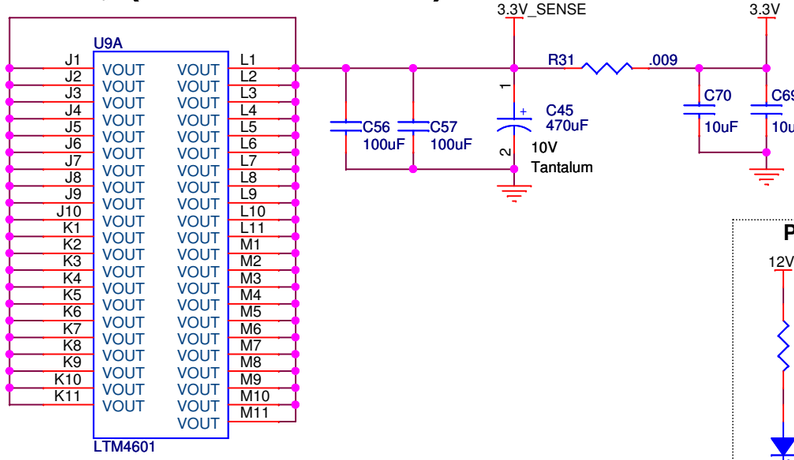
14V-20V DC INPUT

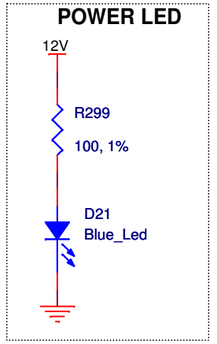


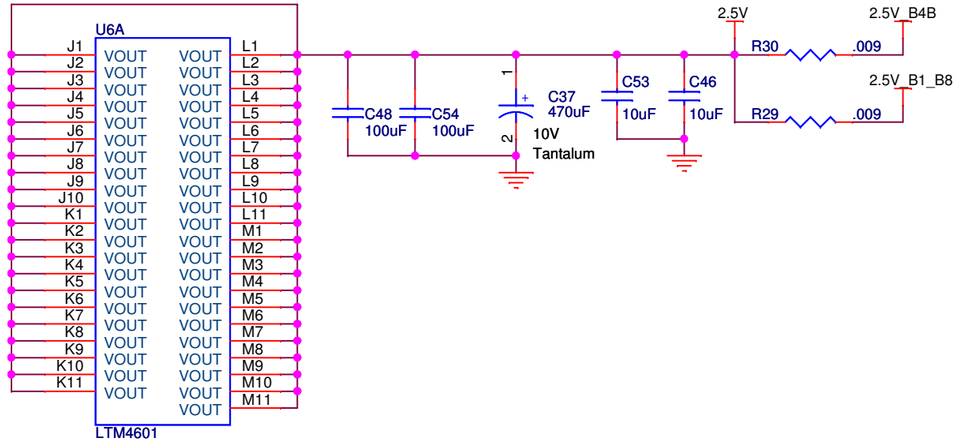




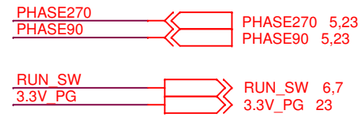


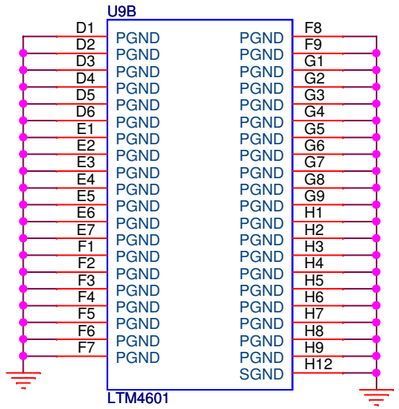


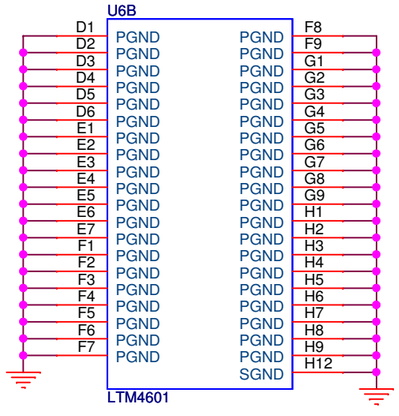




LT4601 SWITCHER







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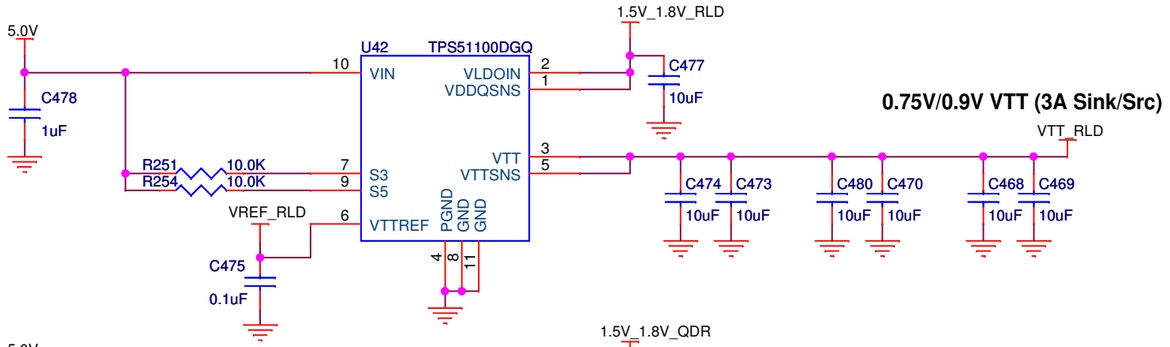
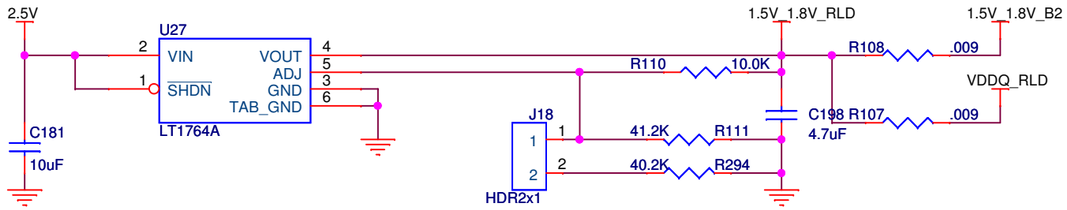
Power 2, (5.0V, RLDRAM II, QDRII+, 2.5V_FPGA)

2.5V_FPGA_PG
VDDQ_QDRII_PG
2.5V_HSMC_PG

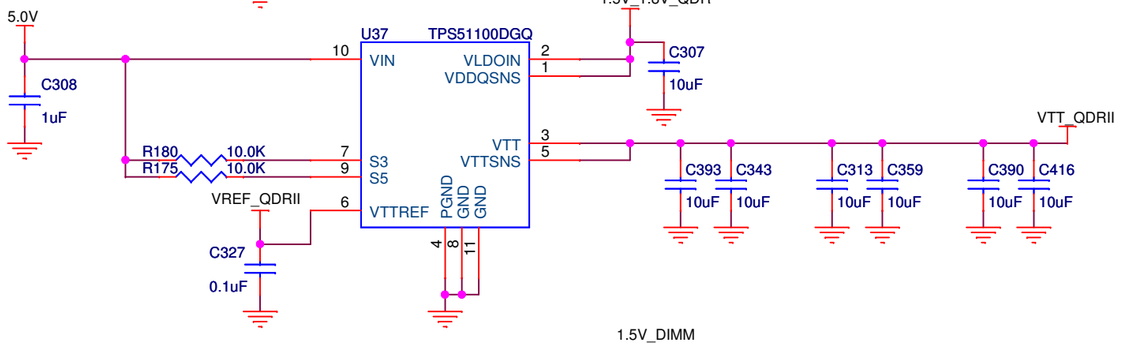
2.5V_FPGA_PG 23
VDDQ_QDRII_PG 23
2.5V_HSMC_PG 23

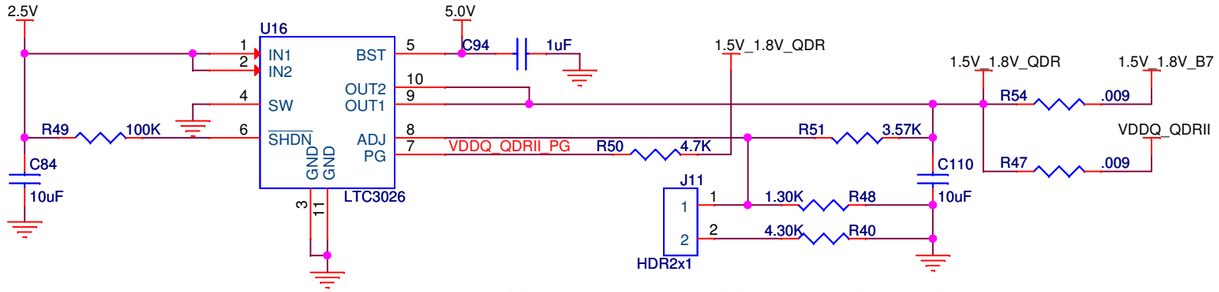


0.75V/0.9V VTT (3A Sink/Src)

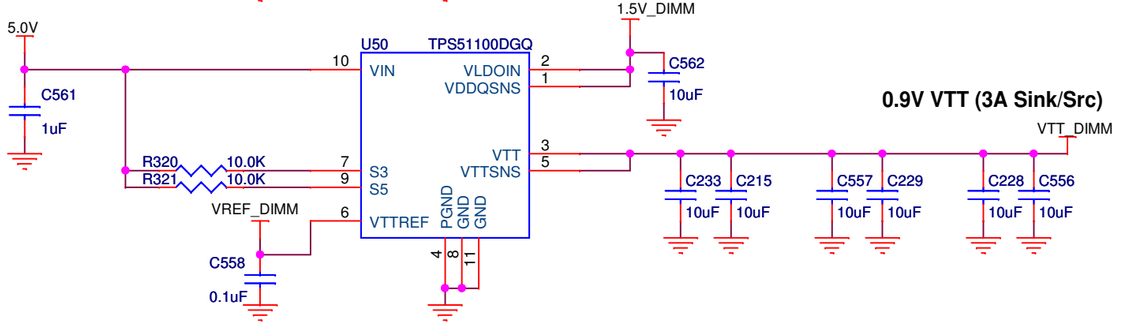


41.2K // 40.2K = 20.3K needed for 1.8V operation
41.2K needed for 1.5V operation (Default)

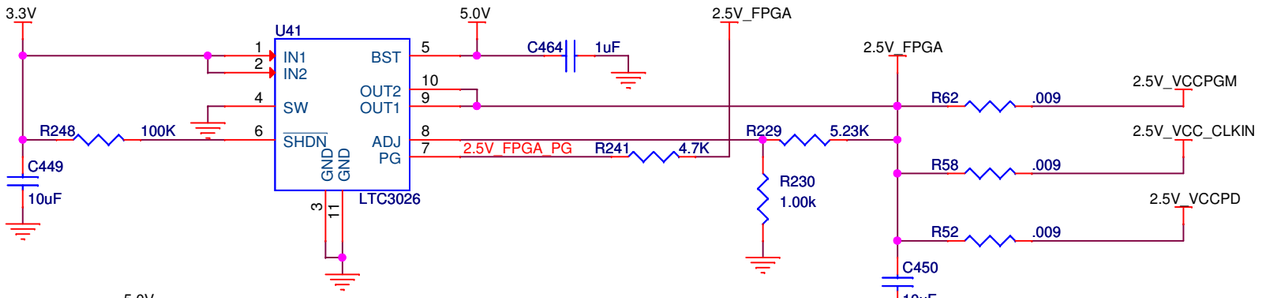


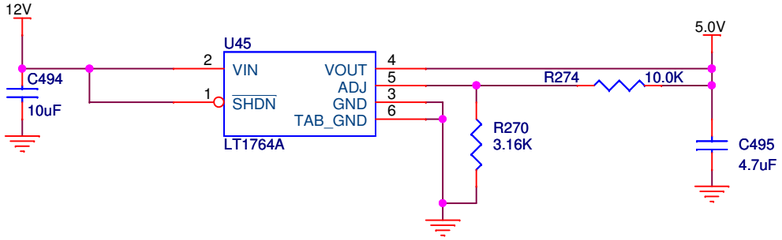


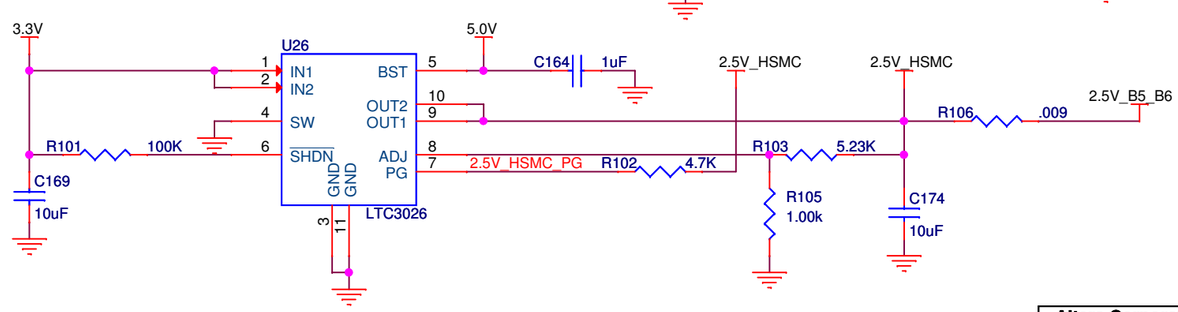
1.30K // 4.3K = 1.00Kneeded for 1.8V operation
1.30K needed for 1.5V operation (Default)



0.9V VTT (3A Sink/Src)







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Power 3, (VCC)

PHASE0 — PHASE0 23
PHASE90 — PHASE90 3,23
PHASE180 — PHASE180 23
PHASE270 — PHASE270 3,23

12V
U32C
LTM4601
C271 150uF
C274 10uF
C275 10uF
C265 0.1uF
D32 20V Zener

12V
U31C
LTM4601
C266 0.1uF

VCC_OUT
U32A
LTM4601
C257 0.1uF
C254 100uF
C255 100uF
C263 470uF 10V Tantalum
C258 470uF 10V Tantalum

VCC
R126 0
VCCL
R123 0.003

U31A
LTM4601

VCC_OUT
C246 0.1uF
C259 100uF
C250 100uF
C262 470uF 10V Tantalum

U32B
LTM4601

U31B
LTM4601

INT_VCC_C
10.0K R312
DNI R314 PHASE_PH
DNI R307 PHASE_DIV
0 R308
20.0K R309
C550 0.1uF
C555 DNI
U49
LTC6902
PHASE0
PHASE90
PHASE180
PHASE270
PHASE_MOD
DNI R311 0
R313
INT_VCC_C

Default Settings:
PH:tied high for 4 phases
DIV: tied to GND for /1

3.3V
10K R335
C570 1000pF
RUN_SW2
INT_VCC_D
PHASE180
TRACK_C
COMP_C
U31D
LTM4601
LTMC_VFB
VOUT_LCL
DC_INPUT
C564 100pF
J12
DNI R326
INT_VCC_D
C572 DNI
C566 DNI

VCC_OUT
C264 220PF
XJ1 881545-2
RUN_SW2
INT_VCC_C
C571 47nF
PHASE0
TRACK_C
C574 0.01uF
COMP_C
C573 DNI
U32D
LTM4601
LTMC_VFB
VOUT_LCL
60.4K R128
R129 36.0K
J21 TSW-103-08-G-S
12V
VCCL
DNI R336
C567 DNI
C559 1000pF
(1-2) 0.9V operation
(2-3) 1.1V operation

1.8V
U48
LTC3026
C554 10uF
R305 100K
5.0V
C551 1uF
VCC
1.1V for Stratix III low power
R310 DNI
5.11K R304
R303 4.7K
2.87K R302
C544 10uF
C547 470uF 10V Tantalum

For Stratix IV option: (Default)
1) DNI R310 (Disables U48) and populate R126.
2) Place jumper on pins 1 and 2 of J21 (Selects 0.9V for VCCL and VCC)
For Stratix III 1.1V option:
1) DNI R310 (Disables U48) and populate R126 (Ties VCCL and VCC to same regulator).
2) Place jumper on pins 2 and 3 of J21 (Selects 1.1V for VCCL and VCC).
For Stratix III Low power option:
1) DNI R126 and populate R310 (Enables U48) and provides 1.1V to VCC
2) Place jumper on pins 1 and 2 of J21 (Selects 0.9V for VCCL)

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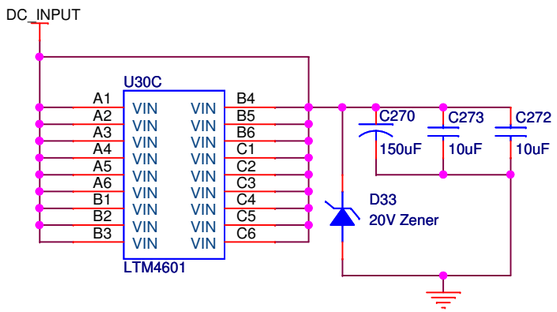
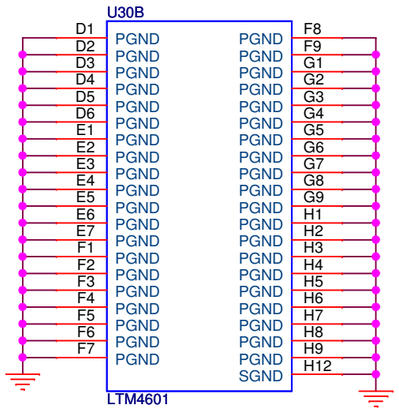
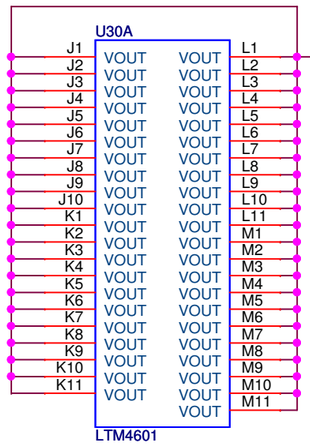
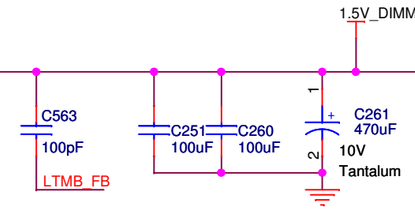
Power 4, (1.5V_DIMM, 1.1V, VCCD_PLL, VCCPT, VCCAUX and 2.5V_A)









LT4601 SWITCHER

MAX_PHASE_CLK0 — MAX_PHASE_CLK0 23

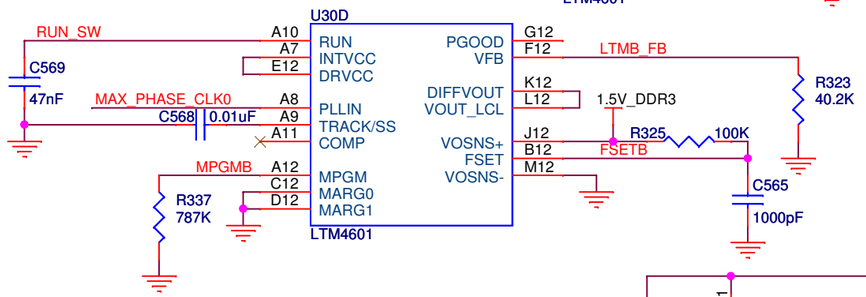
RUN_SW — RUN_SW 3,7

Regulator Sense Signals

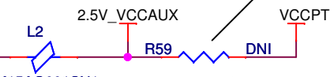
2.5V_A_SENSE_P — 2.5V_A_SENSE_P 8

2.5V_A_SENSE_N — 2.5V_A_SENSE_N 8

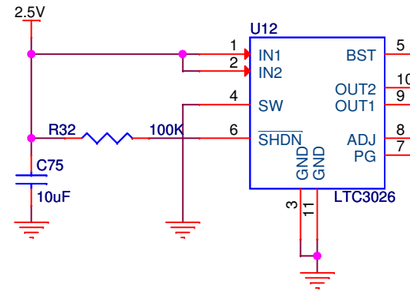
VCCD_SENSE_P — VCCD_SENSE_P 8



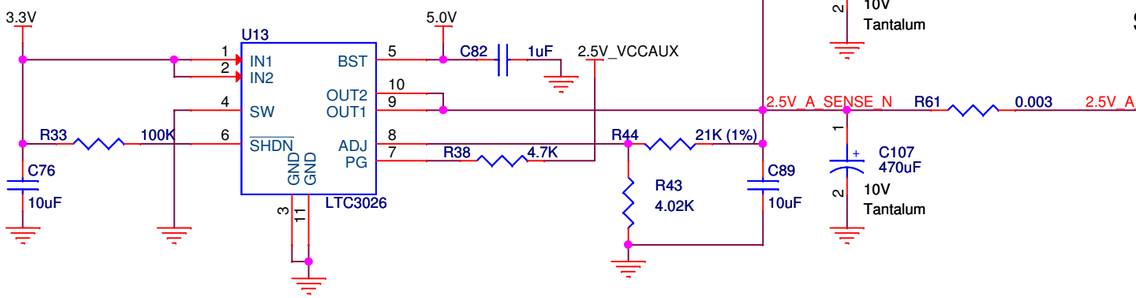
DO NOT INSTALL BOTH R59 AND R53 AT THE SAME TIME!

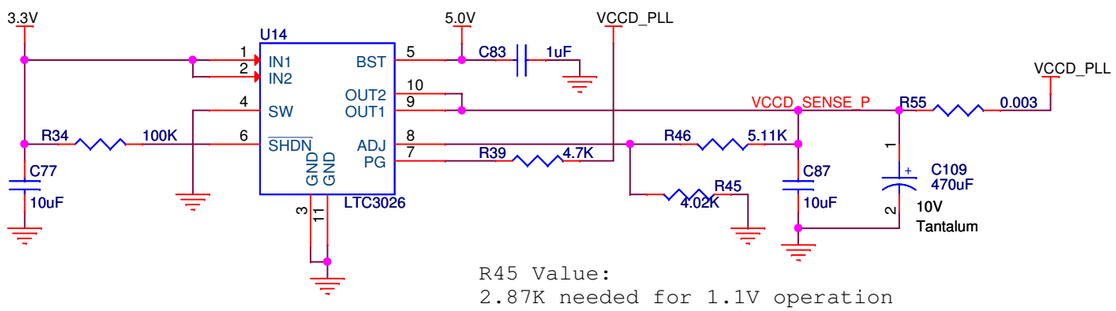


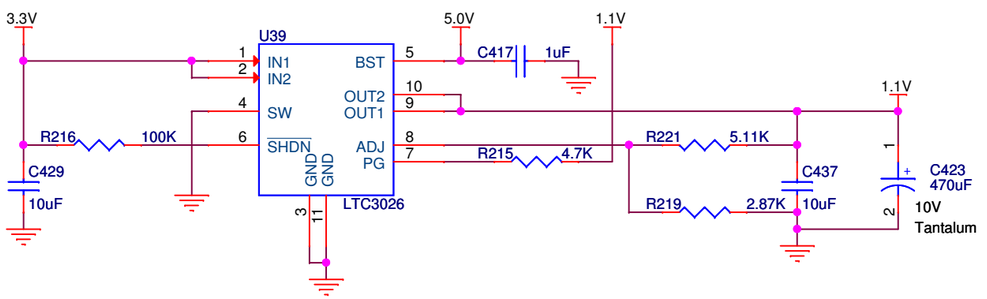
DNI THIS RESISTOR FOR STRATIX IV



DNI THIS RESISTOR FOR STRATIX III







R45 Value:
2.87K needed for 1.1V operation
4.02K needed for 0.9V operation

For Stratix III use 2.87K

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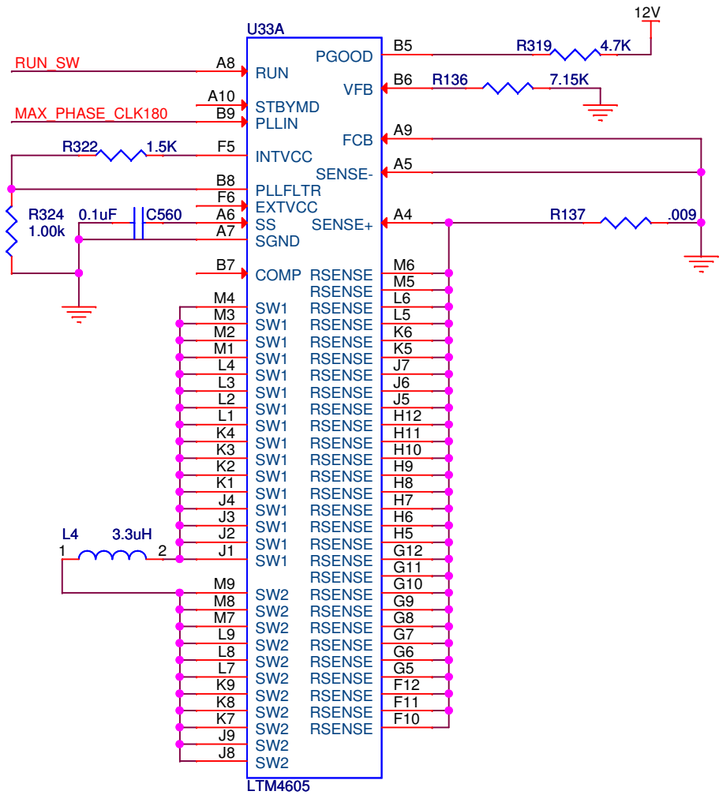
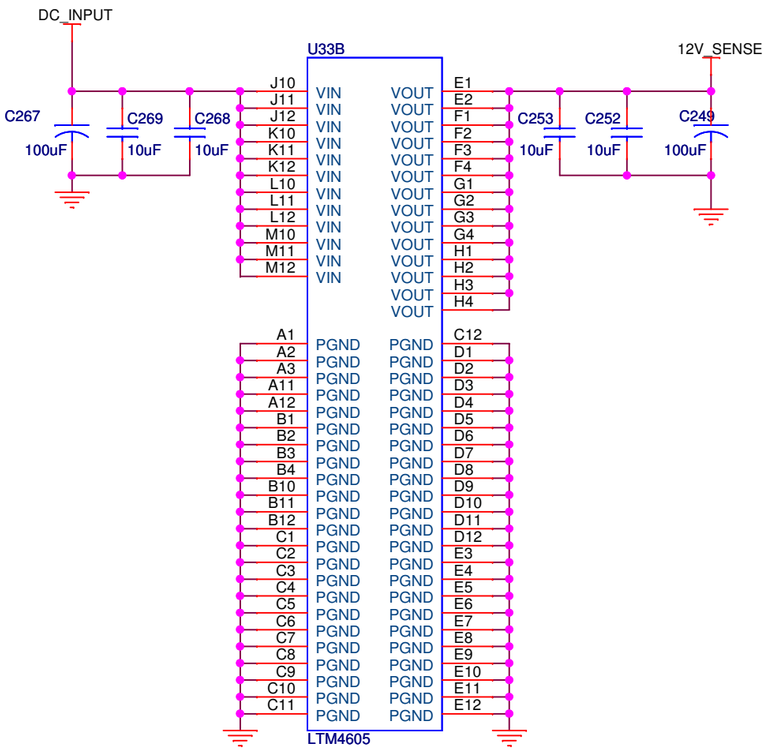
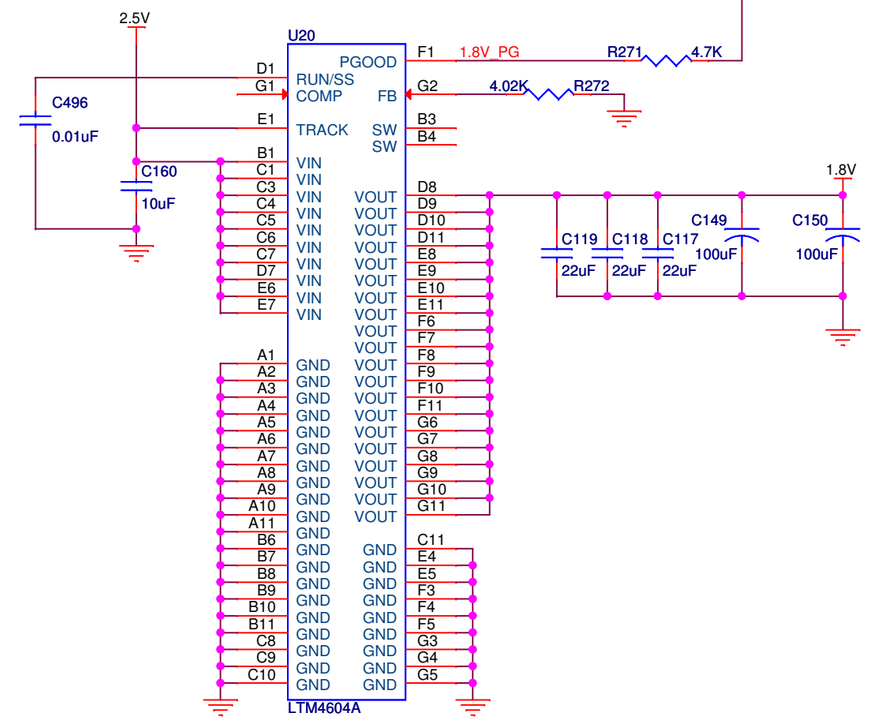
Power 5, (12V and 1.8V)

MAX_PHASE_CLK180
RUN_SW
1.8V_PG

MAX_PHASE_CLK180 23
RUN_SW 3,6
1.8V_PG 23







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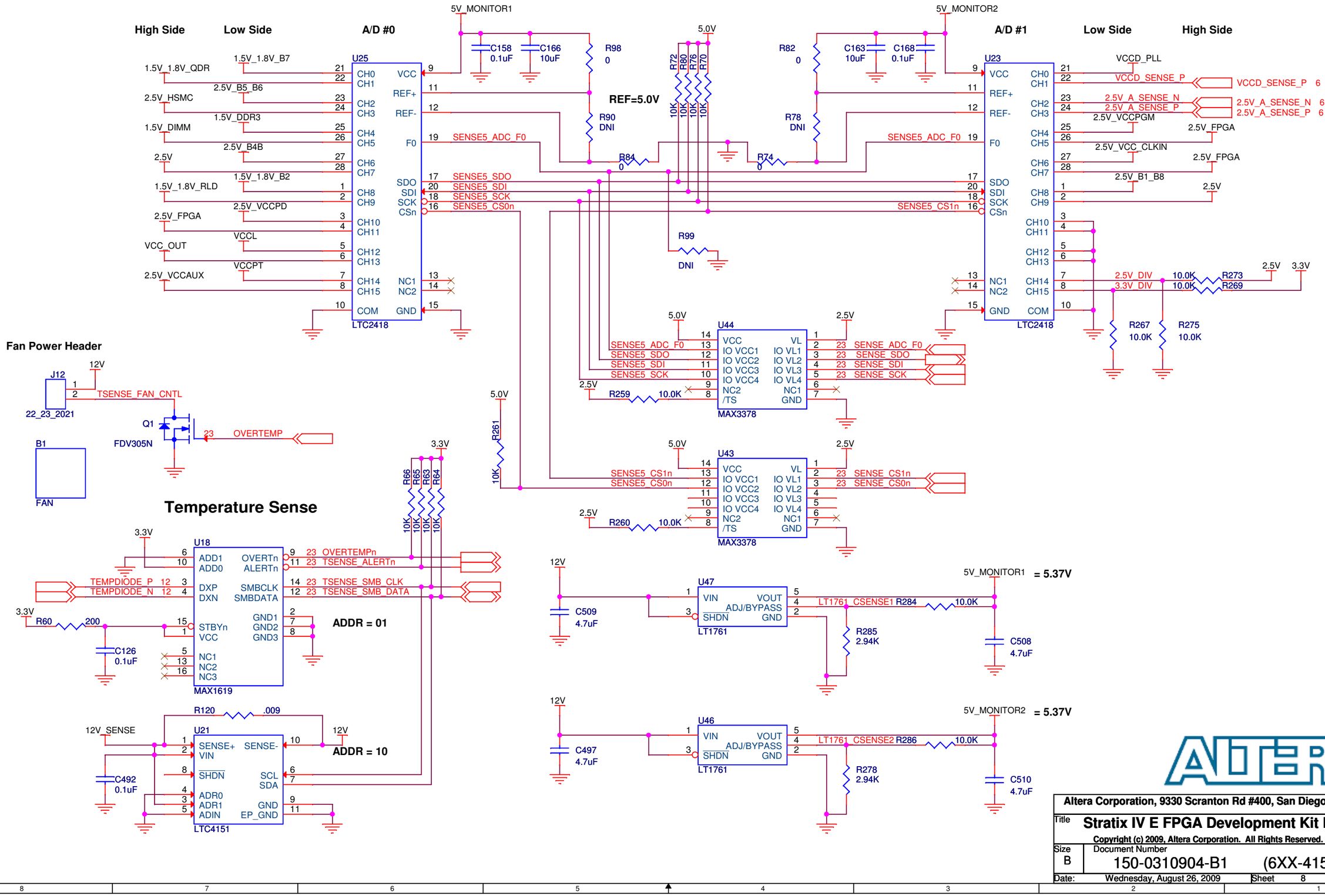
Power & Temp Monitor



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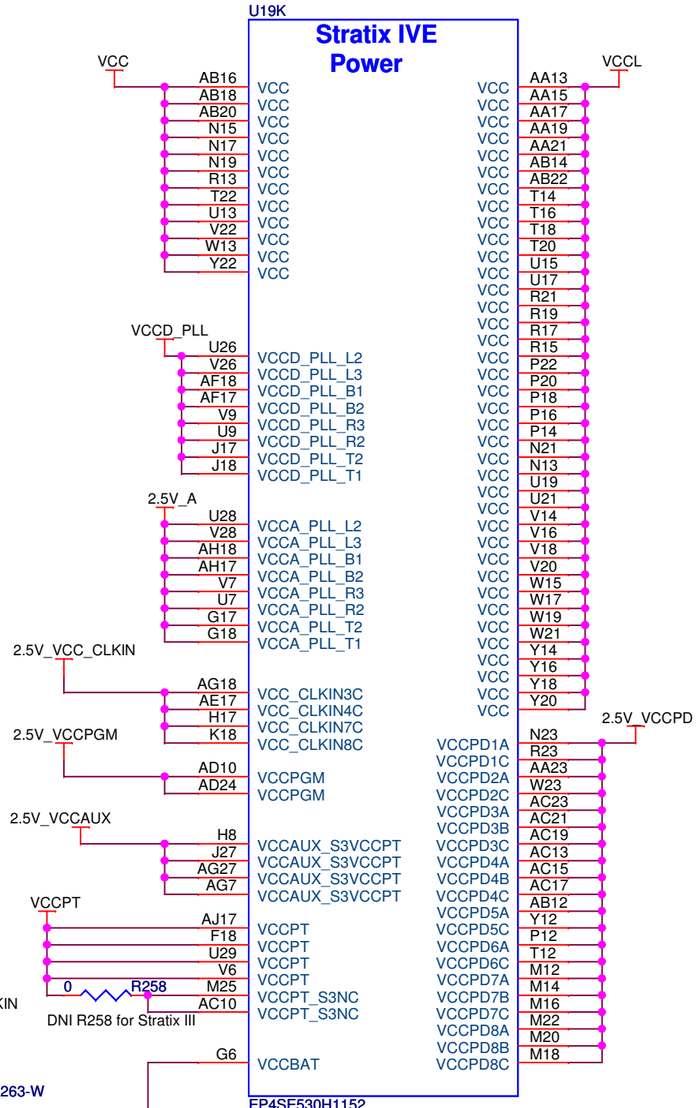
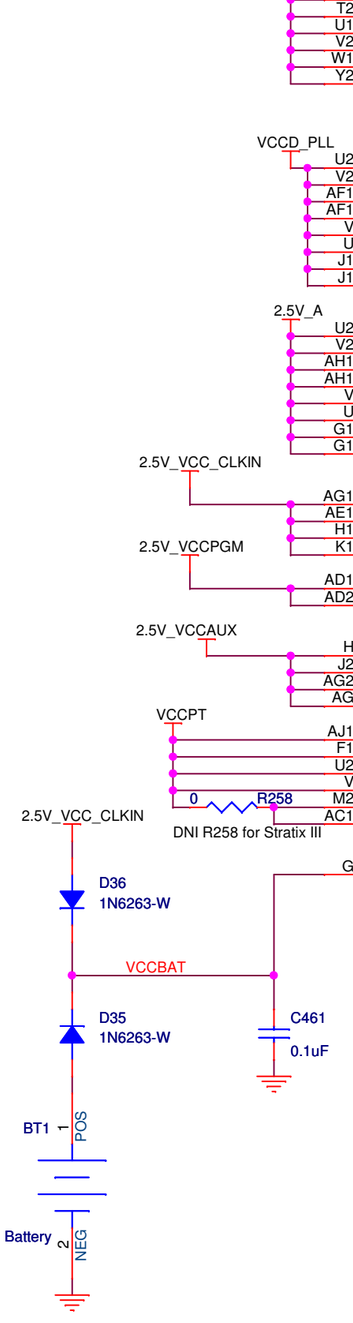
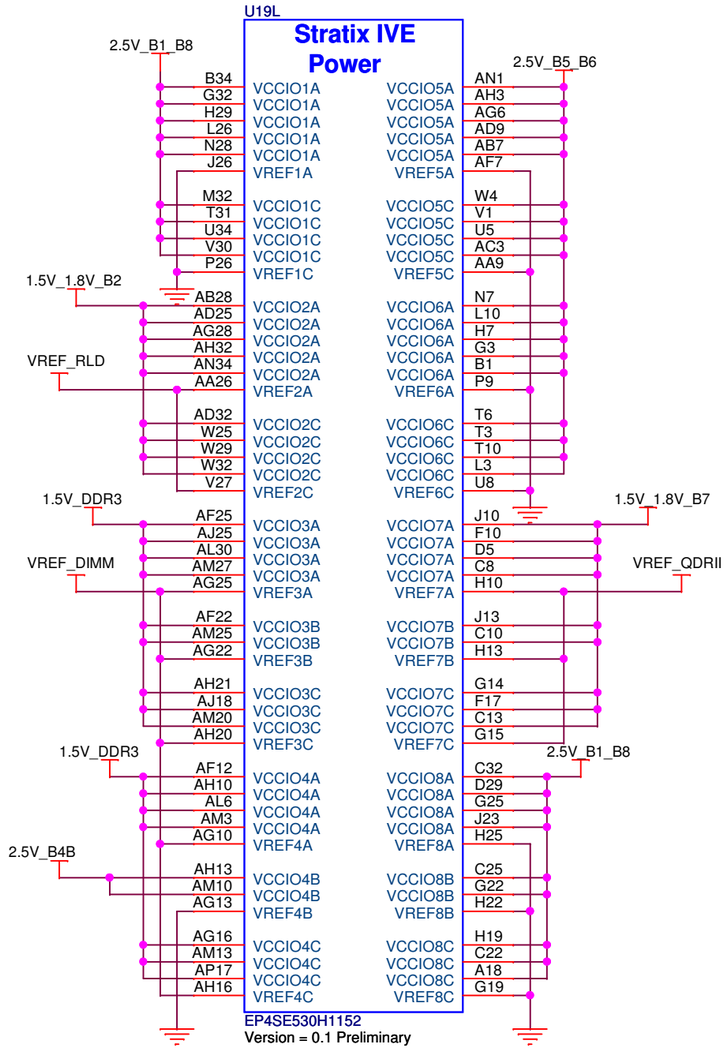
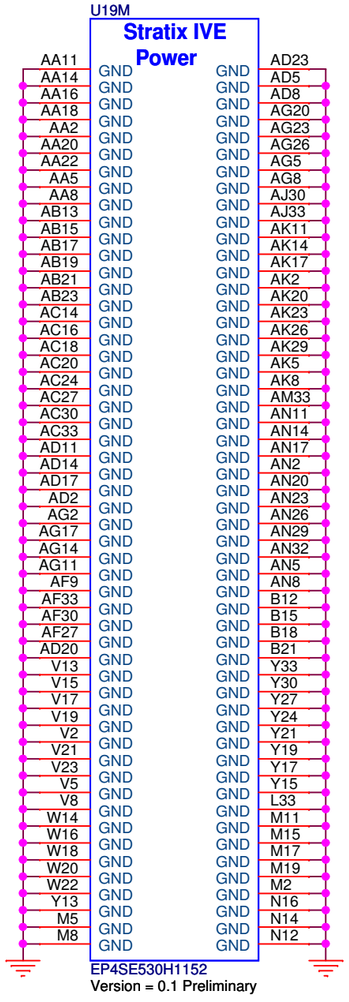
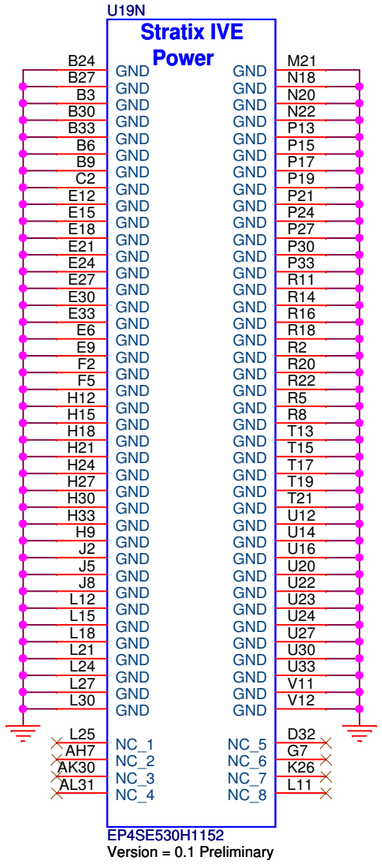
Stratix IV E Power

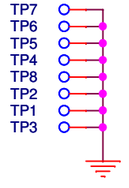




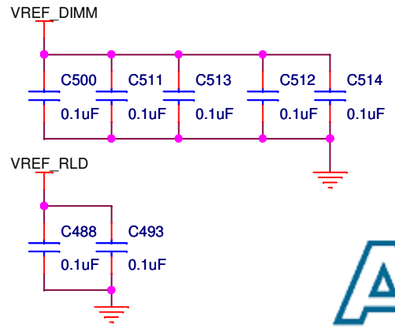


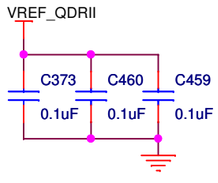






PLACE NEAR FPGA





Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix IV E FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0310904-B1 (6XX-41504R)	B

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Stratix IV E Clocks

CLKIN_100M_P	100, 1% R235	CLKIN_100M_N	
CLKIN_125M_P0	100, 1% R262	CLKIN_125M_N0	
CLKIN_125M_P1	100, 1% R236	CLKIN_125M_N1	
CLKIN_66M_P0	100, 1% R265	CLKIN_66M_N0	
CLKIN_66M_P1	100, 1% R288	CLKIN_66M_N1	
HSMA_CLK_IN_P1	100, 1% R266	HSMA_CLK_IN_N1	
HSMB_CLK_IN_P1	100, 1% R263	HSMB_CLK_IN_N1	

U19I

Stratix IVE Clocks

Bank 1A

		PLL_L1_FB_CLKOUT0P/DIFFIO_TX_L1P	G30 HSMA_TX_LED
		PLL_L1_CLKOUT0N/DIFFIO_TX_L1N	G31 ENET_TX_D7

Bank 1C

ENET_S_CLKP	V31	CLK0P/DIFFIO_RX_L28P	
ENET_S_CLKN	V32	CLK0N/DIFFIO_RX_L28N	
CLKIN_125M_P0	T33	CLK1P	PLL_L2_FB_CLKOUT0P/DIFFIO_TX_L28P T29 ENET_TX_P
CLKIN_125M_N0	T34	CLK1N	PLL_L2_CLKOUT0N/DIFFIO_TX_L28N T30 ENET_TX_N

Bank 2A

		PLL_L4_FB_CLKOUT0P/DIFFIO_TX_L56P	AG29 RLDC_A19
		PLL_L4_CLKOUT0N/DIFFIO_TX_L56N	AG30 RLDC_A11

Bank 2C

CLKIN_66M_P0	W33	CLK2P/DIFFIO_RX_L29P	
CLKIN_66M_N0	W34	CLK2N/DIFFIO_RX_L29N	
CLKIN_50	V33	CLK3P	PLL_L3_FB_CLKOUT0P/DIFFIO_TX_L29P W28
	V34	CLK3N	PLL_L3_CLKOUT0N/DIFFIO_TX_L29N V29

Bank 3C

DDR3_DIMM_A4	AN18		PLL_B1_CLKOUT0P AD18 DDR3_DIMM_CKE1
DDR3_DIMM_A5	AP18	CLK4P/DIFFIO_RX_B32P	PLL_B1_CLKOUT0N AE18 DDR3_DIMM_A14
DDR3_DIMM_SDA	AN19	CLK4N/DIFFIO_RX_B32N	PLL_B1_CLKOUT3 AD19 DDR3_DIMM_A15
DDR3_DIMM_A8	AP19	CLK5P/DIFFOUT_B63P	PLL_B1_CLKOUT4 AE19
		CLK5N/DIFFOUT_B63N	PLL_B1_FBP/CLKOUT1/DIFFIO_RX_B31P AJ19 DDR3_DIMM_RESETn
			PLL_B1_FBN/CLKOUT2/DIFFIO_RX_B31N AK19 DDR3_DIMM_A12

Bank 4C

CLKIN_66M_P1	AN16	CLK6P/DIFFIO_RX_B33P	PLL_B2_CLKOUT0P AE16 DDR3_DIMM_CSn1
CLKIN_66M_N1	AP16	CLK6N/DIFFIO_RX_B33N	PLL_B2_CLKOUT0N AF16 DDR3_DIMM_A13
CLKIN_SMA	AN15	CLK7P/DIFFOUT_B66P	PLL_B2_CLKOUT3 AD15 DDR3_DIMM_CSn2
DDR3_DIMM_A10	AP15	CLK7N/DIFFOUT_B66N	PLL_B2_CLKOUT4 AD16 DDR3_DIMM_CSn3
			PLL_B2_FBP/CLKOUT1/DIFFIO_RX_B34P AL17 DDR3_DIMM_A0
			PLL_B2_FBN/CLKOUT2/DIFFIO_RX_B34N AM17 DDR3_DIMM_A1

Bank 5A

		PLL_R4_FB_CLKOUT0P/DIFFIO_TX_R1P	AH5 HSMA_TX_D_P2
		PLL_R4_CLKOUT0N/DIFFIO_TX_R1N	AH4 HSMA_TX_D_N2

Bank 5C

HSMA_CLK_IN_P1	W2	CLK8P	
HSMA_CLK_IN_N1	W1	CLK8N	
HSMA_CLK_IN_P2	U4	CLK9P/DIFFIO_RX_R28P	PLL_R3_FB_CLKOUT0P/DIFFIO_TX_R28P V10 HSMA_CLK_OUT_P1
HSMA_CLK_IN_N2	U3	CLK9N/DIFFIO_RX_R28N	PLL_R3_CLKOUT0N/DIFFIO_TX_R28N W9 HSMA_CLK_OUT_N1

Bank 6A

		PLL_R1_FB_CLKOUT0P/DIFFIO_TX_R56P	H6 HSMB_CLK_OUT_P2
		PLL_R1_CLKOUT0N/DIFFIO_TX_R56N	H5 HSMB_CLK_OUT_N2

Bank 6C

HSMB_CLK_IN_P1	U2	CLK10P	
HSMB_CLK_IN_N1	U1	CLK10N	PLL_R2_FB_CLKOUT0P/DIFFIO_TX_R29P U11 CLKOUT_SMA
HSMB_CLK_IN_P2	T2	CLK11P/DIFFIO_RX_R29P	PLL_R2_CLKOUT0N/DIFFIO_TX_R29N U10 HSMB_SDA
HSMB_CLK_IN_N2	T1	CLK11N/DIFFIO_RX_R29N	

Bank 7C

CLKIN_100M_P	B17		PLL_T2_CLKOUT0P L17 USER_PB0
CLKIN_100M_N	A17	CLK12P/DIFFIO_RX_T32P	PLL_T2_CLKOUT0N K17 USER_PB3
CLKIN_125M_P1	B16	CLK12N/DIFFIO_RX_T32N	PLL_T2_CLKOUT3 K16 QDRII_RPSn
CLKIN_125M_N1	A16	CLK13P/DIFFOUT_T63P	PLL_T2_CLKOUT4 L16
		CLK13N/DIFFOUT_T63N	PLL_T2_FBP/CLKOUT1/DIFFIO_RX_T31P F16 USER_PB1
			PLL_T2_FBN/CLKOUT2/DIFFIO_RX_T31N E16 USER_PB2

Bank 8C

HSMB_CLK_IN0	B19	CLK14P/DIFFIO_RX_T33P	PLL_T1_CLKOUT0P K19 USER_DIPSW4
USER_DIPSW1	A19	CLK14N/DIFFIO_RX_T33N	PLL_T1_CLKOUT0N J19 USER_DIPSW5
HSMA_CLK_IN0	B20	CLK15P/DIFFOUT_T66P	PLL_T1_CLKOUT3 L19 USER_DIPSW6
USER_DIPSW3	A20	CLK15N/DIFFOUT_T66N	PLL_T1_CLKOUT4 L20 USER_DIPSW7
			PLL_T1_FBP/CLKOUT1/DIFFIO_RX_T34P D18 FSM_A25
			PLL_T1_FBN/CLKOUT2/DIFFIO_RX_T34N C18 USER_DIPSW2

EP4SE530H1152
Version = 0.1 Preliminary

SMA Connector
(external clock source)

J17 — 1 CLKIN_SMA — R109 49.9 — J16 1 CLKOUT_SMA

CLOCK INTERFACE

CLKIN_66M_P0	CLKIN_66M_P0 11
CLKIN_66M_N0	CLKIN_66M_N0 11
CLKIN_66M_P1	CLKIN_66M_P1 11
CLKIN_66M_N1	CLKIN_66M_N1 11
CLKIN_125M_P0	CLKIN_125M_P0 11
CLKIN_125M_N0	CLKIN_125M_N0 11
CLKIN_125M_P1	CLKIN_125M_P1 11
CLKIN_125M_N1	CLKIN_125M_N1 11
CLKIN_100M_P	CLKIN_100M_P 11
CLKIN_100M_N	CLKIN_100M_N 11
CLKIN_50	CLKIN_50 11,23

HSMC PORT A

HSMA_TX_D_P[16:0]	HSMA_TX_D_P[16:0] 16,27
HSMA_TX_D_N[16:0]	HSMA_TX_D_N[16:0] 16,27
HSMA_CLK_IN_P[2:1]	HSMA_CLK_IN_P[2:1] 27
HSMA_CLK_IN_N[2:1]	HSMA_CLK_IN_N[2:1] 27
HSMA_CLK_OUT_P[2:1]	HSMA_CLK_OUT_P[2:1] 16,27
HSMA_CLK_OUT_N[2:1]	HSMA_CLK_OUT_N[2:1] 16,27
HSMA_TX_LED	HSMA_TX_LED 25
HSMA_CLK_IN0	HSMA_CLK_IN0 27

HSMC PORT B

HSMB_CLK_IN_P[2:1]	HSMB_CLK_IN_P[2:1] 27
HSMB_CLK_IN_N[2:1]	HSMB_CLK_IN_N[2:1] 27
HSMB_CLK_OUT_P[2:1]	HSMB_CLK_OUT_P[2:1] 16,27
HSMB_CLK_OUT_N[2:1]	HSMB_CLK_OUT_N[2:1] 16,27
HSMB_TX_D_P[16:0]	HSMB_TX_D_P[16:0] 16,27
HSMB_TX_D_N[16:0]	HSMB_TX_D_N[16:0] 16,27
HSMB_SDA	HSMB_SDA 27
HSMB_CLK_IN0	HSMB_CLK_IN0 27

USER INTERFACE

USER_DIPSW[7:0]	USER_DIPSW[7:0] 17,25
USER_PB[3:0]	USER_PB[3:0] 25

ETHERNET INTERFACE

ENET_RX_D[7..0]	ENET_RX_D[7..0] 14,24
ENET_TX_D[7..0]	ENET_TX_D[7..0] 14,24
ENET_TX_P	ENET_TX_P 24
ENET_TX_N	ENET_TX_N 24
ENET_S_CLKP	ENET_S_CLKP 24
ENET_S_CLKN	ENET_S_CLKN 24

DDR3 DIMM INTERFACE

DDR3_DIMM_A[15:0]	DDR3_DIMM_A[15:0] 15,18
DDR3_DIMM_BA[2:0]	DDR3_DIMM_BA[2:0] 15,18
DDR3_DIMM_CSn[3:0]	DDR3_DIMM_CSn[3:0] 15,18
DDR3_DIMM_CKE[1:0]	DDR3_DIMM_CKE[1:0] 15,18
DDR3_DIMM_SDA	DDR3_DIMM_SDA 18
DDR3_DIMM_RESETn	DDR3_DIMM_RESETn 18
QDRII_RPSn	QDRII_RPSn 19,21

QDRII SRAM INTERFACE

QDRII_A[21:0]	QDRII_A[21:0] 17,19,21

RLDRAM II INTERFACE

RLDC_A[22:0]	RLDC_A[22:0] 14,20,21
FSM_A[26:0]	FSM_A[26:0] 16,17,22,23

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Title: **Stratix IV E FPGA Development Kit Board**

Size	Document Number	Rev
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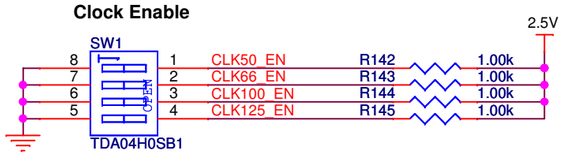
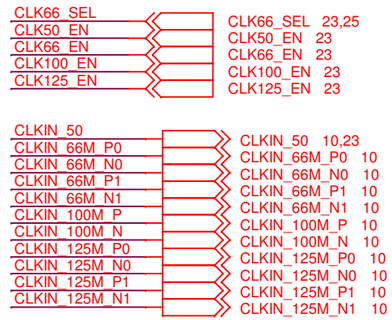
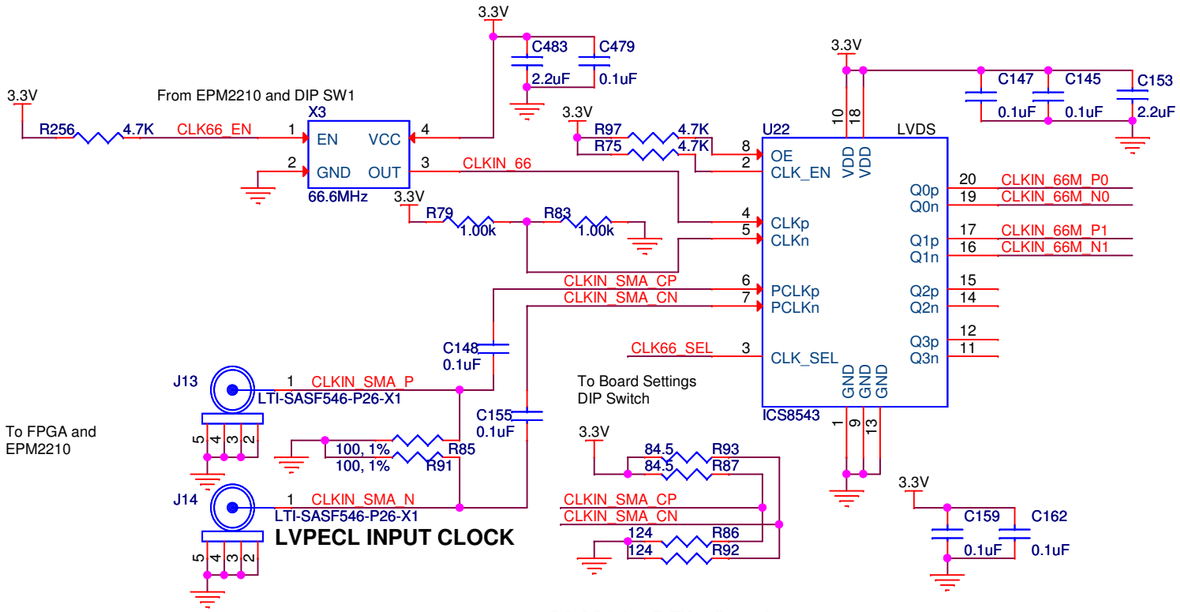
General Clock Circuitry

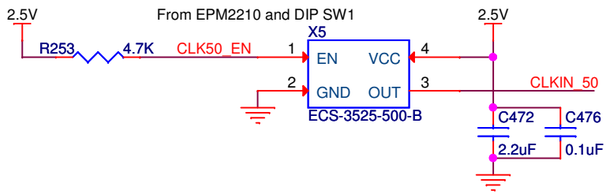
Clock Enable



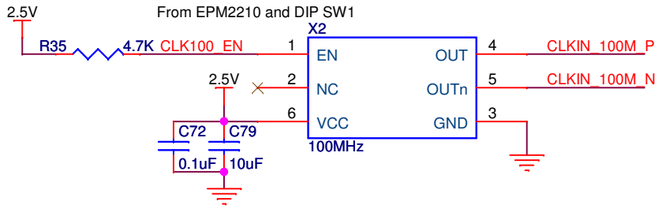
CLOCK INTERFACE





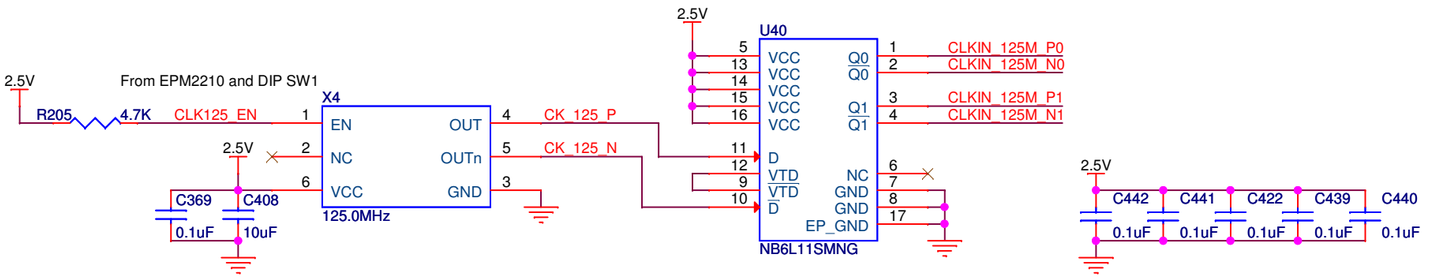


To FPGA and EPM2210



CLK66_SEL Settings:

Setting	SW2, DIP8
High	PCLKp/n
Low	CLKp/n



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix IV E FPGA Development Kit Board**

Size: B | Document Number: 150-0310904-B1 (6XX-41504R) | Rev: B

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Stratix IV E Configuration

Stratix IVE Configuration

U19J

2.5V_VCCPGM

FPGA_DCLK AL3 → DCLK
R276 10.0K FPGA_STATUSn AH28 → nSTATUS
R279 10.0K FPGA_CONFIGn AE25 → nCONFIG
R318 100, 1% FPGA_CONF_DONE AH29 → CONF_DONE
SYS_RESETn U31 → DEV_CLRn/DQ17L/DIFFIO_RX_L27P
R264 10.0K FPGA_INIT_DONE T26 → INIT_DONE/DQ17L/DIFFIO_TX_L27N

Bank 1C

FPGA_DATA0 T28 → DATA0/DQ16L/DIFFIO_TX_L25N
FPGA_DATA1 T27 → DATA1/DQ16L/DIFFIO_TX_L25P
FPGA_DATA2 R34 → DATA2/DQSN16L/DIFFIO_RX_L25N
FPGA_DATA3 R33 → DATA3/DQ20R/DIFFIO_RX_R33N
FPGA_DATA4 T25 → DATA4/DQ16L/DIFFIO_TX_L26N
FPGA_DATA5 T24 → DATA5/DQ16L/DIFFIO_TX_L26P
FPGA_DATA6 T32 → DATA6/DQSN17L/DIFFIO_RX_L26N
FPGA_DATA7 R31 → DATA7/DQS17L/DIFFIO_RX_L26P

U25 → CRC_ERR/DQ17L/DIFFIO_TX_L27P
U32 → DEV_OE/DQ17L/DIFFIO_RX_L27N
R30 → CLKUSR/DQ18R/DIFFIO_RX_R30N
other DQ11 pins are in bank 1 section

R268 10.0K FPGA_CEn AE26 → nCE

EP4SE530H1152
Version = 0.1 Preliminary

TCK F30 JTAG_TCK
TMS H28 JTAG_TMS
TDO G29 JTAG_FPGA_TDO
TDI G28 JTAG_BLASTER_TDO
TRST J28 JTAG_TRST
R257 1.00K → 2.5V_VCCPD

ASDO AH6
TEMPDIODEP E5 TEMPDIODE_P R239 DNI → 2.5V_B4B
TEMPDIODEN D4 TEMPDIODE_N R240 DNI
MSEL0 K10 MSEL0
MSEL1 J9 MSEL1 10.0K R252
MSEL2 K9 MSEL2 10.0K R255
PORSEL AF26
nCSO AE9
nIO_PULLUP AF8
DNU U18
nCEO AJ5

Place at end of chain

JTAG_TCK R132 DNI C256 DNI

Fast Passive Parallel: MSEL[2:0]=000
Passive Serial: MSEL[2:0]=010
FPP w/design security: MSEL[2:0]=001
MSEL pins have internal 5kOhm pull-downs.

J2 1 MSEL0 R2 10.0K → 2.5V_VCCPGM
2
CON2
XJ2
881545-2

CONFIGURATION INTERFACE

FPGA_DATA[7:0] FPGA_DATA[7:0] 23
FPGA_DCLK FPGA_DCLK 23
FPGA_CONF_DONE FPGA_CONF_DONE 23,25
FPGA_STATUSn FPGA_STATUSn 13,23
FPGA_CONFIGn FPGA_CONFIGn 23
SYS_RESETn SYS_RESETn 23,25
FPGA_CEn FPGA_CEn 13

JTAG

JTAG_TCK JTAG_TCK 13,23,27
JTAG_TMS JTAG_TMS 13,23,27
JTAG_FPGA_TDO JTAG_FPGA_TDO 23
JTAG_BLASTER_TDO JTAG_BLASTER_TDO 13
HSMA_JTAG_TDI HSMA_JTAG_TDI 27
HSMB_JTAG_TDI HSMB_JTAG_TDI 27
JTAG_BLASTER_TDI JTAG_BLASTER_TDI 13
JTAG_EPM2210_TDO JTAG_EPM2210_TDO 23
HSMA_JTAG_TDO HSMA_JTAG_TDO 27
HSMB_JTAG_TDO HSMB_JTAG_TDO 27
USB_DISABLEn USB_DISABLEn 13
TEMPDIODE_P TEMPDIODE_P 8
TEMPDIODE_N TEMPDIODE_N 8

USB Blaster Programming Header
(uses JTAG mode only)

XJ3 881545-2
J4 1 USB_DISABLEn R158 1.00k → 2.5V
2
HDR2x1

J24 70247-1051
USB_DISABLEn
2 4 6 8 10
1 3 5 7 9
JTAG_TCK
JTAG_BLASTER_TDI
JTAG_TMS
JTAG_BLASTER_TDO
R159 10.0K → 2.5V
R160 10.0K
R157 1.00k

JTAG Chain Control

XJ4 881545-2
J10 1 2 HDR2x1
1EPM2210_JTAG_EN R36 1.00k → 2.5V

C314 0.1uF
R171 100, 1% → 2.5V

U35
EPM2210_JTAG_EN 4
5 JTAG_EPM2210_TDO
2 JTAG_FPGA_TDO
3 HSMA_JTAG_TDI
7 HSMA_JTAG_TDO
10
9 HSMB_JTAG_TDI
HSMA_JTAG_EN 8
6 NLAS4717EPMTR2G

XJ5 881545-2
J15 1 2 HDR2x1
1 HSMA_JTAG_EN R104 1.00k → 2.5V

C315 0.1uF
R172 100, 1% → 2.5V

XJ6 881545-2
J5 1 2 HDR2x1
1 HSMB_JTAG_EN R11 1.00k → 2.5V

U36
HSMB_JTAG_EN 4
5 HSMB_JTAG_TDO
2
3 JTAG_BLASTER_TDI
7
10
9
8
6 NLAS4717EPMTR2G

Logic 0 = pin 5 --> pin 3 (EPM2210 Enabled)
Logic 1 = pin 2 --> pin 3 (EPM2210 Bypass)

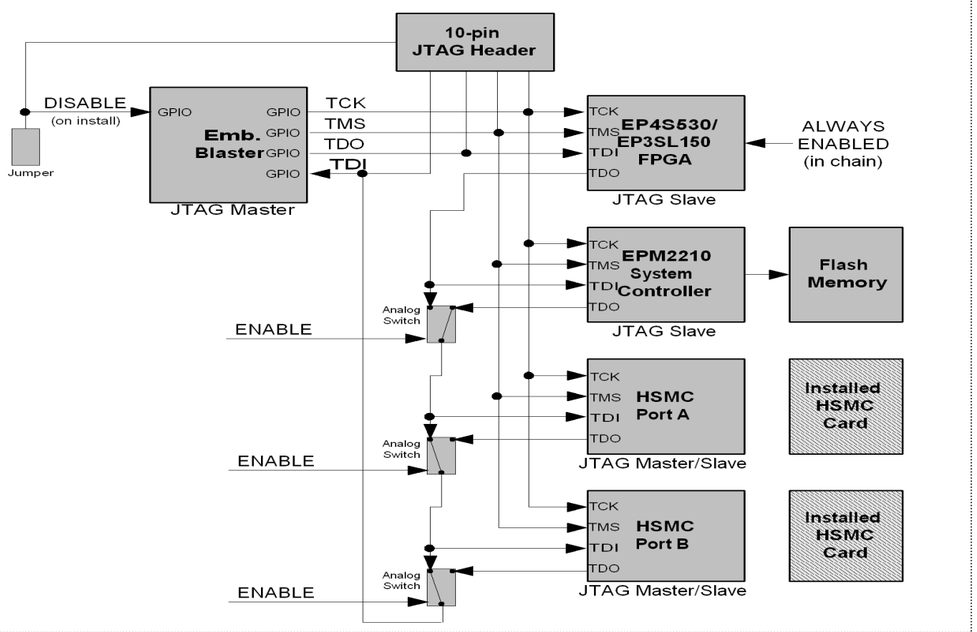
NLAS4717 Switch Functions

When Pins 4 & 8 are:
LOW --> Pins 5 & 7 = ON and Pins 2 & 10 = OFF
HIGH --> Pins 2 &10 = ON and Pins 5 & 7 = OFF

FPGA Not Installed Jumper

J3 DNI
1 JTAG_FPGA_TDO
2 JTAG_BLASTER_TDO

JTAG REFERENCE



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix IV E FPGA Development Kit Board**

Size: B | Document Number: 150-0310904-B1 (6XX-41504R) | Rev: B

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Embedded USB Blaster

USB

J6 USB CON

L1 BLM21PG331SN1

C26 10uF

C32 18pF — C31 18pF — Y1 6.000MHz — USB_XTAL1 — USB_XTAL2

U5 SN65220DBV (NC1, NC2, GNDGND, A, B)

R14 27 — R15 27

R185 10.0K — USB_RESETn

C353 33nF

R182 470 — C329 0.1uF — C352 0.1uF

U7 FT245BL

3V3OUT	6		
USBDM	8	D0	25 USB_D0
USBDP	7	D1	24 USB_D1
RSTOUT#	5	D2	23 USB_D2
XTIN	27	D3	22 USB_D3
XTOUT	28	D4	21 USB_D4
RESET#	4	D5	20 USB_D5
EECS	32	D6	19 USB_D6
EESK	1	D7	18 USB_D7
EEDATA	2	RD#	16 USB_RDn
TEST	31	WR	15 USB_WR
		TXE#	14 USB_TXEn
		RXF#	12 USB_RXFn
		SI/WU	11 USB_SI_WU
		PWREN#	10 USB_PWR_ENn

AVCC 30, VCC1 3, VCC2 26, VCC-IO 13, GND1 9, GND2 17, AGND 29

R187 1.5K

R188 1.00k

U4 AT93C46DN-SH-B (CS, SK, DIN, DOUT, VCC, NC1, NC2, GND)

R168 2.2K — (Optional) — R6 10.0K — USB_EEDATA

DECOUPLING CAPS

C39 10uF 10V Tantalum — C15 0.1uF — C328 0.1uF

U8A — MAX II BANK1

EPM240M100, Pre-programmed

USB_RXFn	B1	IOB1_1	IOB1_17 J7
	C1	IOB1_2	IOB1_18 K10
	C2	IOB1_3	IOB1_19 K3
	D1	IOB1_4	IOB1_20 K4
	D2	IOB1_5	IOB1_21 K5
	D3	IOB1_6	IOB1_22 K6
	E2	IOB1_7	IOB1_23 K7
	F1	IOB1_8	IOB1_24 K9
USB_EECS	F3	IOB1_9	IOB1_25 L1 USB_LED
USB_EESK	G1	IOB1_10	IOB1_26 L10 JTAG_BLASTER_TDO
EEDATA	G2	IOB1_11	IOB1_27 L11
USB_SI_WU	H1	IOB1_12	IOB1_28 L2
USB_DISABLEn	H2	IOB1_13	IOB1_29 L3
USB_PWR_ENn	H3	IOB1_14	IOB1_30 L4 FPGA_CEn
	J5	IOB1_15	IOB1_31 L5
	J6	IOB1_16	IOB1_32 L6 FPGA_STATUSn
			IOB1_33 L7
			IOB1_34 L9 JTAG_TCK
CLKIN_24MHZ	F2	IOB1/CLK0	TCK K1 USB_MAX_TCK
	E1	IOB1/CLK1	TDI J2 USB_MAX_TDI
			TDO K2 USB_MAX_TDO
USB_RESETn	K8	IOB1/DEV_CLRn	TMS J1 USB_MAX_TMS
	L8	IOB1/DEV_OE	

3.3V_MAX — R24 56.2 — D6 Green_LED

USB INTERFACE

JTAG_TCK	JTAG_TCK 12,23,27
JTAG_TMS	JTAG_TMS 12,23,27
JTAG_BLASTER_TDI	JTAG_BLASTER_TDI 12
JTAG_BLASTER_TDO	JTAG_BLASTER_TDO 12
USB_DISABLEn	USB_DISABLEn 12
FPGA_STATUSn	FPGA_STATUSn 12,23
FPGA_CEn	FPGA_CEn 12

U8B — MAX II BANK2

EPM240M100, Pre-programmed

USB_TXEn	A1	IOB2_35	IOB2_51 B5
USB_D1	A10	IOB2_36	IOB2_52 B6
USB_D0	A11	IOB2_37	IOB2_53 B7
USB_WR	A2	IOB2_38	IOB2_54 B8
USB_RDn	A3	IOB2_39	IOB2_55 B9
USB_D7	A4	IOB2_40	IOB2_56 C10
USB_D6	A5	IOB2_41	IOB2_57 C11
USB_D5	A6	IOB2_42	IOB2_58 C5
USB_D4	A7		C6
USB_D3	A8	IOB2_43	IOB2_59 C7
USB_D2	A9	IOB2_44	IOB2_60 D10
	B10	IOB2_45	IOB2_61 D11
	B11	IOB2_46	IOB2_62 D9
	B2	IOB2_47	IOB2_63 E10
	B3	IOB2_48	IOB2_64 E11
	B4	IOB2_49	IOB2_65 F11
		IOB2_50	IOB2_66
			F9
			IOB2_67 G10
			IOB2_68 H10
			IOB2_69 H11
			IOB2_70 H9
			IOB2_71 J10
F10			IOB2_72 J11 JTAG_TMS
G11		IOB2/CLK2	IOB2_73 K11 JTAG_BLASTER_TDI
		IOB2/CLK3	IOB2_74

U38 — LT3010

5V_USB — C379 1uF

IN, NC7, NC6, SHDNn, OUT, SENSE, NC3, GND, EPAD

R196 5.11K — R197 3.16K — C395 0.01uF — C388 1uF — 3.3V_MAX

U8C — MAX II Power

EPM240M100, Pre-programmed

D5	GNDIO	VCCINT	E9
D7	GNDIO	VCCINT	G3
E4	GNDIO		
E8	GNDIO	VCCIO1	E3
G4	GNDIO	VCCIO1	J4
G8	GNDIO	VCCIO1	J8
H5	GNDIO		
H7	GNDIO	VCCIO2	C4
		VCCIO2	C8
		VCCIO2	G9

Y3

3.3V_MAX — R28 1.00k — C59 0.01uF — EN, VCC, GND, OUT — 24MHz — CLKIN_24MHZ — C49 0.01uF — C51 4.7uF — 3.3V_MAX

Install J27 only for prototype

3.3V_MAX — R22 1.00K USB_MAX_TCK — R21 1.00K USB_MAX_TDO, USB_MAX_TMS, USB_MAX_TDI — J26 2x5 — R23 0 — R20 0 — 3.3V_MAX

PLACE NEAR MAX II

3.3V_MAX — C341 0.1uF — C354 0.1uF — C340 0.1uF — C345 0.1uF — C331 0.1uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Stratix IV E FPGA Development Kit Board

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Stratix IV E Banks 1 & 2

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Stratix IVE Bank 1

SEVEN_SEG_SEL3	J29	DQ1L/DIFFIO_TX_L2P	Bank 1A	DQ5L/DIFFIO_TX_L8P	N27 ENET_MDIO
LCD1_DATA2	J30	DQ1L/DIFFIO_TX_L2N		DQ5L/DIFFIO_TX_L8N	M28 HSMB_SCL
MAX_OEn	K27	DQ1L/DIFFIO_TX_L3P		DQ5L/DIFFIO_TX_L9P	P25 LCD1_DATA6
MAX_WEn	K28	DQ1L/DIFFIO_TX_L3N		DQ5L/DIFFIO_TX_L9N	N26 LCD1_D_Cn
ENET_RX_D0	M24	DQ2L/DIFFIO_TX_L4P		DQ6L/DIFFIO_TX_L10P	L31 SEVEN_SEG_E
LCD1_CSn	N25	DQ2L/DIFFIO_TX_L4N		DQ6L/DIFFIO_TX_L10N	L32 SEVEN_SEG_C
LCD1_E_RDn	H31	DQ2L/DIFFIO_RX_L4P		DQ6L/DIFFIO_RX_L10P	H34 ENET_RX_D6
LCD1_DATA1	H32	DQ2L/DIFFIO_RX_L4N		DQ6L/DIFFIO_RX_L10N	G34 EEPROM_CS
ENET_TX_D5	C33	DQS2L/DIFFIO_RX_L3P		DQS5L/DIFFIO_RX_L8P	G33 ENET_TX_D4
ENET_RX_D4	C34	DQSN2L/DIFFIO_RX_L3N		DQSN5L/DIFFIO_RX_L8N	F34 ENET_TX_D1
LCD1_DATA0	F31	DQS1L/DIFFIO_RX_L2P		DQS6L/DIFFIO_RX_L9P	K31 ENET_RX_ER
ENET_INTn	F32	DQSN1L/DIFFIO_RX_L2N		DQSN6L/DIFFIO_RX_L9N	K32 ENET_RX_CLK
SEVEN_SEG_SEL1	M26	DQ3L/DIFFIO_TX_L5P		DQ7L/DIFFIO_TX_L11P	P23 HSMB_RX_LED
SEVEN_SEG_F	M27	DQ3L/DIFFIO_TX_L5N		DQ7L/DIFFIO_TX_L11N	N24 LCD1_BS1
SEVEN_SEG_G	K29	DQ3L/DIFFIO_TX_L6P		DQ7L/DIFFIO_TX_L12P	M29 ENET_TX_ER
SEVEN_SEG_MINUS	K30	DQ3L/DIFFIO_TX_L6N		DQ7L/DIFFIO_TX_L12N	M30 LCD1_DATA7
ENET_TX_D3	L28	DQ4L/DIFFIO_TX_L7P			
SEVEN_SEG_DP	L29	DQ4L/DIFFIO_TX_L7N			J33 LCD1_DATA4
SEVEN_SEG_A	F33	DQ4L/DIFFIO_RX_L7P		DQS7L/DIFFIO_RX_L11P	J34 ENET_RX_D2
LCD1_DATA3	E34	DQ4L/DIFFIO_RX_L7N		DQSN7L/DIFFIO_RX_L11N	
ENET_RX_P	D33	DQS3L/DIFFIO_RX_L5P			
ENET_RX_N	D34	DQSN3L/DIFFIO_RX_L5N			
ENET_RX_COL	J31	DQS4L/DIFFIO_RX_L6P			
ENET_RX_D7	J32	DQSN4L/DIFFIO_RX_L6N		DIFFIO_RX_L12P	K33 ENET_RX_CRS
				DIFFIO_RX_L12N	K34 ENET_MDC
RUP1A	E31	RUP1A/DIFFIO_RX_L1P			
RDN1A	E32	RDN1A/DIFFIO_RX_L1N			

Bank 1B

MAX_CSn	N29	DQ12L/DIFFIO_TX_L19P	Bank 1C	DQ14L/DIFFIO_TX_L22P	T23 EEPROM_DOUT
SEVEN_SEG_B	N30	DQ12L/DIFFIO_TX_L19N		DQ14L/DIFFIO_TX_L22N	R24 LCD1_DATA5
ENET_TX_D0	P28	DQ12L/DIFFIO_TX_L20P		DQ14L/DIFFIO_TX_L23P	R27 SEVEN_SEG_SEL4
ENET_RX_D5	P29	DQ12L/DIFFIO_TX_L20N		DQ14L/DIFFIO_TX_L23N	R28 SEVEN_SEG_SEL2
EEPROM_DIN	R25	DQ13L/DIFFIO_TX_L21P		DQ15L/DIFFIO_RX_L24P	P34 ENET_RX_D1
SEVEN_SEG_D	R26	DQ13L/DIFFIO_TX_L21N		DQ15L/DIFFIO_RX_L24N	N34 ENET_TX_D2
LCD1_WEn	N31	DQ13L/DIFFIO_RX_L21P		DQ15L/DIFFIO_TX_L24P	R29 LCD1_SERn
ENET_RX_DV	P32	DQ13L/DIFFIO_RX_L21N	other DQ11 pin in config section		
ENET_RESETn	M31	DQS12L/DIFFIO_RX_L19P		DQS14L/DIFFIO_RX_L22P	N33 ENET_TX_D6
ENET_LED_LINK1000	N32	DQSN12L/DIFFIO_RX_L19N		DQSN14L/DIFFIO_RX_L22N	M34 ENET_RX_D3
ENET_GTX_CLK	M33	DQS13L/DIFFIO_RX_L20P		DQS15L/DIFFIO_RX_L23P	P31 EEPROM_CLK
ENET_TX_EN	L34	DQSN13L/DIFFIO_RX_L20N		DQSN15L/DIFFIO_RX_L23N	R32 ENET_TX_CLK

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Stratix IVE Bank 2

RLDC_BA1	AC28	DQ28L/DIFFIO_TX_L46P	Bank 2A	DQ32L/DIFFIO_TX_L51P	AD28 RLDC_DQ18
RLDC_CSn	AC29	DQ28L/DIFFIO_TX_L46N		DQ32L/DIFFIO_TX_L51N	AD29 RLDC_DQ19
RLDC_A20	AA24	DQ28L/DIFFIO_TX_L45P		DQ32L/DIFFIO_TX_L52P	AF28 RLDC_DQ22
RLDC_A7	AA25	DQ28L/DIFFIO_TX_L45N		DQ32L/DIFFIO_TX_L52N	AF29 RLDC_DQ23
RLDC_A16	AD30	DQ29L/DIFFIO_TX_L47P		DQ33L/DIFFIO_TX_L53P	AE27 RLDC_DQ30
RLDC_REFn	AD31	DQ29L/DIFFIO_TX_L47N		DQ33L/DIFFIO_TX_L53N	AE28 RLDC_DQ31
RLDC_A14	AH33	DQ29L/DIFFIO_RX_L47P		DQ33L/DIFFIO_RX_L53P	AM34 RLDC_DQ34
RLDC_A15	AG34	DQ29L/DIFFIO_RX_L47N		DQ33L/DIFFIO_RX_L53N	AL34 RLDC_DQ33
RLDC_A17	AE31	DQS28L/DIFFIO_RX_L46P		DQS32L/DIFFIO_RX_L52P	AJ31 RLDC_QK_P1
RLDC_WEn	AE32	DQSN28L/DIFFIO_RX_L46N		DQSN32L/DIFFIO_RX_L52N	AJ32 RLDC_QK_N1
RLDC_CK_P	AF31	DQS29L/DIFFIO_RX_L48P		DQS33L/DIFFIO_RX_L54P	AH30 RLDC_A10
RLDC_CK_N	AF32	DQSN29L/DIFFIO_RX_L48N		DQSN33L/DIFFIO_RX_L54N	AH31 RLDC_DM
RLDC_A5	AB26	DQ30L/DIFFIO_TX_L49P		DQ34L/DIFFIO_TX_L55P	AC25 RLDC_DQ26
RLDC_A9	AB27	DQ30L/DIFFIO_TX_L49N		DQ34L/DIFFIO_TX_L55N	AC26 RLDC_DQ27
RLDC_A3	AB24	DQ30L/DIFFIO_TX_L48P		DQ34L/DIFFIO_TX_L54P	AD26 RLDC_DQ28
RLDC_A2	AB25	DQ30L/DIFFIO_TX_L48N		DQ34L/DIFFIO_TX_L54N	AD27 RLDC_DQ29
RLDC_DQ20	AE29	DQ31L/DIFFIO_TX_L50P			
RLDC_DQ21	AE30	DQ31L/DIFFIO_TX_L50N		DQS34L/DIFFIO_RX_L55P	AL32 RLDC_DQ35
RLDC_DQ24	AG31	DQ31L/DIFFIO_RX_L50P		DQSN34L/DIFFIO_RX_L55N	AL33 RLDC_DQ32
RLDC_DQ25	AG32	DQ31L/DIFFIO_RX_L50N			
	AJ34	DQS30L/DIFFIO_RX_L49P			
RLDC_A12	AH34	DQSN30L/DIFFIO_RX_L49N			
RLDC_DK_P1	AK33	DQS31L/DIFFIO_RX_L51P			AG33 RLDC_A13
RLDC_DK_N1	AK34	DQSN31L/DIFFIO_RX_L51N		DIFFIO_RX_L45P	AF34 RLDC_A18
RUP2A	AK31			DIFFIO_RX_L45N	
RDN2A	AK32	RUP2A/DIFFIO_RX_L56P			
		RDN2A/DIFFIO_RX_L56N			

Bank 2B

RLDC_A6	AA33	DQ18L/DIFFIO_RX_L30P	Bank 2C	DQ21L/DIFFIO_TX_L35P	AA29 RLDC_DQ0
	Y34	DQ18L/DIFFIO_RX_L30N		DQ21L/DIFFIO_TX_L35N	AA30 RLDC_DQ1
RLDC_A4	W26	DQ18L/DIFFIO_TX_L30P		DQ21L/DIFFIO_TX_L34P	Y23 RLDC_DQ13
RLDC_A22	W27	DQ18L/DIFFIO_TX_L30N		DQ21L/DIFFIO_TX_L34N	W24 RLDC_DQ12
RLDC_A21	W30	DQ19L/DIFFIO_TX_L32P		DQ22L/DIFFIO_RX_L36P	AD33 RLDC_DQ4
	W31	DQ19L/DIFFIO_TX_L32N		DQ22L/DIFFIO_RX_L36N	AD34 RLDC_DQ5
RLDC_A1	V24	DQ19L/DIFFIO_TX_L31P		DQ22L/DIFFIO_RX_L36P	Y25 RLDC_DQ7
RLDC_A0	V25	DQ19L/DIFFIO_TX_L31N		DQ22L/DIFFIO_RX_L36N	Y26 RLDC_DQ8
	Y31	DQS18L/DIFFIO_RX_L31P		DQS21L/DIFFIO_RX_L35P	AB31 RLDC_QK_P0
	Y32	DQSN18L/DIFFIO_RX_L31N		DQSN21L/DIFFIO_RX_L35N	AB32 RLDC_QK_N0
RLDC_BA2	AB33	DQS19L/DIFFIO_RX_L32P		DQS22L/DIFFIO_RX_L37P	AC31 RLDC_BA0
RLDC_A8	AA34	DQSN19L/DIFFIO_RX_L32N		DQSN22L/DIFFIO_RX_L37N	AC32 RLDC_QVLD
RLDC_DQ10	AA31	DQ20L/DIFFIO_RX_L33P		DQ23L/DIFFIO_TX_L37P	AA27 RLDC_DQ16
RLDC_DQ11	AA32	DQ20L/DIFFIO_RX_L33N		DQ23L/DIFFIO_TX_L37N	AA28 RLDC_DQ17
RLDC_DQ14	Y28	DQ20L/DIFFIO_TX_L33P		DQ23L/DIFFIO_TX_L38P	AB29 RLDC_DQ2
RLDC_DQ15	Y29	DQ20L/DIFFIO_TX_L33N		DQ23L/DIFFIO_TX_L38N	AB30 RLDC_DQ3
RLDC_DK_P0	AC34	DQS20L/DIFFIO_RX_L34P		DQS23L/DIFFIO_RX_L38P	AE33 RLDC_DQ9
RLDC_DK_N0	AB34	DQSN20L/DIFFIO_RX_L34N		DQSN23L/DIFFIO_RX_L38N	AE34 RLDC_DQ6

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R232 49.9 RUP1A
R231 49.9 RDN1A

1.5V_1.8V_B2

R280 49.9 RUP2A
R282 49.9 RDN2A

MAX II INTERFACE

MAX_CSn 23
MAX_OEn 23
MAX_WEn 23

EEPROM_DOUT 24
EEPROM_CS 24
EEPROM_CLK 24
EEPROM_DIN 24

RLDRAM II INTERFACE

RLDC_DQ[35:0] RLDC_DQ[35:0] 20
RLDC_BA[2:0] RLDC_BA[2:0] 20,21
RLDC_A[22:0] RLDC_A[22:0] 10,20,21
RLDC_DK_P[1:0] RLDC_DK_P[1:0] 20
RLDC_DK_N[1:0] RLDC_DK_N[1:0] 20
RLDC_QK_P[1:0] RLDC_QK_P[1:0] 20
RLDC_QK_N[1:0] RLDC_QK_N[1:0] 20
RLDC_CK_P RLDC_CK_P 20
RLDC_CK_N RLDC_CK_N 20
RLDC_WEn RLDC_WEn 20,21
RLDC_REFn RLDC_REFn 20,21
RLDC_CSn RLDC_CSn 20,21
RLDC_DM RLDC_DM 20
RLDC_QVLD RLDC_QVLD 20

HSMC PORT B

HSMB_SCL HSMB_SCL 27
HSMB_RX_LED HSMB_RX_LED 25

ETHERNET INTERFACE

ENET_RX_D[7..0] ENET_RX_D[7..0] 24
ENET_TX_D[7..0] ENET_TX_D[7..0] 10,24
ENET_GTX_CLK ENET_GTX_CLK 24
ENET_TX_CLK ENET_TX_CLK 24
ENET_TX_ER ENET_TX_ER 24
ENET_TX_EN ENET_TX_EN 24
ENET_MDIO ENET_MDIO 24
ENET_RESETn ENET_RESETn 24
ENET_INTn ENET_INTn 24
ENET_RX_P ENET_RX_P 24
ENET_RX_N ENET_RX_N 24
ENET_RX_ER ENET_RX_ER 24
ENET_RX_CLK ENET_RX_CLK 24
ENET_LED_LINK1000 ENET_LED_LINK1000 24
ENET_RX_COL ENET_RX_COL 24
ENET_RX_DV ENET_RX_DV 24
ENET_RX_CRS ENET_RX_CRS 24
ENET_MDC ENET_MDC 24

128x64 LCD DISPLAY INTERFACE

LCD1_DATA[7:0] LCD1_DATA[7:0] 26
LCD1_CSn LCD1_CSn 26
LCD1_SERn LCD1_SERn 26
LCD1_D_Cn LCD1_D_Cn 26
LCD1_WEn LCD1_WEn 26
LCD1_E_RDn LCD1_E_RDn 26
LCD1_BS1 LCD1_BS1 26

SEVEN-SEG INTERFACE

SEVEN_SEG_SEL[4:1] SEVEN_SEG_SEL[4:1] 25
SEVEN_SEG_A SEVEN_SEG_A 25
SEVEN_SEG_B SEVEN_SEG_B 25
SEVEN_SEG_C SEVEN_SEG_C 25
SEVEN_SEG_D SEVEN_SEG_D 25
SEVEN_SEG_E SEVEN_SEG_E 25
SEVEN_SEG_F SEVEN_SEG_F 25
SEVEN_SEG_G SEVEN_SEG_G 25
SEVEN_SEG_DP SEVEN_SEG_DP 25
SEVEN_SEG_MINUS SEVEN_SEG_MINUS 25

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Stratix IV E Banks 3 & 4

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Stratix IVE Bank 3

DDR3_DIMM_DQ7	AJ26	DQ1B/DIFFOUT_B3P	Bank 3A	DQ4B/DIFFOUT_B11P	AP30	DDR3_DIMM_DQ9	
DDR3_DIMM_DQ6	AH27	DQ1B/DIFFOUT_B1N		DQ4B/DIFFOUT_B11N	AP32	DDR3_DIMM_DQ8	
DDR3_DIMM_DQ5	AJ27	DQ1B/DIFFOUT_B1P		DQ4B/DIFFIO_RX_B6P	AN31	DDR3_DIMM_DQ11	
DDR3_DIMM_DQ4	AJ29	DQ1B/DIFFOUT_B3N		DQ4B/DIFFIO_RX_B6N	AP31	DDR3_DIMM_DQ10	
DDR3_DIMM_DQ3	AM30	DQ2B/DIFFIO_RX_B3P		DQ5B/DIFFOUT_B15N	AK25	DDR3_DIMM_DQ22	
DDR3_DIMM_DQ2	AN30	DQ2B/DIFFIO_RX_B3N		DQ5B/DIFFOUT_B13N	AK27	DDR3_DIMM_DQ20	
DDR3_DIMM_DQ1	AM29	DQ2B/DIFFOUT_B5P		DQ5B/DIFFOUT_B13P	AL28	DDR3_DIMM_DQ21	
DDR3_DIMM_DQ0	AL29	DQ2B/DIFFOUT_B5N		DQ5B/DIFFOUT_B15P	AM26	DDR3_DIMM_DQ23	
DDR3_DIMM_DM0	AJ28	RUP3A/DQS1B/DIFFIO_RX_B1P		DQS4B/DIFFIO_RX_B5P	AN33	DDR3_DIMM_DQS_P1	
DDR3_DIMM_DQS_N9	AK28	RDN3A/DQSN1B/DIFFIO_RX_B1N		DQSN4B/DIFFIO_RX_B5N	AP33	DDR3_DIMM_DQS_N1	
DDR3_DIMM_DQS_P0	AM31	DQS2B/DIFFIO_RX_B2P		DQS5B/DIFFIO_RX_B7P	AL26	DDR3_DIMM_DM2	
DDR3_DIMM_DQS_N0	AM32	DQSN2B/DIFFIO_RX_B2N		DQSN5B/DIFFIO_RX_B7N	AL27	DDR3_DIMM_DQS_N11	
DDR3_DIMM_DQ15	AF23	DQ3B/DIFFOUT_B9P		DQ6B/DIFFOUT_B17N	AM28	DDR3_DIMM_DQ16	
DDR3_DIMM_DQ13	AF24	DQ3B/DIFFOUT_B7P		DQ6B/DIFFOUT_B17P	AP29	DDR3_DIMM_DQ17	
DDR3_DIMM_DQ14	AH25	DQ3B/DIFFOUT_B9N		DQ6B/DIFFIO_RX_B9P	AN27	DDR3_DIMM_DQ19	
DDR3_DIMM_DQ12	AH26	DQ3B/DIFFOUT_B7N		DQ6B/DIFFIO_RX_B9N	AP27	DDR3_DIMM_DQ18	
DDR3_DIMM_DM1	AG24	DQS3B/DIFFIO_RX_B4P		DQS6B/DIFFIO_RX_B8P	AN28	DDR3_DIMM_DQS_P2	
DDR3_DIMM_DQS_N10	AH24	DQSN3B/DIFFIO_RX_B4N		DQSN6B/DIFFIO_RX_B8N	AP28	DDR3_DIMM_DQS_N2	
DDR3_DIMM_TEST2	AE24	DQ7B/DIFFOUT_B19N		DQS7B/DIFFIO_RX_B10P	AC22	DDR3_DIMM_TEST1	
	AE23	DQ7B/DIFFOUT_B19P		DQSN7B/DIFFIO_RX_B10N	AD22		
DDR3_DIMM_DQ28	AH23	DQ9B/DIFFOUT_B25N	Bank 3B	DQ11B/DIFFOUT_B33N	AD21	DDR3_DIMM_DQ70	
DDR3_DIMM_DQ30	AJ23	DQ9B/DIFFOUT_B27N		DQ11B/DIFFOUT_B33P	AE20	DDR3_DIMM_DQ71	
DDR3_DIMM_DQ29	AJ24	DQ9B/DIFFOUT_B25P		DQ11B/DIFFOUT_B31P	AE21	DDR3_DIMM_DQ69	
DDR3_DIMM_DQ31	AK22	DQ9B/DIFFOUT_B27P		DQ11B/DIFFOUT_B31N	AE22	DDR3_DIMM_DQ68	
DDR3_DIMM_DQ24	AK24	DQ10B/DIFFOUT_B29N		DQ12B/DIFFOUT_B35P	AP23	DDR3_DIMM_DQ65	
DDR3_DIMM_DQ25	AL25	DQ10B/DIFFOUT_B29P		DQ12B/DIFFOUT_B35N	AP26	DDR3_DIMM_DQ64	
DDR3_DIMM_DQ27	AL23	DQ10B/DIFFIO_RX_B15P		DQ12B/DIFFIO_RX_B18P	AN24	DDR3_DIMM_DQ67	
DDR3_DIMM_DQ26	AM23	DQ10B/DIFFIO_RX_B15N		DQ12B/DIFFIO_RX_B18N	AP24	DDR3_DIMM_DQ66	
DDR3_DIMM_DM3	AH22	DQS9B/DIFFIO_RX_B13P		DQS11B/DIFFIO_RX_B16P	AF21	DDR3_DIMM_DM8	
DDR3_DIMM_DQS_N12	AJ22	DQSN9B/DIFFIO_RX_B13N		DQSN11B/DIFFIO_RX_B16N	AG21	DDR3_DIMM_DQS_N17	
DDR3_DIMM_DQS_P3	AL24	DQS10B/DIFFIO_RX_B14P		DQS12B/DIFFIO_RX_B17P	AN25	DDR3_DIMM_DQS_P8	
DDR3_DIMM_DQS_N3	AM24	DQSN10B/DIFFIO_RX_B14N		DQSN12B/DIFFIO_RX_B17N	AP25	DDR3_DIMM_DQS_N8	
DDR3_DIMM_DQ38	AJ20	DQ17B/DIFFOUT_B51N	Bank 3C	DQ19B/DIFFOUT_B57N	AK18	DDR3_DIMM_A9	
DDR3_DIMM_DQ36	AL22	DQ17B/DIFFOUT_B49N		DQ19B/DIFFOUT_B57P	AL18	DDR3_DIMM_A2	
DDR3_DIMM_DQ39	AJ21	DQ17B/DIFFOUT_B51P		DQ19B/DIFFOUT_B55N	AL20	DDR3_DIMM_A11	
DDR3_DIMM_DQ37	AM22	DQ17B/DIFFOUT_B49P		DQ19B/DIFFOUT_B55P	AM18	DDR3_DIMM_A3	
DDR3_DIMM_DQ32	AM21	DQ18B/DIFFOUT_B53N					
DDR3_DIMM_DQ33	AP20	DQ18B/DIFFOUT_B53P		DQS19B/DIFFIO_RX_B28P	AL19	DDR3_DIMM_A6	
DDR3_DIMM_DQ35	AN21	DQ18B/DIFFIO_RX_B27P		DQSN19B/DIFFIO_RX_B28N	AM19	DDR3_DIMM_A7	
DDR3_DIMM_DQ34	AP21	DQ18B/DIFFIO_RX_B27N					
DDR3_DIMM_DM4	AK21	RUP3C/DQS17B/DIFFIO_RX_B25P		DIFFIO_RX_B29P	AF19	DDR3_DIMM_TEST3	
DDR3_DIMM_DQS_N13	AL21	RDN3C/DQSN17B/DIFFIO_RX_B25N		DIFFIO_RX_B29N	AF20	DDR3_DIMM_SCL	
DDR3_DIMM_DQS_P4	AN22	DQS18B/DIFFIO_RX_B26P		DIFFIO_RX_B30P	AG19	DDR3_DIMM_ERR_OUTn	
DDR3_DIMM_DQS_N4	AP22	DQSN18B/DIFFIO_RX_B26N		DIFFIO_RX_B30N	AH19	DDR3_DIMM_PAR_IN	

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Stratix IVE Bank 4

DDR3_DIMM_DQ50	AG12	DQ33B/DIFFOUT_B112P	Bank 4A	DQ36B/DIFFOUT_B122P	AL4	DDR3_DIMM_DQ62	
DDR3_DIMM_DQ51	AJ13	DQ33B/DIFFOUT_B112N		DQ36B/DIFFOUT_B122N	AM4	DDR3_DIMM_DQ63	
DDR3_DIMM_DQ48	AH12	DQ33B/DIFFIO_RX_B56P		DQ36B/DIFFOUT_B120P	AM6	DDR3_DIMM_DQ60	
DDR3_DIMM_DQ49	AJ12	DQ33B/DIFFIO_RX_B56N		DQ36B/DIFFOUT_B120N	AN6	DDR3_DIMM_DQ61	
DDR3_DIMM_DQ52	AJ10	DQ34B/DIFFOUT_B114P		DQ37B/DIFFOUT_B124P	AJ6		
DDR3_DIMM_DQ53	AL8	DQ34B/DIFFOUT_B114N		DQ37B/DIFFOUT_B124N	AK6		
DDR3_DIMM_DQ54	AL7	DQ34B/DIFFOUT_B116P		DQ37B/DIFFIO_RX_B62P	AJ7	DDR3_DIMM_CLK_P1	
DDR3_DIMM_DQ55	AJ9	DQ34B/DIFFOUT_B116N		DQ37B/DIFFIO_RX_B62N	AK7	DDR3_DIMM_CLK_N1	
DDR3_DIMM_DQS_P6	AH11	DQS33B/DIFFIO_RX_B57P		DQS36B/DIFFIO_RX_B61P	AL5	DDR3_DIMM_DM7	
DDR3_DIMM_DQS_N6	AJ11	DQSN33B/DIFFIO_RX_B57N		DQSN36B/DIFFIO_RX_B61N	AM5	DDR3_DIMM_DQS_N16	
DDR3_DIMM_DM6	AK9	DQS34B/DIFFIO_RX_B58P		DQS37B/DIFFIO_RX_B63P	AH8	DDR3_DIMM_CLK_P0	
DDR3_DIMM_DQS_N15	AL9	DQSN34B/DIFFIO_RX_B58N		DQSN37B/DIFFIO_RX_B63N	AJ8	DDR3_DIMM_CLK_N0	
DDR3_DIMM_DQ58	AP2	DQ35B/DIFFOUT_B118P		DQ38B/DIFFOUT_B128P	AE10		
DDR3_DIMM_DQ59	AP5	DQ35B/DIFFOUT_B118N		DQ38B/DIFFOUT_B128N	AF10		
DDR3_DIMM_DQ56	AN4	DQ35B/DIFFIO_RX_B59P		DQ38B/DIFFOUT_B126P	AE11	DDR3_DIMM_EVENTn	
DDR3_DIMM_DQ57	AP4	DQ35B/DIFFIO_RX_B59N		DQ38B/DIFFOUT_B126N	AF11	DDR3_DIMM_TEST4	
DDR3_DIMM_DQS_P7	AN3	DQS35B/DIFFIO_RX_B60P		DQ32B/DIFFOUT_B110P	AE12		
DDR3_DIMM_DQS_N7	AP3	DQSN35B/DIFFIO_RX_B60N		DQ32B/DIFFOUT_B110N	AD13		
RUP4A	AG9	RUP4A/DQS38B/DIFFIO_RX_B64P		DQS32B/DIFFIO_RX_B55P	AC12	DDR3_DIMM_TEST5	
RDN4A	AH9	RDN4A/DQSN38B/DIFFIO_RX_B64N		DQSN32B/DIFFIO_RX_B55N	AD12		
LCD_DATA0	AP9	DQ27B/DIFFOUT_B94P	Bank 4B	DQ29B/DIFFOUT_B100P	AK10		
LCD_DATA1	AP11	DQ27B/DIFFOUT_B94N		DQ29B/DIFFOUT_B100N	AM11		
LCD_DATA2	AN10	DQ27B/DIFFIO_RX_B47P		DQ29B/DIFFIO_RX_B50P	AK12	HSMA_RX_LED	
LCD_DATA3	AP10	DQ27B/DIFFIO_RX_B47N		DQ29B/DIFFIO_RX_B50N	AL12	LCD1_RSTn	
LCD_DATA4	AE13	DQ28B/DIFFOUT_B98P		DQ30B/DIFFOUT_B102P	AM8		
LCD_DATA5	AE14	DQ28B/DIFFOUT_B98N		DQ30B/DIFFOUT_B102N	AP8		
LCD_DATA6	AE15	DQ28B/DIFFOUT_B96P		DQ30B/DIFFOUT_B104P	AP6		
LCD_DATA7	AF15	DQ28B/DIFFOUT_B96N		DQ30B/DIFFOUT_B104N	AM7		
LCD_D_Cn	AF13	DQS28B/DIFFIO_RX_B49P		DQS29B/DIFFIO_RX_B51P	AL10	HSMA_D0	
LCD_WEn	AF14	DQSN28B/DIFFIO_RX_B49N		DQSN29B/DIFFIO_RX_B51N	AL11	HSMA_D1	
LCD_CSn	AM9	DQS27B/DIFFIO_RX_B48P		DQS30B/DIFFIO_RX_B52P	AN7	HSMA_D2	
SPEAKER_OUT	AN9	DQSN27B/DIFFIO_RX_B48N		DQSN30B/DIFFIO_RX_B52N	AP7	HSMA_D3	
DDR3_DIMM_CASn	AK13	DQ20B/DIFFOUT_B74P	Bank 4C	DQ22B/DIFFOUT_B80P	AM12	DDR3_DIMM_DQ45	
DDR3_DIMM_ODT1	AL13	DQ20B/DIFFOUT_B74N		DQ22B/DIFFOUT_B80N	AP13	DDR3_DIMM_DQ44	
DDR3_DIMM_RASn	AL15	DQ20B/DIFFOUT_B72P		DQ22B/DIFFOUT_B78P	AP14	DDR3_DIMM_DQ47	
DDR3_DIMM_BA0	AM15	DQ20B/DIFFOUT_B72N		DQ22B/DIFFOUT_B78N	AN13	DDR3_DIMM_DQ46	
DDR3_DIMM_DQ42	AG15	DQ21B/DIFFOUT_B76P					
DDR3_DIMM_DQ43	AK15	DQ21B/DIFFOUT_B76N		DQS22B/DIFFIO_RX_B40P	AN12	DDR3_DIMM_DM5	
DDR3_DIMM_DQ40	AH15	DQ21B/DIFFIO_RX_B38P		DQSN22B/DIFFIO_RX_B40N	AP12	DDR3_DIMM_DQS_N14	
DDR3_DIMM_DQ41	AJ15	DQ21B/DIFFIO_RX_B38N					
DDR3_DIMM_ODT0	AL14	DQS20B/DIFFIO_RX_B37P		DIFFIO_RX_B35P	AL16	DDR3_DIMM_CSn0	
DDR3_DIMM_WEn	AM14	DQSN20B/DIFFIO_RX_B37N		DIFFIO_RX_B35N	AM16	DDR3_DIMM_BA1	
DDR3_DIMM_DQS_P5	AH14	DQS21B/DIFFIO_RX_B39P		DIFFIO_RX_B36P	AJ16	DDR3_DIMM_CKE0	
DDR3_DIMM_DQS_N5	AJ14	DQSN21B/DIFFIO_RX_B39N		DIFFIO_RX_B36N	AK16	DDR3_DIMM_BA2	

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DDR3 DIMM INTERFACE

DDR3_DIMM_DQ[71:0]	DDR3_DIMM_DQ[71:0]	18
DDR3_DIMM_DQS_P[8:0]	DDR3_DIMM_DQS_P[8:0]	18
DDR3_DIMM_DQS_N[17:0]	DDR3_DIMM_DQS_N[17:0]	18
DDR3_DIMM_DM[8:0]	DDR3_DIMM_DM[8:0]	18
DDR3_DIMM_A[15:0]	DDR3_DIMM_A[15:0]	10,18
DDR3_DIMM_CLK_P[1:0]	DDR3_DIMM_CLK_P[1:0]	18
DDR3_DIMM_CLK_N[1:0]	DDR3_DIMM_CLK_N[1:0]	18
DDR3_DIMM_CSn[3:0]	DDR3_DIMM_CSn[3:0]	10,18
DDR3_DIMM_CKE[1:0]	DDR3_DIMM_CKE[1:0]	10,18
DDR3_DIMM_BA[2:0]	DDR3_DIMM_BA[2:0]	18
DDR3_DIMM_ODT[1:0]	DDR3_DIMM_ODT[1:0]	18
DDR3_DIMM_SCL	DDR3_DIMM_SCL	18
DDR3_DIMM_PAR_IN	DDR3_DIMM_PAR_IN	18
DDR3_DIMM_ERR_OUTn	DDR3_DIMM_ERR_OUTn	18
DDR3_DIMM_EVENTn	DDR3_DIMM_EVENTn	18
DDR3_DIMM_RASn	DDR3_DIMM_RASn	18
DDR3_DIMM_CASn	DDR3_DIMM_CASn	18
DDR3_DIMM_WEn	DDR3_DIMM_WEn	18

128x64 LCD DISPLAY INTERFACE

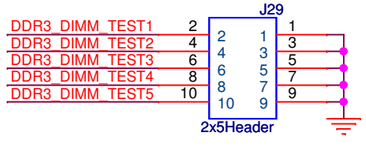
LCD1_RSTn	LCD1_RSTn	26

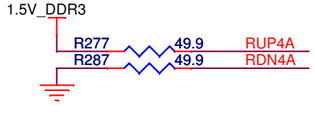
LCD DISPLAY INTERFACE

LCD_DATA[7:0]	LCD_DATA[7:0]	26
LCD_CSn	LCD_CSn	26
LCD_D_Cn	LCD_D_Cn	26
LCD_WEn	LCD_WEn	26

HSMA INTERFACE

HSMA_D[3:0]	HSMA_D[3:0]	27
HSMA_RX_LED	HSMA_RX_LED	25
SPEAKER_OUT	SPEAKER_OUT	26





Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix IV E FPGA Development Kit Board**

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Stratix IV E Banks 5 & 6

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Stratix IVE Bank 5

HSMA_TX_D_P3	AE8	DQ1R/DIFFIO_TX_R2P	Bank 5A	DQ5R/DIFFIO_TX_R8P	AB8 HSMA_TX_D_P10
HSMA_TX_D_N3	AE7	DQ1R/DIFFIO_TX_R2N		DQ5R/DIFFIO_TX_R8N	AC7 HSMA_TX_D_N10
HSMA_TX_D_P4	AF6	DQ1R/DIFFIO_TX_R3P		DQ5R/DIFFIO_TX_R9P	AA10
HSMA_TX_D_N4	AF5	DQ1R/DIFFIO_TX_R3N		DQ5R/DIFFIO_TX_R9N	AB9
HSMA_TX_D_P1	AC9	DQ2R/DIFFIO_TX_R4P		DQ6R/DIFFIO_TX_R10P	AC6 HSMA_TX_D_P8
HSMA_TX_D_N1	AC8	DQ2R/DIFFIO_TX_R4N		DQ6R/DIFFIO_TX_R10N	AC5 HSMA_TX_D_N8
HSMA_RX_D_P3	AL2	DQ2R/DIFFIO_RX_R4P		DQ6R/DIFFIO_RX_R10P	AF2 HSMA_RX_D_P8
HSMA_RX_D_N3	AL1	DQ2R/DIFFIO_RX_R4N		DQ6R/DIFFIO_RX_R10N	AF1 HSMA_RX_D_N8
HSMA_RX_D_P2	AM2	DQS1R/DIFFIO_RX_R2P		DQS5R/DIFFIO_RX_R8P	AF4 HSMA_RX_D_P6
HSMA_RX_D_N2	AM1	DQSN1R/DIFFIO_RX_R2N		DQSN5R/DIFFIO_RX_R8N	AF3 HSMA_RX_D_N6
HSMA_RX_D_P0	AJ4	DQS2R/DIFFIO_RX_R3P		DQS6R/DIFFIO_RX_R9P	AG1 HSMA_RX_D_P7
HSMA_RX_D_N0	AJ3	DQSN2R/DIFFIO_RX_R3N		DQSN6R/DIFFIO_RX_R9N	AH1 HSMA_RX_D_N7
HSMA_TX_D_P6	AE6	DQ3R/DIFFIO_TX_R5P		DQ7R/DIFFIO_TX_R11P	AA12 HSMA_TX_D_P16
HSMA_TX_D_N6	AE5	DQ3R/DIFFIO_TX_R5N		DQ7R/DIFFIO_TX_R11N	AB11 HSMA_TX_D_N16
HSMA_TX_D_P0	AC11	DQ3R/DIFFIO_TX_R6P		DQ7R/DIFFIO_TX_R12P	AD4 HSMA_TX_D_P7
HSMA_TX_D_N0	AB10	DQ3R/DIFFIO_TX_R6N		DQ7R/DIFFIO_TX_R12N	AD3 HSMA_TX_D_N7
HSMA_TX_D_P5	AD7	DQ4R/DIFFIO_TX_R7P			
HSMA_TX_D_N5	AD6	DQ4R/DIFFIO_TX_R7N		DQS7R/DIFFIO_RX_R11P	AE4 HSMA_RX_D_P10
HSMA_RX_D_P5	AH2	DQ4R/DIFFIO_RX_R7P		DQSN7R/DIFFIO_RX_R11N	AE3 HSMA_RX_D_N10
HSMA_RX_D_N5	AJ1	DQ4R/DIFFIO_RX_R7N			
HSMA_RX_D_P1	AG4	DQS3R/DIFFIO_RX_R5P		RUP5A/DIFFIO_RX_R1P	AK4 RUP5A
HSMA_RX_D_N1	AG3	DQSN3R/DIFFIO_RX_R5N		RDN5A/DIFFIO_RX_R1N	AK3 RDN5A
HSMA_RX_D_P4	AJ2	DQS4R/DIFFIO_RX_R6P			
HSMA_RX_D_N4	AK1	DQSN4R/DIFFIO_RX_R6N			
HSMA_RX_D_P9	AE2	DIFFIO_RX_R12P			
HSMA_RX_D_N9	AE1	DIFFIO_RX_R12N			

Bank 5B

HSMA_TX_D_P9	AB6	DQ12R/DIFFIO_TX_R19P	Bank 5C	DQ15R/DIFFIO_TX_R24P	Y6 HSMA_TX_D_P11
HSMA_TX_D_N9	AB5	DQ12R/DIFFIO_TX_R19N		DQ15R/DIFFIO_TX_R24N	Y5 HSMA_TX_D_N11
HSMA_TX_D_P12	AA7	DQ12R/DIFFIO_TX_R20P		DQ15R/DIFFIO_RX_R24P	AA1 HSMA_RX_D_P13
HSMA_TX_D_N12	AA6	DQ12R/DIFFIO_TX_R20N		DQ15R/DIFFIO_RX_R24N	AB1 HSMA_RX_D_N13
HSMA_TX_D_P14	Y10	DQ13R/DIFFIO_TX_R21P		DQ16R/DIFFIO_TX_R25P	W8 HSMB_TX_D_P12
HSMA_TX_D_N14	Y9	DQ13R/DIFFIO_TX_R21N		DQ16R/DIFFIO_TX_R25N	W7 HSMB_TX_D_N12
HSMA_RX_D_P15	AB4	DQ13R/DIFFIO_RX_R21P		DQ16R/DIFFIO_TX_R26P	W11 HSMA_CLK_OUT0
HSMA_RX_D_N15	AA3	DQ13R/DIFFIO_RX_R21N		DQ16R/DIFFIO_TX_R26N	W10 FSM_A26
HSMA_RX_D_P14	AC4	DQS12R/DIFFIO_RX_R19P		DQS15R/DIFFIO_RX_R23P	AA4 HSMA_RX_D_P16
HSMA_RX_D_N14	AB3	DQSN12R/DIFFIO_RX_R19N		DQSN15R/DIFFIO_RX_R23N	Y3 HSMA_RX_D_N16
HSMA_RX_D_P11	AC2	DQS13R/DIFFIO_RX_R20P		DQS16R/DIFFIO_RX_R25P	Y4 CPU_RESETn
HSMA_RX_D_N11	AD1	DQSN13R/DIFFIO_RX_R20N		DQSN16R/DIFFIO_RX_R25N	W3
HSMA_TX_D_P13	Y8	DQ14R/DIFFIO_TX_R22P		DQ17R/DIFFIO_TX_R27P	W6
HSMA_TX_D_N13	Y7	DQ14R/DIFFIO_TX_R22N		DQ17R/DIFFIO_TX_R27N	W5 HSMB_D1
HSMA_TX_D_P15	W12	DQ14R/DIFFIO_TX_R23P		DQ17R/DIFFIO_RX_R27P	V4
HSMA_TX_D_N15	Y11	DQ14R/DIFFIO_TX_R23N		DQ17R/DIFFIO_RX_R27N	V3 HSMA_SDA
HSMA_RX_D_P12	AB2	DQS14R/DIFFIO_RX_R22P		DQS17R/DIFFIO_RX_R26P	Y2 HSMA_SCL
HSMA_RX_D_N12	AC1	DQSN14R/DIFFIO_RX_R22N		DQSN17R/DIFFIO_RX_R26N	Y1

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Stratix IVE Bank 6

HSMB_TX_D_P0	P11	DQ28R/DIFFIO_TX_R45P	Bank 6A	DQ32R/DIFFIO_TX_R52P	J7 HSMB_TX_D_P11
HSMB_TX_D_N0	P10	DQ28R/DIFFIO_TX_R45N		DQ32R/DIFFIO_TX_R52N	J6 HSMB_TX_D_N11
HSMB_TX_D_P7	M7	DQ28R/DIFFIO_TX_R46P		DQ32R/DIFFIO_TX_R51P	N11 HSMB_TX_D_P16
HSMB_TX_D_N7	M6	DQ28R/DIFFIO_TX_R46N		DQ32R/DIFFIO_TX_R51N	N10 HSMB_TX_D_N16
HSMB_TX_D_P9	L5	DQ29R/DIFFIO_TX_R47P		DQ33R/DIFFIO_TX_R53P	K8 HSMB_TX_D_P13
HSMB_TX_D_N9	L4	DQ29R/DIFFIO_TX_R47N		DQ33R/DIFFIO_TX_R53N	K7 HSMB_TX_D_N13
HSMB_RX_D_P9	G2	DQ29R/DIFFIO_RX_R47P		DQ33R/DIFFIO_RX_R53P	G5 HSMB_RX_D_P15
HSMB_RX_D_N9	H1	DQ29R/DIFFIO_RX_R47N		DQ33R/DIFFIO_RX_R53N	G4 HSMB_RX_D_N15
HSMB_RX_D_P6	K4	DQS28R/DIFFIO_RX_R46P		DQS32R/DIFFIO_RX_R52P	F4 HSMB_RX_D_P16
HSMB_RX_D_N6	K3	DQSN28R/DIFFIO_RX_R46N		DQSN32R/DIFFIO_RX_R52N	F3 HSMB_RX_D_N16
HSMB_RX_D_P7	J4	DQS29R/DIFFIO_RX_R48P		DQS33R/DIFFIO_RX_R54P	C1 HSMB_RX_D_P13
HSMB_RX_D_N7	J3	DQSN29R/DIFFIO_RX_R48N		DQSN33R/DIFFIO_RX_R54N	D1 HSMB_RX_D_N13
HSMB_TX_D_P6	N9	DQ30R/DIFFIO_TX_R49P		DQ34R/DIFFIO_TX_R55P	L9 HSMB_TX_D_P14
HSMB_TX_D_N6	N8	DQ30R/DIFFIO_TX_R49N		DQ34R/DIFFIO_TX_R55N	L8 HSMB_TX_D_N14
HSMB_TX_D_P8	L7	DQ30R/DIFFIO_TX_R48P		DQ34R/DIFFIO_TX_R54P	M10 HSMB_TX_D_P15
HSMB_TX_D_N8	L6	DQ30R/DIFFIO_TX_R48N		DQ34R/DIFFIO_TX_R54N	M9 HSMB_TX_D_N15
HSMB_RX_D_P11	H4	DQ31R/DIFFIO_RX_R50P			
HSMB_RX_D_N11	H3	DQ31R/DIFFIO_RX_R50N		DQS34R/DIFFIO_RX_R55P	D3 HSMB_RX_D_P14
HSMB_TX_D_P10	K6	DQ31R/DIFFIO_TX_R50P		DQSN34R/DIFFIO_RX_R55N	D2 HSMB_RX_D_N14
HSMB_TX_D_N10	K5	DQ31R/DIFFIO_TX_R50N			
HSMB_RX_D_P10	F1	DQS30R/DIFFIO_RX_R49P		DIFFIO_RX_R45P	H2 HSMB_RX_D_P8
HSMB_RX_D_N10	G1	DQSN30R/DIFFIO_RX_R49N		DIFFIO_RX_R45N	J1 HSMB_RX_D_N8
HSMB_RX_D_P12	E2	DQS31R/DIFFIO_RX_R51P			
HSMB_RX_D_N12	E1	DQSN31R/DIFFIO_RX_R51N			
RUP6A	E4	RUP6A/DIFFIO_RX_R56P			
RDN6A	E3	RDN6A/DIFFIO_RX_R56N			

Bank 6B

HSMB_RX_D_P2	P2	DQ18R/DIFFIO_RX_R30P	Bank 6C	DQ21R/DIFFIO_TX_R34P	P6 HSMB_CLK_OUT_P1
HSMB_RX_D_N2	R1	DQ18R/DIFFIO_RX_R30N		DQ21R/DIFFIO_TX_R34N	P5 HSMB_CLK_OUT_N1
HSMB_TX_D_P2	T7	DQ18R/DIFFIO_TX_R30P		DQ21R/DIFFIO_TX_R35P	R12 HSMA_CLK_OUT_P2
HSMB_TX_D_N2	U6	DQ18R/DIFFIO_TX_R30N		DQ21R/DIFFIO_TX_R35N	T11 HSMA_CLK_OUT_N2
HSMB_TX_D_P3	T5	DQ19R/DIFFIO_TX_R32P		DQ22R/DIFFIO_TX_R36P	R10 HSMB_TX_D_P4
HSMB_TX_D_N3	T4	DQ19R/DIFFIO_TX_R32N		DQ22R/DIFFIO_TX_R36N	R9 HSMB_TX_D_N4
HSMB_TX_D_P1	T9	DQ19R/DIFFIO_TX_R31P		DQ22R/DIFFIO_TX_R36P	L2 HSMB_RX_D_P5
HSMB_TX_D_N1	T8	DQ19R/DIFFIO_TX_R31N		DQ22R/DIFFIO_RX_R36N	L1 HSMB_RX_D_N5
HSMB_RX_D_P3	N2	DQS19R/DIFFIO_RX_R32P		DQS21R/DIFFIO_RX_R35P	N4 HSMB_TX_LED
HSMB_RX_D_N3	P1	DQSN19R/DIFFIO_RX_R32N		DQSN21R/DIFFIO_RX_R35N	N3 MAX_CLK
HSMB_RX_D_P0	R4	DQS18R/DIFFIO_RX_R31P		DQS22R/DIFFIO_RX_R37P	M4
HSMB_RX_D_N0	R3	DQSN18R/DIFFIO_RX_R31N		DQSN22R/DIFFIO_RX_R37N	M3
HSMB_RX_D_P1	P4	DQ20R/DIFFIO_RX_R33P		DQ23R/DIFFIO_TX_R37P	P8 HSMB_D3
HSMB_RX_D_N1	P3	DQ20R/DIFFIO_RX_R33N		DQ23R/DIFFIO_TX_R37N	P7 HSMB_D0
HSMB_TX_D_P5	R7	DQ20R/DIFFIO_TX_R33P		DQ23R/DIFFIO_TX_R38P	N6 HSMB_CLK_OUT0
HSMB_TX_D_N5	R6	DQ20R/DIFFIO_TX_R33N		DQ23R/DIFFIO_TX_R38N	N5 HSMB_D2
HSMB_RX_D_P4	M1	DQS20R/DIFFIO_RX_R34P		DQS23R/DIFFIO_RX_R38P	K2
HSMB_RX_D_N4	N1	DQSN20R/DIFFIO_RX_R34N		DQSN23R/DIFFIO_RX_R38N	K1 MAX_TO_STRATIX4

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Version = 0.1 Preliminary

2.5V_B5_B6
R281 49.9 RUP5A
R283 49.9 RDN5A

2.5V_B5_B6
R250 49.9 RUP6A
R249 49.9 RDN6A

HSMC PORT A

HSMA_TX_D_P[16:0] HSMA_TX_D_P[16:0] 10,27
HSMA_TX_D_N[16:0] HSMA_TX_D_N[16:0] 10,27
HSMA_RX_D_P[16:0] HSMA_RX_D_P[16:0] 27
HSMA_RX_D_N[16:0] HSMA_RX_D_N[16:0] 27
HSMA_CLK_IN_P[2:1] HSMA_CLK_IN_P[2:1] 10,27
HSMA_CLK_IN_N[2:1] HSMA_CLK_IN_N[2:1] 10,27
HSMA_CLK_OUT_P[2:1] HSMA_CLK_OUT_P[2:1] 10,27
HSMA_CLK_OUT_N[2:1] HSMA_CLK_OUT_N[2:1] 10,27
HSMA_SDA HSMA_SDA 27
HSMA_SCL HSMA_SCL 27
HSMA_CLK_OUT0 HSMA_CLK_OUT0 27

HSMC PORT B

HSMB_TX_D_P[16:0] HSMB_TX_D_P[16:0] 27
HSMB_TX_D_N[16:0] HSMB_TX_D_N[16:0] 27
HSMB_RX_D_P[16:0] HSMB_RX_D_P[16:0] 27
HSMB_RX_D_N[16:0] HSMB_RX_D_N[16:0] 27
HSMB_CLK_OUT_P[2:1] HSMB_CLK_OUT_P[2:1] 10,27
HSMB_CLK_OUT_N[2:1] HSMB_CLK_OUT_N[2:1] 10,27
HSMB_CLK_IN_P[2:1] HSMB_CLK_IN_P[2:1] 10,27
HSMB_CLK_IN_N[2:1] HSMB_CLK_IN_N[2:1] 10,27
HSMB_D[3:0] HSMB_D[3:0] 27
HSMB_CLK_OUT0 HSMB_CLK_OUT0 27
HSMB_TX_LED HSMB_TX_LED 25

CPU RESET

CPU_RESETn CPU_RESETn 25

MAX INTERFACE

MAX_TO_STRATIX4 MAX_TO_STRATIX4 23
MAX_CLK MAX_CLK 23
FSM_A[26:0] FSM_A[26:0] 10,17,22,23

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Stratix IV E Banks 7 & 8

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Stratix IVE Bank 7

Bank 7A

QDRII_Q15	F6	DQ1T/DIFFOUT_T1P	DQ4T/DIFFOUT_T11P	A3	QDRII_Q0
QDRII_Q5	F8	DQ1T/DIFFOUT_T1N	DQ4T/DIFFOUT_T11N	A5	QDRII_Q3
QDRII_Q11	G8	DQ1T/DIFFOUT_T3P	DQ4T/DIFFIO_RX_T6P	B4	QDRII_Q1
QDRII_Q7	F9	DQ1T/DIFFOUT_T3N	DQ4T/DIFFIO_RX_T6N	A4	QDRII_Q2
QDRII_Q17	D6	DQ2T/DIFFOUT_T5P	DQ5T/DIFFOUT_T15P	D8	QDRII_A13
QDRII_Q4	C6	DQ2T/DIFFOUT_T5N	DQ5T/DIFFOUT_T15N	E10	QDRII_A11
QDRII_Q16	C5	DQ2T/DIFFIO_RX_T3P	DQ5T/DIFFIO_RX_T13P	E8	QDRII_A12
QDRII_Q14	B5	DQ2T/DIFFIO_RX_T3N	DQ5T/DIFFIO_RX_T13N	D7	QDRII_A8
RUP7A	F7	RUP7A/DQS1T/DIFFIO_RX_T1P	DQS4T/DIFFIO_RX_T5P	B2	QDRII_Q13
RDN7A	E7	RDN7A/DQSN1T/DIFFIO_RX_T1N	DQSN4T/DIFFIO_RX_T5N	A2	QDRII_QVLD
QDRII_CQ_N	C4	DQS2T/DIFFIO_RX_T2P	DQS5T/DIFFIO_RX_T7P	D9	QDRII_A10
QDRII_ODT	C3	DQSN2T/DIFFIO_RX_T2N	DQSN5T/DIFFIO_RX_T7N	C9	QDRII_A16
QDRII_Q8	G10	DQ3T/DIFFOUT_T9P	DQ6T/DIFFOUT_T17P	C7	QDRII_A5
QDRII_Q9	J12	DQ3T/DIFFOUT_T9N	DQ6T/DIFFOUT_T17N	A6	QDRII_A6
QDRII_Q6	G9	DQ3T/DIFFOUT_T7P	DQ6T/DIFFIO_RX_T9P	B8	QDRII_A9
QDRII_Q10	J11	DQ3T/DIFFOUT_T7N	DQ6T/DIFFIO_RX_T9N	A8	QDRII_A15
QDRII_CQ_P	H11	DQS3T/DIFFIO_RX_T4P	DQS6T/DIFFIO_RX_T8P	B7	QDRII_A14
QDRII_Q12	G11	DQSN3T/DIFFIO_RX_T4N	DQSN6T/DIFFIO_RX_T8N	A7	
QDRII_DOFFn	K12	DQS7T/DIFFIO_RX_T10P	DQ7T/DIFFOUT_T19P	L13	
	K11	DQSN7T/DIFFIO_RX_T10N	DQ7T/DIFFOUT_T19N	M13	

Bank 7B

QDRII_D4	E11	DQ9T/DIFFOUT_T27P	DQ11T/DIFFOUT_T31P	K13	QDRII_D11
QDRII_D13	G13	DQ9T/DIFFOUT_T27N	DQ11T/DIFFOUT_T31N	K14	QDRII_D12
QDRII_D15	F11	DQ9T/DIFFOUT_T25P	DQ11T/DIFFOUT_T33P	L14	QDRII_D9
QDRII_D17	G12	DQ9T/DIFFOUT_T25N	DQ11T/DIFFOUT_T33N	K15	QDRII_D10
QDRII_D14	D10	DQ10T/DIFFOUT_T29P	DQ12T/DIFFIO_RX_T18P	B11	QDRII_D2
QDRII_D8	D13	DQ10T/DIFFOUT_T29N	DQ12T/DIFFIO_RX_T18N	A11	QDRII_D3
QDRII_D7	D12	DQ10T/DIFFIO_RX_T15P	DQ12T/DIFFOUT_T35P	A9	QDRII_D0
QDRII_D6	C12	DQ10T/DIFFIO_RX_T15N	DQ12T/DIFFOUT_T35N	A12	QDRII_D5
QDRII_D16	F13	DQS9T/DIFFIO_RX_T13P	DQS11T/DIFFIO_RX_T16P	J14	QDRII_K_P
	F12	DQSN9T/DIFFIO_RX_T13N	DQSN11T/DIFFIO_RX_T16N	H14	QDRII_K_N
QDRII_BWSn1	D11	DQS10T/DIFFIO_RX_T14P	DQS12T/DIFFIO_RX_T17P	B10	QDRII_D1
QDRII_BWSn0	C11	DQSN10T/DIFFIO_RX_T14N	DQSN12T/DIFFIO_RX_T17N	A10	

Bank 7C

QDRII_A19	D15	DQ17T/DIFFOUT_T51P	DQ19T/DIFFOUT_T57P	E17	
QDRII_A17	F15	DQ17T/DIFFOUT_T51N	DQ19T/DIFFOUT_T57N	D17	QDRII_WPSn
QDRII_A20	E13	DQ17T/DIFFOUT_T49P	DQ19T/DIFFOUT_T55P	C15	
QDRII_A0	D14	DQ17T/DIFFOUT_T49N	DQ19T/DIFFOUT_T55N	C17	
QDRII_A4	C14	DQ18T/DIFFOUT_T53P		D16	
QDRII_A2	A15	DQ18T/DIFFOUT_T53N	DQS19T/DIFFIO_RX_T28P	C16	
QDRII_A21	B14	DQ18T/DIFFIO_RX_T27P	DQSN19T/DIFFIO_RX_T28N		
QDRII_A3	A14	DQ18T/DIFFIO_RX_T27N			
QDRII_A7	F14	DQS17T/DIFFIO_RX_T25P	DIFFIO_RX_T30P	H16	
QDRII_A1	E14	DQSN17T/DIFFIO_RX_T25N	DIFFIO_RX_T30N	G16	
QDRII_A18	B13	DQS18T/DIFFIO_RX_T26P	DIFFIO_RX_T29P	J15	
	A13	DQSN18T/DIFFIO_RX_T26N	DIFFIO_RX_T29N	J16	

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Stratix IVE Bank 8

Bank 8A

FSM_A0	F22	DQ33T/DIFFOUT_T112P	DQ36T/DIFFOUT_T120P	C29	FSM_A21
FSM_A1	H23	DQ33T/DIFFOUT_T112N	DQ36T/DIFFOUT_T120N	B29	FSM_A20
FSM_A2	G23	DQ33T/DIFFIO_RX_T56P	DQ36T/DIFFOUT_T122P	C31	FSM_A22
FSM_A3	F23	DQ33T/DIFFIO_RX_T56N	DQ36T/DIFFOUT_T122N	D31	FSM_A23
FSM_A7	F26	DQ34T/DIFFOUT_T116P	DQ37T/DIFFOUT_T124P	F27	FSM_A24
FSM_A5	D28	DQ34T/DIFFOUT_T116N	DQ37T/DIFFOUT_T124N	G27	FSM_D0
FSM_A6	F25	DQ34T/DIFFOUT_T114P	DQ37T/DIFFIO_RX_T62P	F28	FSM_D1
FSM_A4	D27	DQ34T/DIFFOUT_T114N	DQ37T/DIFFIO_RX_T62N	E28	FSM_D2
FSM_A8	G24	DQS33T/DIFFIO_RX_T57P	DQS36T/DIFFIO_RX_T61P	D30	FSM_D3
FSM_A9	F24	DQSN33T/DIFFIO_RX_T57N	DQSN36T/DIFFIO_RX_T61N	C30	FSM_D4
FSM_A10	E26	DQS34T/DIFFIO_RX_T58P	DQS37T/DIFFIO_RX_T63P	F29	FSM_D5
FSM_A11	D26	DQSN34T/DIFFIO_RX_T58N	DQSN37T/DIFFIO_RX_T63N	E29	FSM_D6
FSM_A12	A30	DQ35T/DIFFOUT_T118P		J25	FSM_D8
FSM_A13	A33	DQ35T/DIFFOUT_T118N	DQ38T/DIFFOUT_T128P	K25	FLASH_CEn
FSM_A14	B31	DQ35T/DIFFIO_RX_T59P	DQ38T/DIFFOUT_T128N	J24	FSM_D7
FSM_A15	A31	DQ35T/DIFFIO_RX_T59N	DQ38T/DIFFOUT_T126P	K24	FLASH_CLK
FSM_A16	B32		DQ38T/DIFFOUT_T126N	L22	FLASH_WEn
FSM_A17	A32	DQS35T/DIFFIO_RX_T60P	DQ32T/DIFFOUT_T110P	K23	FLASH_OEn
RUP8A	H26	DQSN35T/DIFFIO_RX_T60N	DQ32T/DIFFOUT_T110N	M23	FSM_A18
RDN8A	G26	RUP8A/DQS38T/DIFFIO_RX_T64P	DQS32T/DIFFIO_RX_T55P	L23	FSM_A19
		RDN8A/DQSN38T/DIFFIO_RX_T64N	DQSN32T/DIFFIO_RX_T55N		

Bank 8B

FSM_D9	A24	DQ27T/DIFFOUT_T94P	DQ29T/DIFFOUT_T100P	C24	FSM_D21
FSM_D10	A26	DQ27T/DIFFOUT_T94N	DQ29T/DIFFOUT_T100N	E25	FSM_D22
FSM_D11	B25	DQ27T/DIFFIO_RX_T47P	DQ29T/DIFFIO_RX_T50P	D25	FSM_D23
FSM_D12	A25	DQ27T/DIFFIO_RX_T47N	DQ29T/DIFFIO_RX_T50N	D24	FSM_D24
FSM_D15	K21	DQ28T/DIFFOUT_T98P	DQ30T/DIFFOUT_T104P	C28	FSM_D28
FSM_D16	K22	DQ28T/DIFFOUT_T98N	DQ30T/DIFFOUT_T104N	A29	FSM_D26
FSM_D14	K20	DQ28T/DIFFOUT_T96P	DQ30T/DIFFOUT_T102P	A27	FSM_D25
FSM_D13	J20	DQ28T/DIFFOUT_T96N	DQ30T/DIFFOUT_T102N	C27	FSM_D27
FSM_D17	C26	DQS27T/DIFFIO_RX_T48P	DQS29T/DIFFIO_RX_T51P	E23	FSM_D29
FSM_D18	B26	DQSN27T/DIFFIO_RX_T48N	DQSN29T/DIFFIO_RX_T51N	D23	FSM_D30
FSM_D19	J22	DQS28T/DIFFIO_RX_T49P	DQS30T/DIFFIO_RX_T52P	B28	FSM_D31
FSM_D20	J21	DQSN28T/DIFFIO_RX_T49N	DQSN30T/DIFFIO_RX_T52N	A28	USER_DIPSW0
USER_LED4	D19	DIFFIO_RX_T35P	DIFFIO_RX_T36P	F19	USER_LED6
USER_LED5	C19	DIFFIO_RX_T35N	DIFFIO_RX_T36N	E19	USER_LED7

Bank 8C

FLASH_RDYBSYn	C20	DQ20T/DIFFOUT_T72P	DQ22T/DIFFOUT_T78P	A22	SSRAM_OEn
FLASH_ADVn	D20	DQ20T/DIFFOUT_T72N	DQ22T/DIFFOUT_T78N	A21	SSRAM_CE1n
SSRAM_BWn0	D22	DQ20T/DIFFOUT_T74P	DQ22T/DIFFOUT_T80P	B22	SSRAM_BWEn
SSRAM_BWn1	E22	DQ20T/DIFFOUT_T74N	DQ22T/DIFFOUT_T80N	C23	USER_LED1
SSRAM_BWn2	E20	DQ21T/DIFFOUT_T76P			
SSRAM_BWn3	H20	DQ21T/DIFFOUT_T76N			
SSRAM_ADSCn	G20	DQ21T/DIFFIO_RX_T38P			
SSRAM_ADSPn	F20	DQ21T/DIFFIO_RX_T38N	RUP8C/DQS22T/DIFFIO_RX_T40P	B23	USER_LED2
SSRAM_ADVn	D21		RDN8C/DQSN22T/DIFFIO_RX_T40N	A23	USER_LED3
SSRAM_CLK	C21	DQS20T/DIFFIO_RX_T37P			
FLASH_RESETn	G21	DQSN20T/DIFFIO_RX_T37N			
USER_LED0	F21	DQS21T/DIFFIO_RX_T39P			
		DQSN21T/DIFFIO_RX_T39N			

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QDRII SRAM INTERFACE

QDRII_Q[17:0] — QDRII_Q[17:0] 19
QDRII_D[17:0] — QDRII_D[17:0] 19,21
QDRII_A[21:0] — QDRII_A[21:0] 19,21
QDRII_BWSn0 — QDRII_BWSn0 19,21
QDRII_BWSn1 — QDRII_BWSn1 19,21
QDRII_K_P — QDRII_K_P 19
QDRII_K_N — QDRII_K_N 19
QDRII_CQ_P — QDRII_CQ_P 19
QDRII_CQ_N — QDRII_CQ_N 19
QDRII_QVLD — QDRII_QVLD 19
QDRII_DOFFn — QDRII_DOFFn 19
QDRII_ODT — QDRII_ODT 19,21
QDRII_WPSn — QDRII_WPSn 19,21

SHARED BUS INTERFACE

FSM_D[31:0] — FSM_D[31:0] 22,23
FSM_A[26:0] — FSM_A[26:0] 10,16,22,23

SSRAM INTERFACE

SSRAM_BWn[3:0] — SSRAM_BWn[3:0] 22
SSRAM_OEn — SSRAM_OEn 22
SSRAM_BWEn — SSRAM_BWEn 22
SSRAM_ADVn — SSRAM_ADVn 22
SSRAM_ADSCn — SSRAM_ADSCn 22
SSRAM_ADSPn — SSRAM_ADSPn 22
SSRAM_CE1n — SSRAM_CE1n 22
SSRAM_CLK — SSRAM_CLK 22

USER INTERFACE

USER_LED[7:0] — USER_LED[7:0] 25
USER_DIPSW[7:0] — USER_DIPSW[7:0] 10,25

FLASH INTERFACE

FLASH_CLK — FLASH_CLK 22,23
FLASH_CEn — FLASH_CEn 22,23
FLASH_ADVn — FLASH_ADVn 22,23
FLASH_WEn — FLASH_WEn 22,23
FLASH_OEn — FLASH_OEn 22,23
FLASH_RESETn — FLASH_RESETn 22,23
FLASH_RDYBSYn — FLASH_RDYBSYn 22,23

1.5V_1.8V_B7
R237 49.9 RUP7A
R238 49.9 RDN7A

2.5V_B1_B8
R234 49.9 RUP8A
R233 49.9 RDN8A

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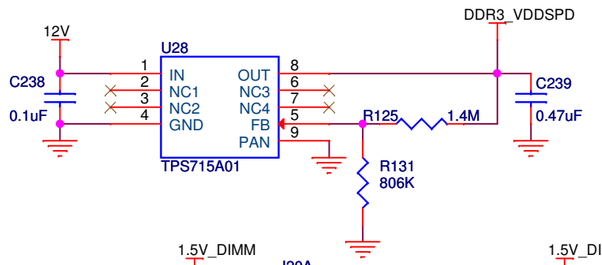
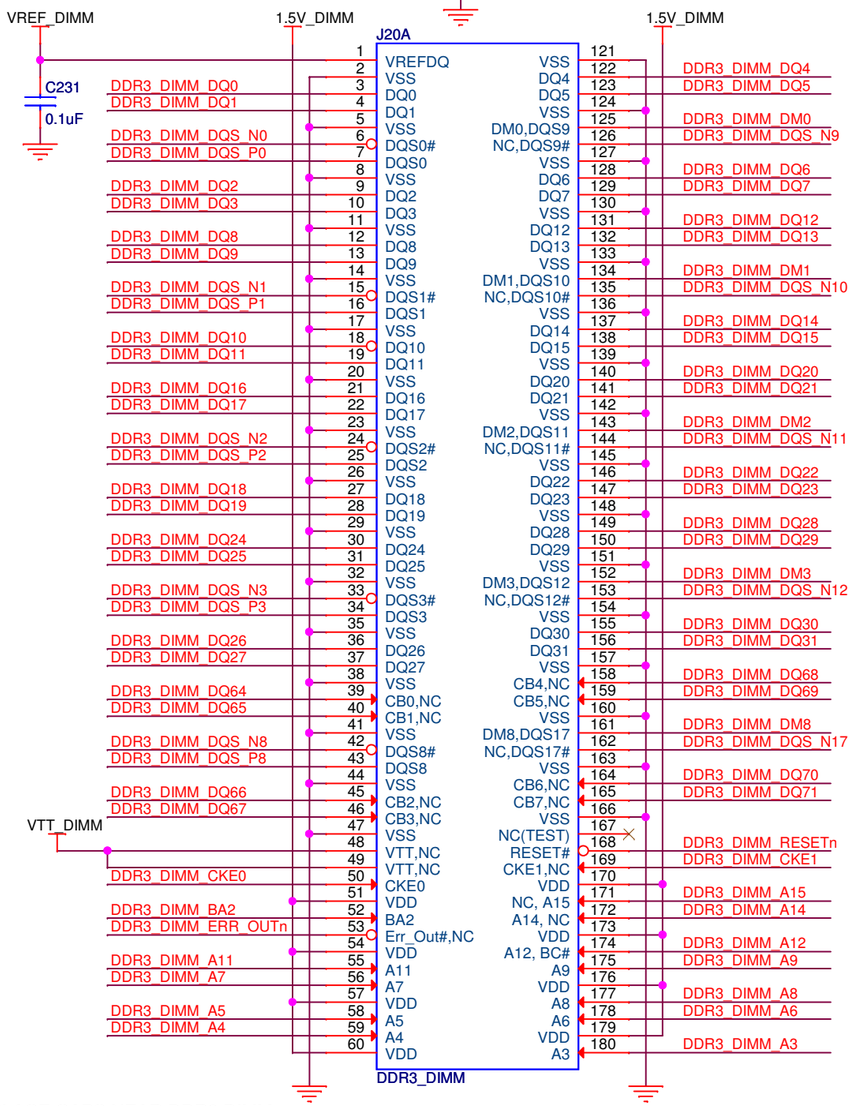
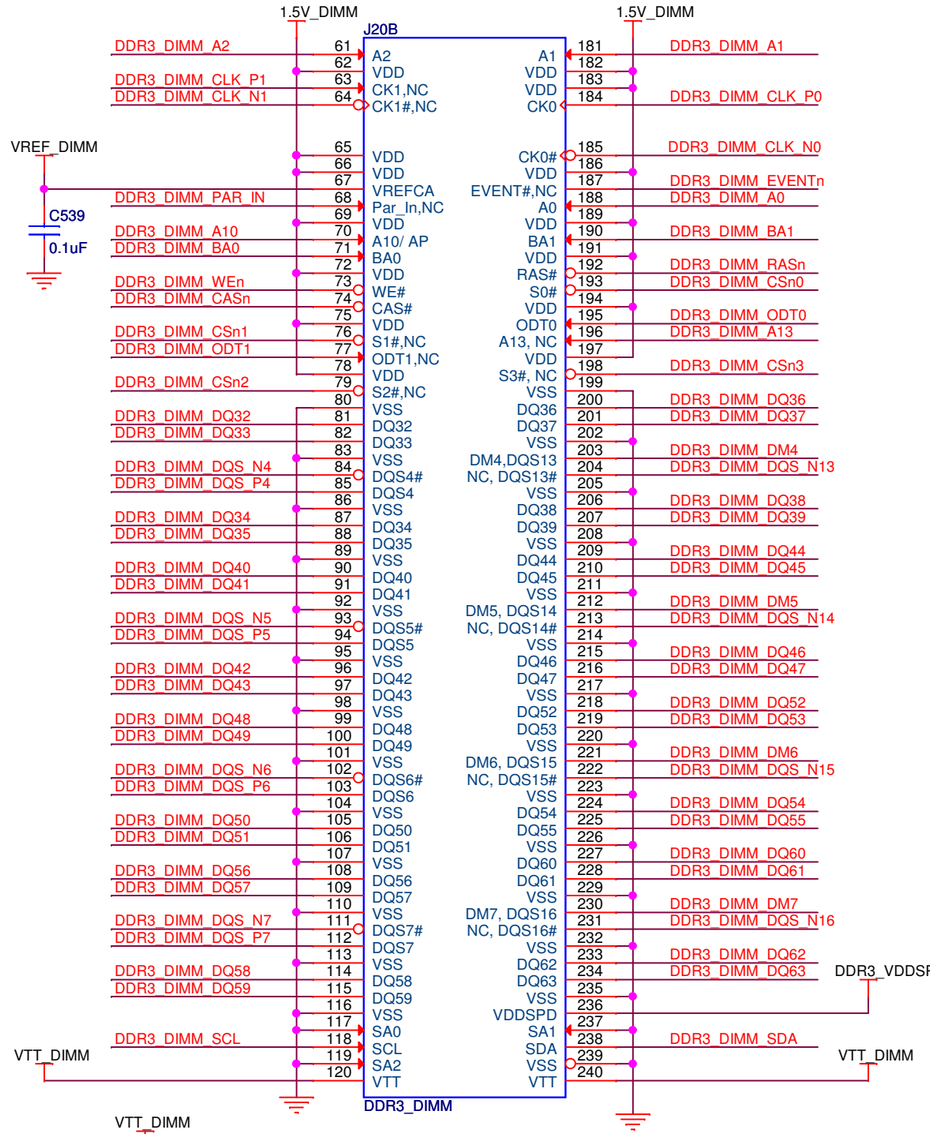
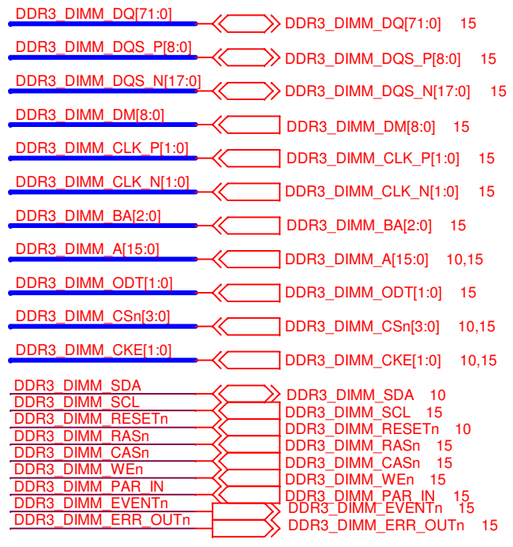
DDR3 SDRAM UDIMM (VIO)

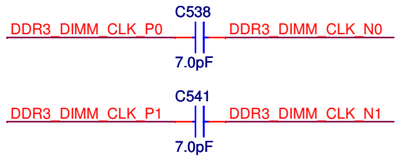


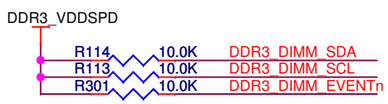




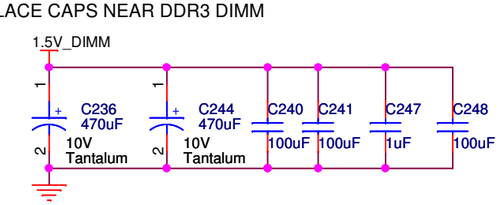
DDR3 DIMM on (VIO) INTERFACE

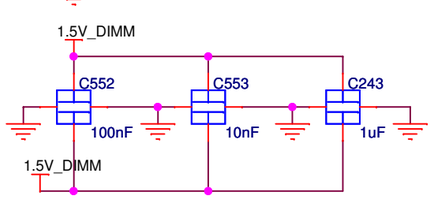


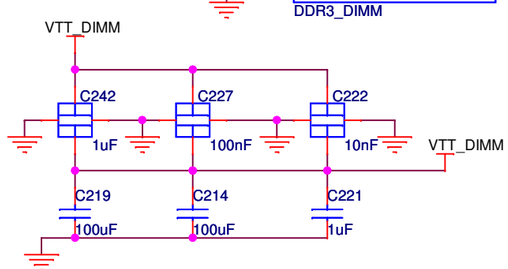




PLACE CAPS NEAR DDR3 DIMM







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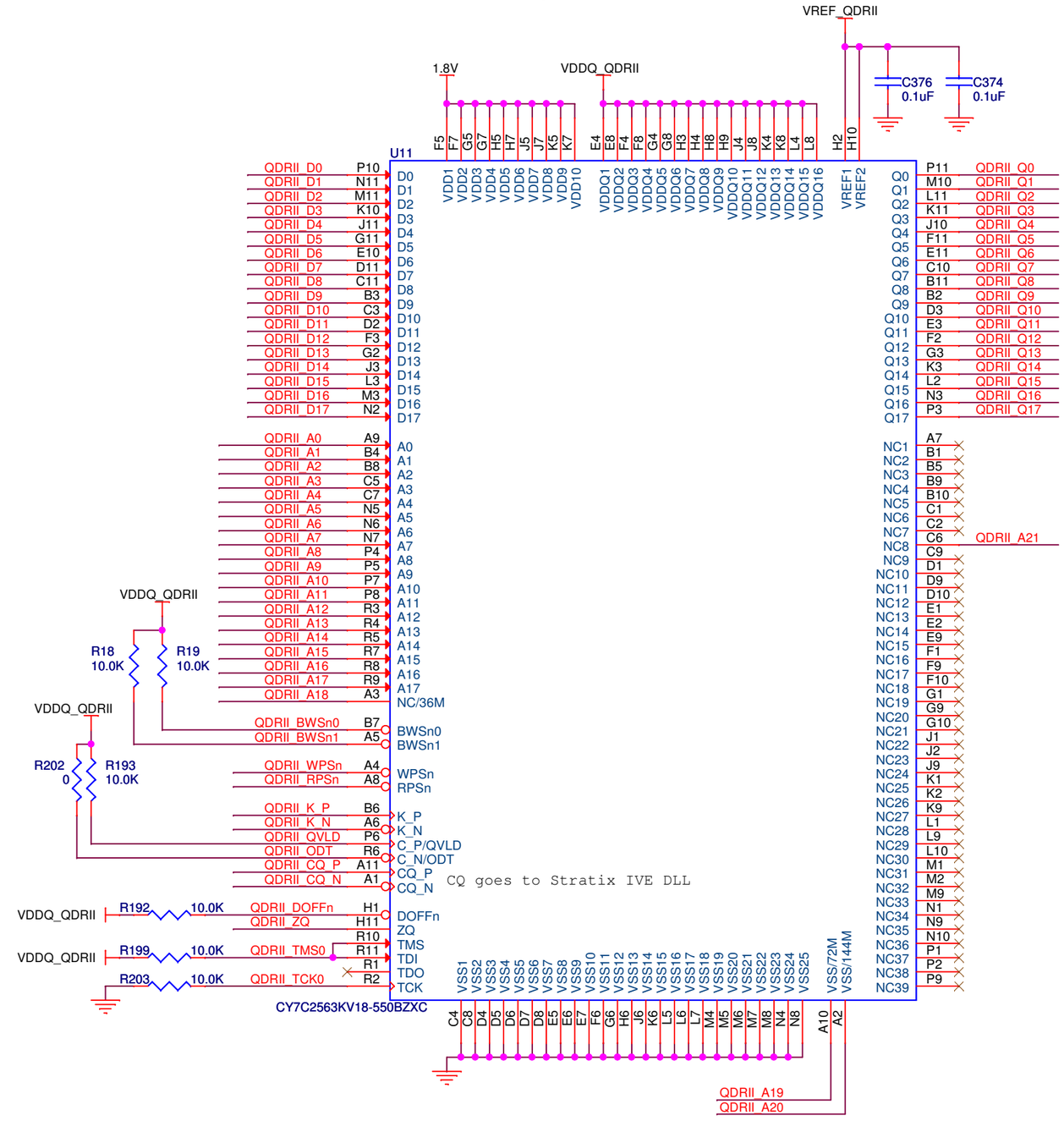
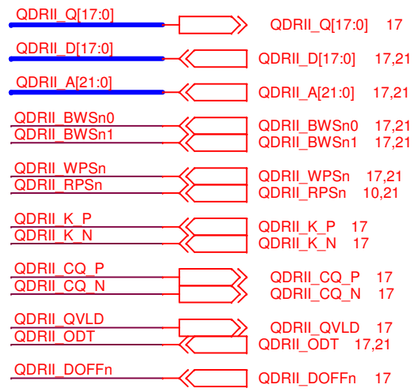
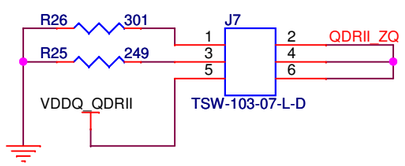
QDRII+ SRAM



QDRII+ SRAM INTERFACE



QDRII+ Output Impedance



Setting	Shunt J47
60 ohms	PIN1-PIN2
50 ohms	PIN3-PIN4
Min Drive	PIN5-PIN6

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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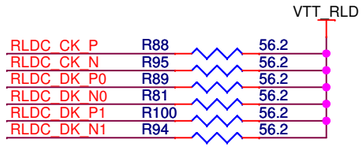
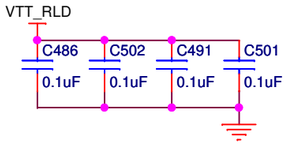
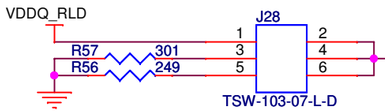
RLDRAM II, CIO



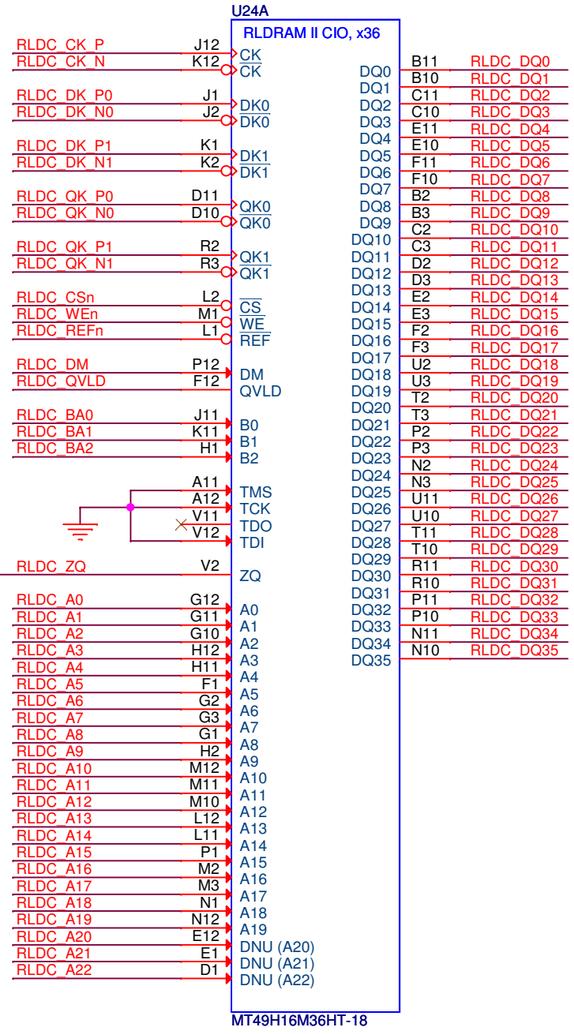
PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM II

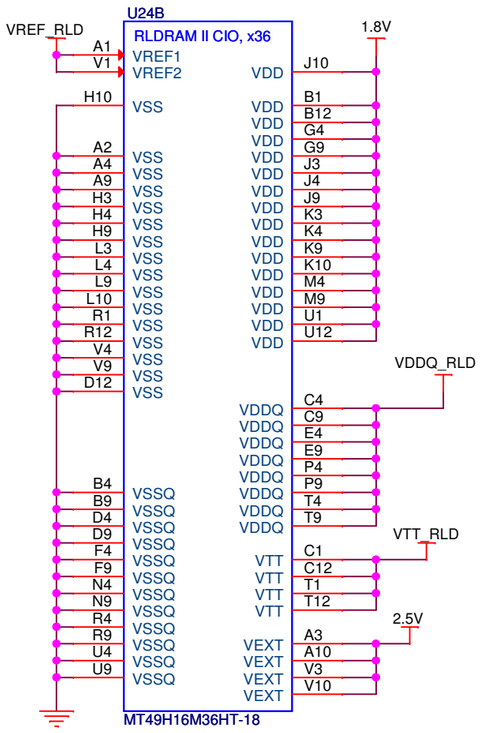




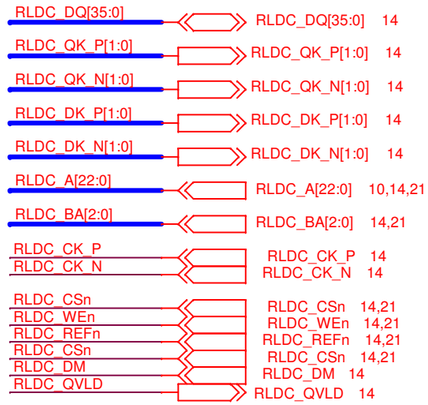
Output Impedence

Setting	Shunt Position
MAX Drive	PIN1-PIN2
60 Ohms	PIN3-PIN4
50 Ohms	PIN5-PIN6

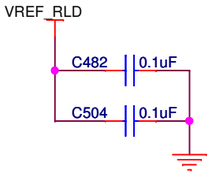




RLDRAM II INTERFACE

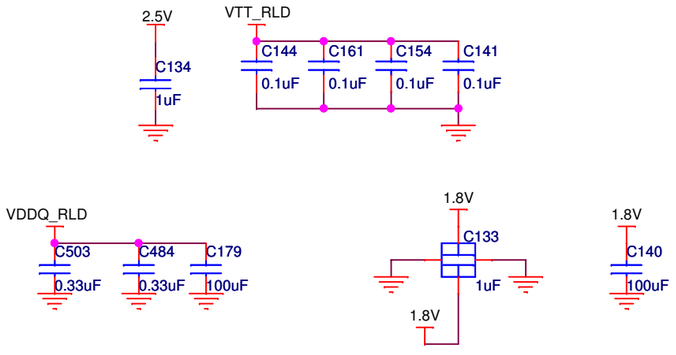


PLACE THESE CAPACITORS AS CLOSE AS POSSIBLE TO THE RLDRAM II



HSTL1

BYPASS CAPS FOR RLDRAM II CIO



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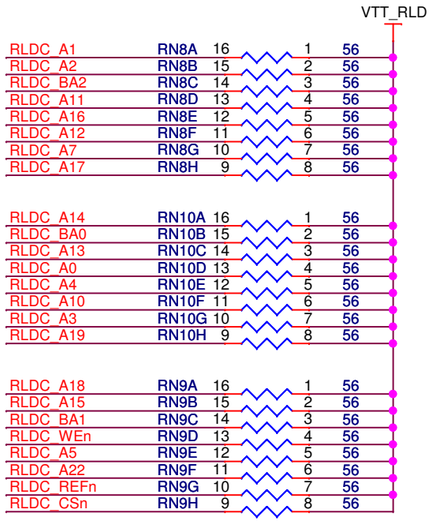
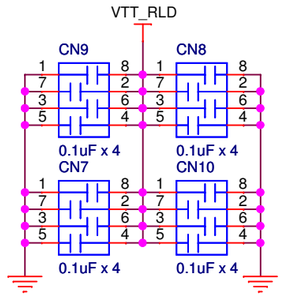
RLDRAM II and QDRII+ TERMINATIONS

Place Near RLDRAM II

On-die termination (ODT) is enabled by setting A9 to "1" during an MRS command.

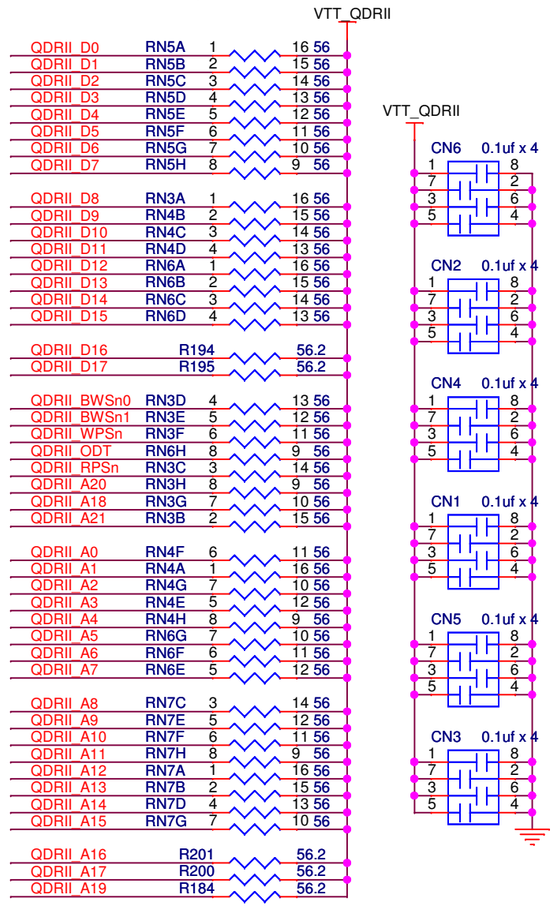
PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE RLDRAM II CIO

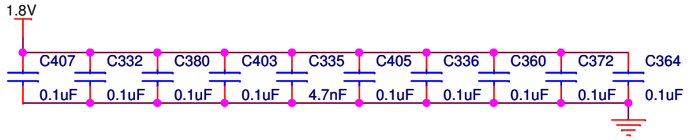


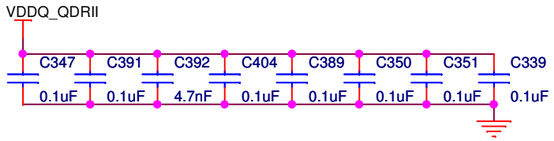


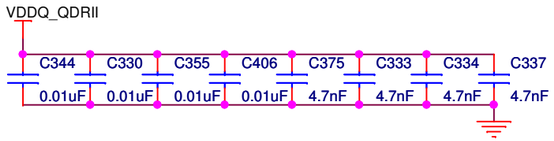
NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER PULL UP RESISTOR

Place Near QDRII+

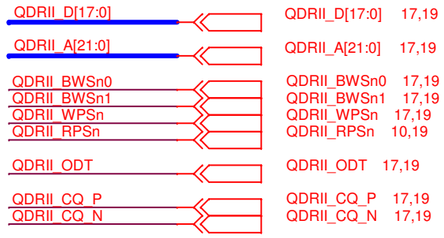




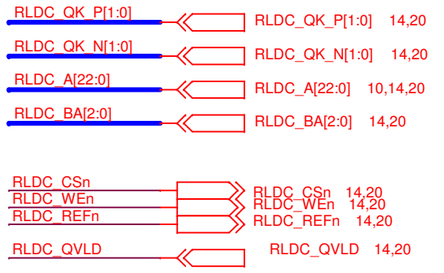




QDRII+ SRAM INTERFACE



RLDRAM II INTERFACE



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Title: Stratix IV E FPGA Development Kit Board

Size: B | Document Number: 150-0310904-B1 (6XX-41504R) | Rev: B

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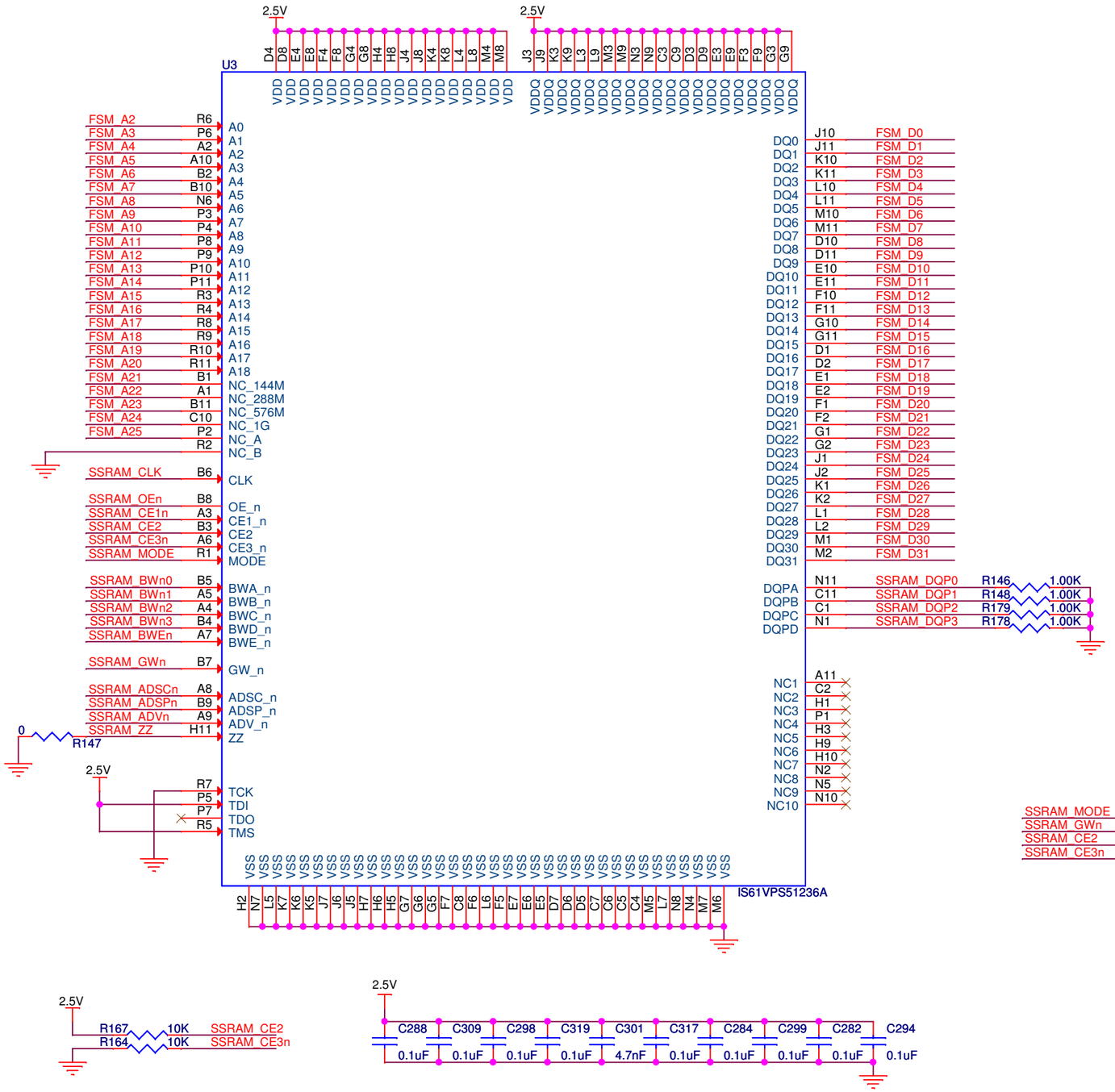
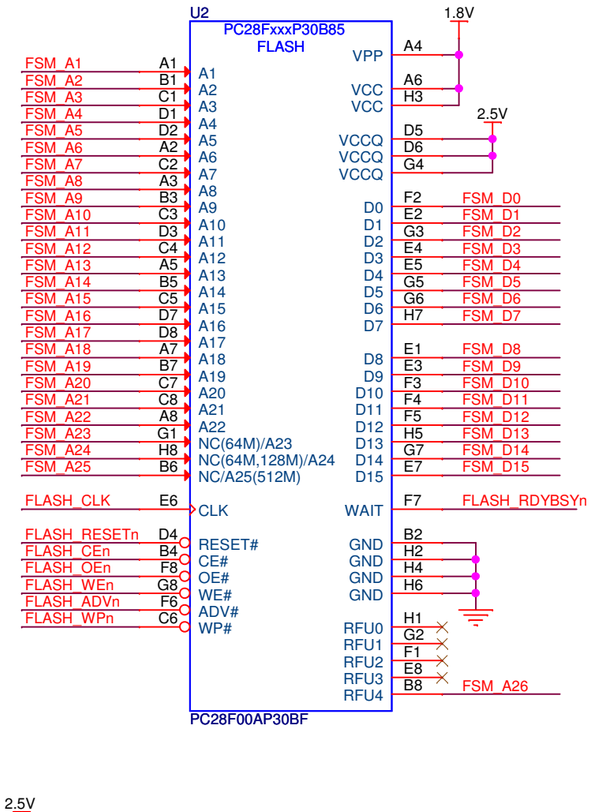
SSRAM & FLASH

SSRAM



FLASH 512Mb (32M X 16)



SHARED BUS

FSM_D[31:0] — FSM_D[31:0] 17,23

FSM_A[26:0] — FSM_A[26:0] 10,16,17,23

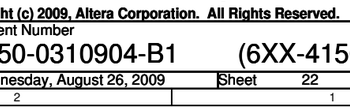
SSRAM INTERFACE

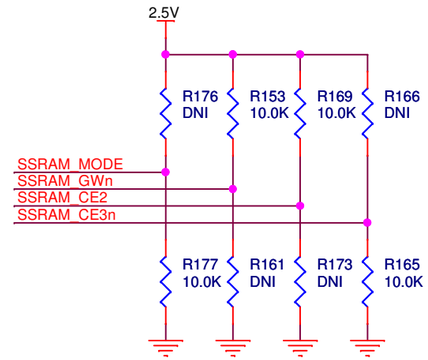
SSRAM_BWn[3:0] — SSRAM_BWn[3:0] 17

SSRAM_OEn — SSRAM_OEn 17
SSRAM_BWEn — SSRAM_BWEn 17
SSRAM_ADVn — SSRAM_ADVn 17
SSRAM_ADSCn — SSRAM_ADSCn 17
SSRAM_ADSPn — SSRAM_ADSPn 17
SSRAM_CE1n — SSRAM_CE1n 17
SSRAM_CLK — SSRAM_CLK 17
SSRAM_MODE — SSRAM_MODE 23
SSRAM_ZZ — SSRAM_ZZ 23
SSRAM_GWn — SSRAM_GWn 23

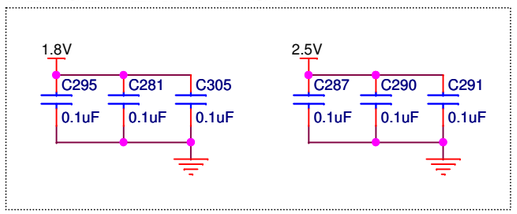
FLASH INTERFACE

FLASH_RESETn — FLASH_RESETn 17,23
FLASH_WEn — FLASH_WEn 17,23
FLASH_OEn — FLASH_OEn 17,23
FLASH_RDYBSYn — FLASH_RDYBSYn 17,23
FLASH_CEn — FLASH_CEn 17,23
FLASH_CLK — FLASH_CLK 17,23
FLASH_ADVn — FLASH_ADVn 17,23





PLACE NEAR FLASH



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Title: **Stratix IV E FPGA Development Kit Board**

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MAX II

U10A — MAX II BANK1

EPM2210_F256FBGA

FPGA_DATA0	D3	IOB1_1	IOB1_25	H3	CLK50_EN
FPGA_DCLK	C2	IOB1_2	IOB1_26	J1	CLK100_EN
FPGA_CONF_DONE	E3	IOB1_3	IOB1_27	H4	CLK66_EN
FPGA_STATUSn	C3	IOB1_4	IOB1_28	J2	CLK125_EN
FPGA_CONFIGn	E4	IOB1_5	IOB1_29	J4	MAX_PHASE_CLK0
	D2	IOB1_6	IOB1_30	K1	MAX_PHASE_CLK180
	E5	IOB1_7	IOB1_31	J3	
	D1	IOB1_8	IOB1_32	K2	
SENSE_SDO	F3	IOB1_9			
SENSE_ADC_F0	E2	IOB1_10	IOB1_34	L1	FPGA_DATA1
SENSE_SDI	F4	IOB1_11	IOB1_35	K5	FPGA_DATA2
SENSE_SCK	E1	IOB1_12	IOB1_36	L2	FPGA_DATA3
SENSE_CS0n	F5	IOB1_13	IOB1_37	K4	FPGA_DATA4
SENSE_CS1n	F2	IOB1_14	IOB1_38	M1	FPGA_DATA5
	F6	IOB1_15	IOB1_39	K3	FPGA_DATA6
	F1	IOB1_16	IOB1_40	M2	FPGA_DATA7
	G3			L5	
	G2	IOB1_17	IOB1_41	M3	
	G4	IOB1_18	IOB1_42	L4	
	G1	IOB1_19	IOB1_43	N1	TSENSE_SMB_DATA
	G5	IOB1_20	IOB1_44	L3	TSENSE_SMB_CLK
	H2	IOB1_21	IOB1_45	N2	MAX_DIP3
		IOB1_22	IOB1_46	M4	OVERTEMP
			IOB1_47	N3	
MAX_TO_STRATIX4	H1	IOB1_24	IOB1_48		
			IOB1_49	P2	
MAX_CLK	H5			P3	JTAG_TCK
TSENSE_ALERTn	J5	IOB1/GCLK0	TCK	L6	JTAG_FPGA_TDO
		IOB1/GCLK1	TDI	M5	JTAG_EPM2210_TDO
			TDO	N4	JTAG_TMS
			TMS		

U10B — MAX II BANK2

EPM2210_F256FBGA

PHASE0	C13	IOB2_50	IOB2_74	E9	2.5V_FPGA_PG
PHASE90	B16	IOB2_51	IOB2_75	A9	VDDQ_QDRII_PG
PHASE180	C12	IOB2_52	IOB2_76	A8	1.8V_PG
PHASE270	A15	IOB2_53	IOB2_77	B8	
	D12	IOB2_54	IOB2_78	E8	3.3V_PG
	B14	IOB2_55	IOB2_79	A7	2.5V_HSMC_PG
	C11	IOB2_56	IOB2_80	D8	
	B13	IOB2_57	IOB2_81	B7	
SSRAM_MODE	D11			C8	
SSRAM_ZZ	A13	IOB2_58	IOB2_82	A6	
SSRAM_GWn	E11	IOB2_59	IOB2_83		
	B12	IOB2_60		B6	
	C10	IOB2_61	IOB2_85	E7	OVERTEMPn
	A12	IOB2_62	IOB2_86	A5	
	D10	IOB2_63	IOB2_87	D7	
	B11	IOB2_64	IOB2_88	B5	
		IOB2_65	IOB2_89		
	E10			C7	
	A11	IOB2_66	IOB2_90	A4	
		IOB2_67	IOB2_91	E6	
			IOB2_92	B4	
	B10		IOB2_93	D6	
	C9	IOB2_69	IOB2_94	C4	
FACTORY_CONFIGn	A10	IOB2_70	IOB2_95	C6	
	D9	IOB2_71	IOB2_96	B3	
	B9	IOB2_72	IOB2_97		
		IOB2_73		C5	
			IOB2_98	A2	
			IOB2_99	D5	
			IOB2_100	B1	
			IOB2_101	D4	MAX_PB
			IOB2_102		

MAX_PB is labeled as "USER_1/USER_2" on the board

U10C — MAX II BANK3

EPM2210_F256FBGA

FSM_D18	P14	IOB3_103	IOB3_127	J16	FSM_A26
PGM0	N13	IOB3_104	IOB3_128	J13	
PGM1	P15	IOB3_105	IOB3_129	H16	
PGM2	M14	IOB3_106	IOB3_130	H13	
MAX_DIP4	N14	IOB3_107	IOB3_131	H15	MAX_ERROR
MAX_DIP5	M13	IOB3_108	IOB3_132	H14	MAX_LOAD
MAX_DIP6	N15	IOB3_109	IOB3_133	G16	MAX_FACTORY
CLK66_SEL	L14	IOB3_110	IOB3_134	G12	MAX_USER
PGM3	N16			G15	
FLASH_ADVn	L13	IOB3_111	IOB3_135		
FLASH_RESETn	M15	IOB3_112		F16	HSMA_PSNTn
FLASH_WEn	L12	IOB3_113	IOB3_137	G13	HSMB_PSNTn
FLASH_OEn	M16	IOB3_114	IOB3_138	F15	
FLASH_RDYBSYn	L11	IOB3_115	IOB3_139	G14	
FLASH_CLK	L15	IOB3_116	IOB3_140	E16	
FLASH_CEn	K14	IOB3_117	IOB3_141	F11	
		IOB3_118	IOB3_142		
MAX_CSn	L16			E15	MAX_EMB
MAX_OEn	K13	IOB3_119	IOB3_143	F12	FSM_D24
MAX_WEn	K15	IOB3_120	IOB3_144	D16	FSM_D25
	K12	IOB3_121	IOB3_145	F13	FSM_D26
MAX_DIP2	K16	IOB3_122	IOB3_146	D15	FSM_D27
		IOB3_123	IOB3_147	F14	FSM_D28
			IOB3_148	D14	FSM_D29
	J15	IOB3_125	IOB3_149	E12	FSM_D30
	J14	IOB3_126	IOB3_150		
			IOB3_151	C15	FSM_D31
			IOB3_152	E13	FSM_A25
			IOB3_153	C14	
CLKIN_50	J12	IOB3/GLCK2	IOB3_154	E14	MAX_DIP0
CLKIN_MAX_100	H12	IOB3/GCLK3	IOB3_155	D13	MAX_DIP1

MAX_EMB is labeled as "USER_1" on the board

U10D — MAX II BANK4

EPM2210_F256FBGA

FSM_D0	P4	IOB4_156	IOB4_180	N9	FSM_A0
FSM_D1	R1	IOB4_157	IOB4_181	T8	FSM_A1
FSM_D2	P5	IOB4_158	IOB4_182	T9	FSM_A2
FSM_D3	T2	IOB4_159	IOB4_183	R9	FSM_A3
FSM_D4	N5	IOB4_160	IOB4_184	P9	FSM_A4
FSM_D5	R3	IOB4_161	IOB4_185	T10	FSM_A5
FSM_D6	P6	IOB4_162			
FSM_D7	R4	IOB4_163	IOB4_187	R10	FSM_A7
FSM_D8	N6			M10	FSM_A8
FSM_D9	T4	IOB4_164	IOB4_188	T11	FSM_A9
FSM_D10	M6	IOB4_165	IOB4_189	N10	FSM_A10
FSM_D11	R5	IOB4_166	IOB4_190	R11	FSM_A11
FSM_D12	P7	IOB4_167	IOB4_191	P10	FSM_A12
FSM_D13	T5	IOB4_168	IOB4_192	T12	FSM_A13
FSM_D14	N7	IOB4_169	IOB4_193	M11	FSM_A14
FSM_D15	R6	IOB4_170	IOB4_194	R12	FSM_A15
		IOB4_171	IOB4_195		
FSM_D16	M7			N11	FSM_A16
FSM_D17	T6	IOB4_172	IOB4_196	T13	FSM_A17
		IOB4_173	IOB4_197	P11	FSM_A18
			IOB4_198	R13	FSM_A19
FSM_D19	R7	IOB4_175	IOB4_199	M12	FSM_A20
FSM_D20	P8	IOB4_176	IOB4_200	R14	FSM_A21
FSM_D21	T7	IOB4_177	IOB4_201	N12	FSM_A22
FSM_D22	N8	IOB4_178	IOB4_202	T15	FSM_A23
FSM_D23	R8	IOB4_179	IOB4_203		
			IOB4_204	P12	FSM_A24
SYS_RESETn	M9	IOB4/DEV_CLRn	IOB4_205	R16	RESET_CONFIGn
	M8	IOB4/DEV_OE	IOB4_206	P13	FSM_A6

U10E — MAX II Power

EPM2210_F256FBGA

	H7	GNDINT	VCCINT	H8	
	H9	GNDINT	VCCINT	H10	
	J8	GNDINT	VCCINT	J7	
	J10	GNDINT	VCCINT	J9	
	G6	GNDINT	VCCINT	K6	
	F7	GNDINT	VCCINT	L7	
	K11	GNDINT	VCCINT	G11	
	L10	GNDINT	VCCINT	F10	
	A1	GNDIO	VCCIO1	C1	
	A16	GNDIO	VCCIO1	H6	
	B2	GNDIO	VCCIO1	J6	
	B15	GNDIO	VCCIO1	P1	
	G7	GNDIO			
	G8	GNDIO	VCCIO2	A3	
	G9	GNDIO	VCCIO2	A14	
	G10	GNDIO	VCCIO2	F8	
	K7	GNDIO	VCCIO2	F9	
	K8	GNDIO			
	K9	GNDIO	VCCIO3	C16	
	K10	GNDIO	VCCIO3	H11	
	R2	GNDIO	VCCIO3	J11	
	R15	GNDIO	VCCIO3	P16	
	T1	GNDIO			
	T16	GNDIO	VCCIO4	L8	
			VCCIO4	L9	
			VCCIO4	T3	
			VCCIO4	T14	

2.5V

Y2 — 100MHz

R191 1.00K

C366 0.01uF

L7 DNI

C358 0.01uF

C361 4.7uF

CLKIN_MAX_100

CLOCK INTERFACE

CLK50_EN	CLK50_EN 11
CLK66_SEL	CLK66_SEL 11,25
CLK66_EN	CLK66_EN 11
CLK125_EN	CLK125_EN 11
CLK100_EN	CLK100_EN 11
CLKIN_50	CLKIN_50 10,11
MAX_CLK	MAX_CLK 16
PHASE0	PHASE0 5
PHASE90	PHASE90 3,5
PHASE180	PHASE180 5
PHASE270	PHASE270 3,5
MAX_PHASE_CLK0	MAX_PHASE_CLK0 6
MAX_PHASE_CLK180	MAX_PHASE_CLK180 7

SHARED BUS

FSM_D[31:0]	FSM_D[31:0] 17,22
FSM_A[26:0]	FSM_A[26:0] 10,16,17,22

FLASH INTERFACE

FLASH_RESETn	FLASH_RESETn 17,22
FLASH_WEn	FLASH_WEn 17,22
FLASH_OEn	FLASH_OEn 17,22
FLASH_RDYBSYn	FLASH_RDYBSYn 17,22
FLASH_CLK	FLASH_CLK 17,22
FLASH_CEn	FLASH_CEn 17,22
FLASH_ADVn	FLASH_ADVn 17,22
SSRAM_ZZ	SSRAM_ZZ 22
SSRAM_GWn	SSRAM_GWn 22
SSRAM_MODE	SSRAM_MODE 22

CONFIGURATION INTERFACE

JTAG_TCK	JTAG_TCK 12,13,27
JTAG_TMS	JTAG_TMS 12,13,27
JTAG_EPM2210_TDO	JTAG_EPM2210_TDO 12
JTAG_FPGA_TDO	JTAG_FPGA_TDO 12
FPGA_DATA[7:0]	FPGA_DATA[7:0] 12
FPGA_DCLK	FPGA_DCLK 12
FPGA_CONF_DONE	FPGA_CONF_DONE 12,25
FPGA_STATUSn	FPGA_STATUSn 12,13
FPGA_CONFIGn	FPGA_CONFIGn 12
HSMA_PSNTn	HSMA_PSNTn 27
HSMB_PSNTn	HSMB_PSNTn 27

CURRENT SENSE

SENSE_SDO	SENSE_SDO 8
SENSE_ADC_F0	SENSE_ADC_F0 8
SENSE_SDI	SENSE_SDI 8
SENSE_SCK	SENSE_SCK 8
SENSE_CS0n	SENSE_CS0n 8
SENSE_CS1n	SENSE_CS1n 8

FPGA OSCILLATOR CONTROL

TSENSE_ALERTn	TSENSE_ALERTn 8
OVERTEMPn	OVERTEMPn 8
OVERTEMP	OVERTEMP 8
MAX_TO_STRATIX4	MAX_TO_STRATIX4 16
TSENSE_SMB_DATA	TSENSE_SMB_DATA 8
TSENSE_SMB_CLK	TSENSE_SMB_CLK 8

USER I/O's

PGM[3:0]	PGM[3:0] 25
MAX_DIP[6:0]	MAX_DIP[6:0] 25
RESET_CONFIGn	RESET_CONFIGn 25
FACTORY_CONFIGn	FACTORY_CONFIGn 25
MAX_CSn	MAX_CSn 14
MAX_OEn	MAX_OEn 14
MAX_WEn	MAX_WEn 14
MAX_ERROR	MAX_ERROR 25
MAX_LOAD	MAX_LOAD 25
MAX_FACTORY	MAX_FACTORY 25
MAX_USER	MAX_USER 25
MAX_EMB	MAX_EMB 25
MAX_PB	MAX_PB 25
2.5V_HSMC_PG	2.5V_HSMC_PG 4
SYS_RESETn	SYS_RESETn 12,25
2.5V_FPGA_PG	2.5V_FPGA_PG 4
VDDQ_QDRII_PG	VDDQ_QDRII_PG 4
1.8V_PG	1.8V_PG 7
3.3V_PG	3.3V_PG 3

Place near MAX II

2.5V

C321 C324 C338 C370 C371 C323 C322 C362 C377 C357 C346 C384 — 0.1uF

2.5V

C387 C348 C396 C368 C399 C378 C367 C385 — 0.1uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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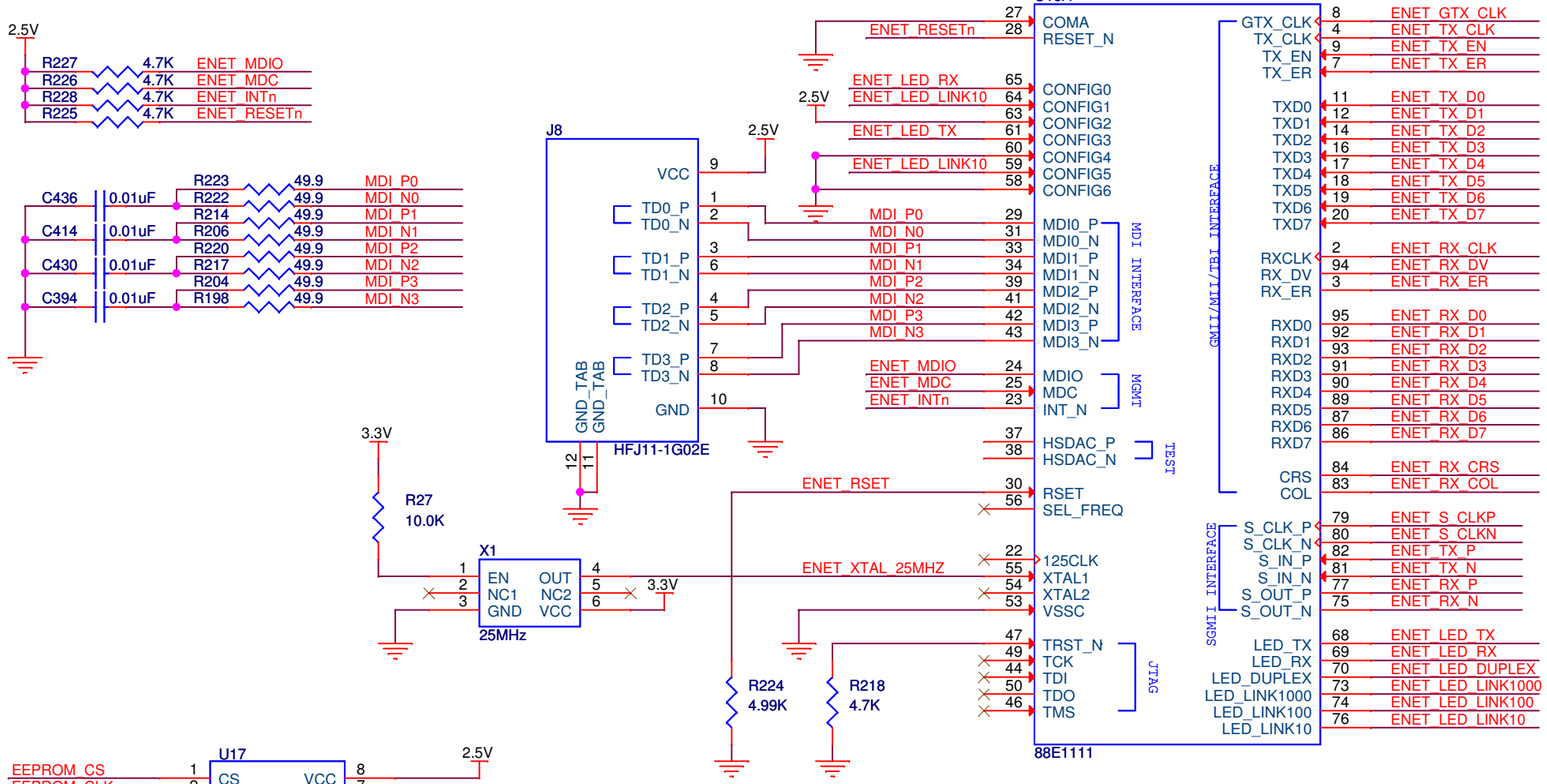
10/100/1000 Ethernet

SGMII Mode (default)



ETHERNET INTERFACE

ENET_TX_D[7..0] — ENET_TX_D[7..0] 10,14

ENET_GTX_CLK — ENET_GTX_CLK 14
ENET_TX_CLK — ENET_TX_CLK 14
ENET_TX_ER — ENET_TX_ER 14
ENET_TX_EN — ENET_TX_EN 14
ENET_MDC — ENET_MDC 14

ENET_RX_D[7..0] — ENET_RX_D[7..0] 14

ENET_RX_DV — ENET_RX_DV 14
ENET_MDIO — ENET_MDIO 14
ENET_RESETn — ENET_RESETn 14
ENET_RX_ER — ENET_RX_ER 14
ENET_RX_CRS — ENET_RX_CRS 14
ENET_RX_COL — ENET_RX_COL 14
ENET_RX_CLK — ENET_RX_CLK 14

ENET_INTn — ENET_INTn 14

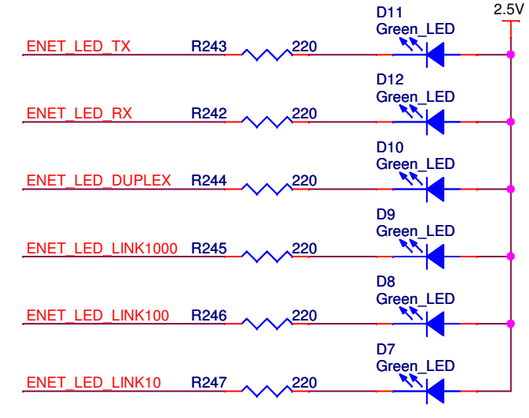
ENET_LED_LINK1000 — ENET_LED_LINK1000 14

ETHERNET SGMII INTERFACE

ENET_TX_P — ENET_TX_P 10
ENET_TX_N — ENET_TX_N 10

ENET_RX_P — ENET_RX_P 14
ENET_RX_N — ENET_RX_N 14
ENET_S_CLKP — ENET_S_CLKP 10
ENET_S_CLKN — ENET_S_CLKN 10

EEPROM_CS — EEPROM_CS 14
EEPROM_CLK — EEPROM_CLK 14
EEPROM_DIN — EEPROM_DIN 14
EEPROM_DOUT — EEPROM_DOUT 14



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Stratix IV E FPGA Development Kit Board

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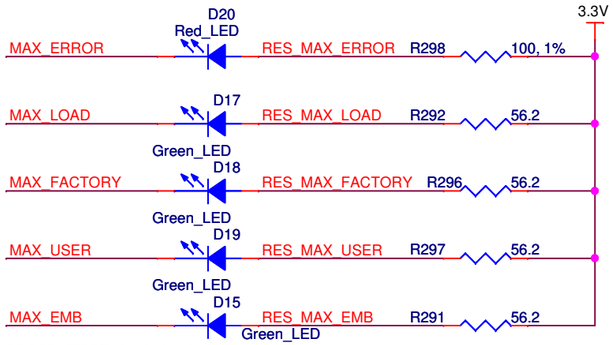
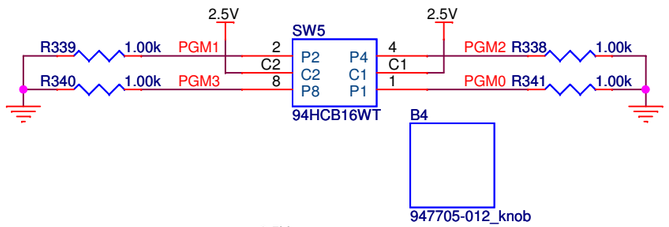
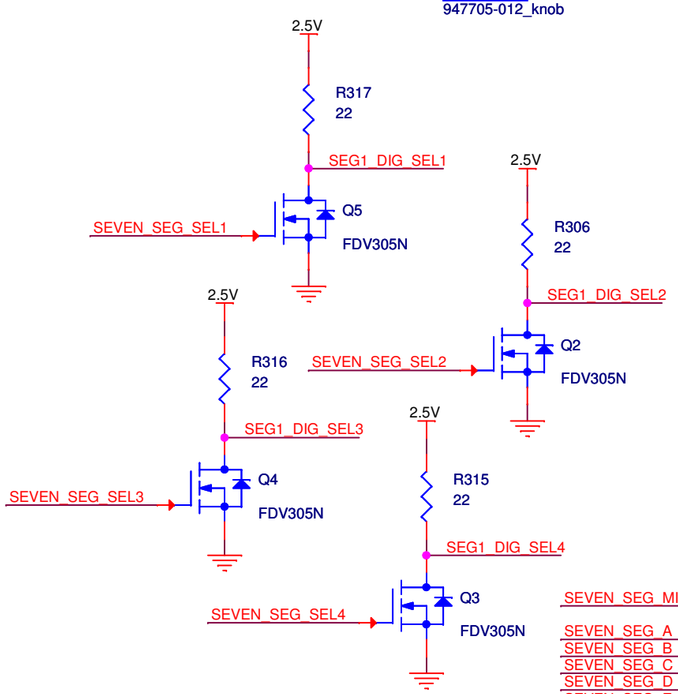
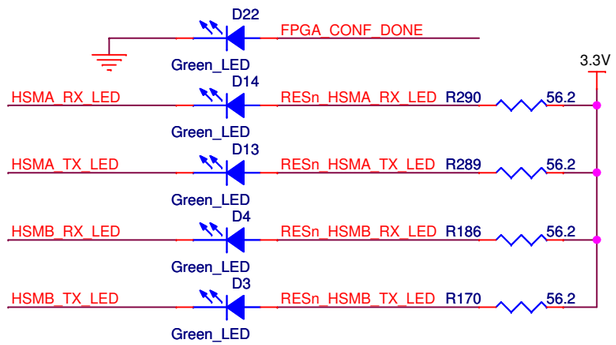
User IO & Connector

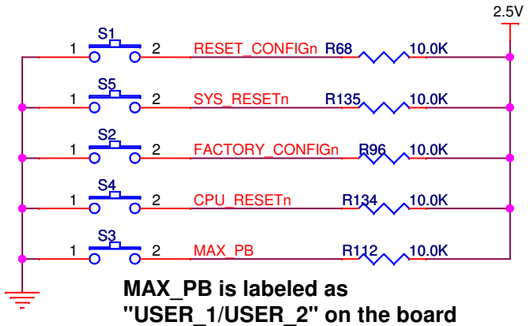


MAX_EMB is labeled as "USER_1" on the board

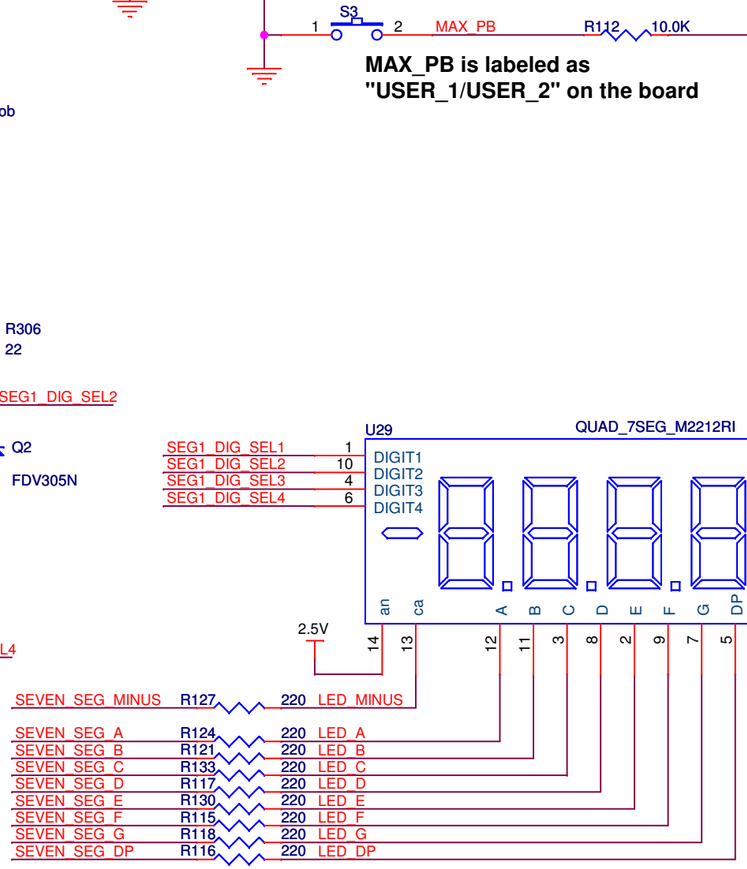


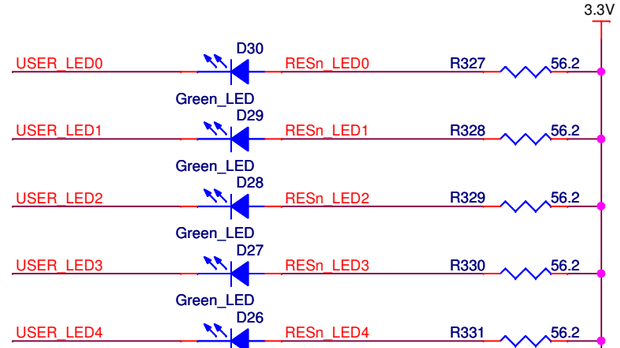


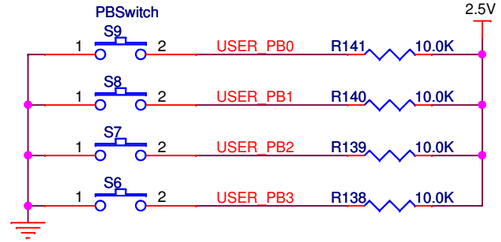


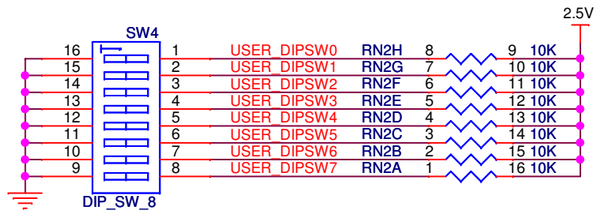


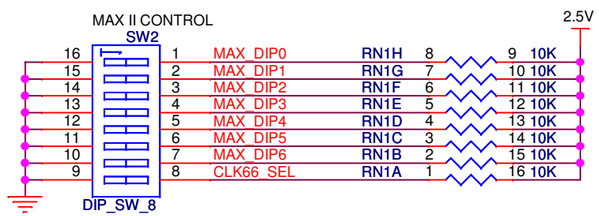
MAX_PB is labeled as "USER_1/USER_2" on the board



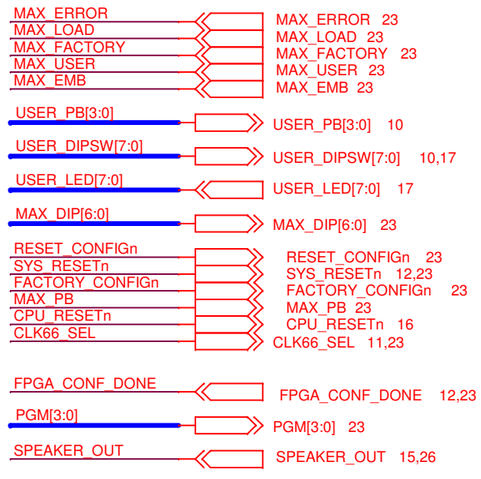




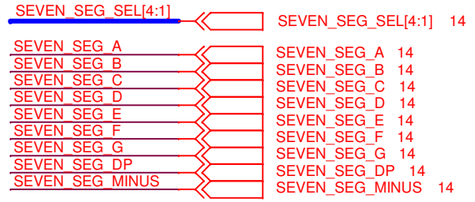




USER I/O's



SEVEN-SEG INTERFACE



HSMC INTERFACE

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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Speaker, LCD & Display Connectors

B5
2x7 HDR

B6
LCM-S01602DSR/C

SPACER5
MSPM-7-01
SPACER6
MSPM-7-01

PLACE NEAR FPC/FFC CONNECTOR

2.5V
C68 0.1uF
C67 0.01uF
12V
C292 0.1uF
C297 10uF 25V Tantalum

B3
128x64 LCD

SPACER1 MSPM-3-01
SPACER3 MSPM-3-01
SPACER2 MSPM-3-01
SPACER4 MSPM-3-01

1.00k R211

J27
LCD1_CSn 1
LCD1_RSTn 2
LCD1_D_Cn 3
LCD1_WEn 4
LCD1_E_RDn 5
LCD1_DATA0 6
LCD1_DATA1 7
LCD1_DATA2 8
LCD1_DATA3 9
LCD1_DATA4 10
LCD1_DATA5 11
LCD1_DATA6 12
LCD1_DATA7 13
2.5V
V5
V1
V2
V3
V4
V5
LCD1_BS1
LCD1_SERn
R212 10.0K
2.5V
FPC_FFC_30PIN

2x16 LED DISPLAY INTERFACE

LCD_DATA[7:0] — LCD_DATA[7:0] 15
LCD_CSn — LCD_CSn 15
LCD_D_Cn — LCD_D_Cn 15
LCD_WEn — LCD_WEn 15

128x64 LCD DISPLAY INTERFACE

LCD1_DATA[7:0] — LCD1_DATA[7:0] 14
LCD1_SERn — LCD1_SERn 14
LCD1_CSn — LCD1_CSn 14
LCD1_RSTn — LCD1_RSTn 15
LCD1_D_Cn — LCD1_D_Cn 14
LCD1_WEn — LCD1_WEn 14
LCD1_E_RDn — LCD1_E_RDn 14
LCD1_BS1 — LCD1_BS1 14

SPEAKER_OUT — SPEAKER_OUT 15

2 x 16 Display Connector

5.0V
J23
LCD_WEn
LCD_DATA0
LCD_DATA2
LCD_DATA4
LCD_DATA6
LCD_D_Cn
LCD_CSn
LCD_DATA1
LCD_DATA3
LCD_DATA5
LCD_DATA7
HDR2X7

12V

Short 12V to old -12V rail for new positive bias voltage LCD

L6 DNI
C276 DNI
L5 DNI
+12SW
-12SW
C289 10uF
U34
VIN SW1
GND
SHDN NFB
DNI
DNI D34
-12FB
R152 80.6K
C293 10uF
R155 10.0K

R154 8.06K
9.3V V5
C415 1uF
R207 DNI
R1001 3.01K
1.0V V4
C418 1uF
R208 3.32K
2.1V V3
C419 1uF
R209 15.4K
7.3V V2
C420 1uF
R210 2.94K
8.3V V1
C421 1uF
R213 DNI
2.5V

R1000 2.94K

Above power circuit was reworked to support a new graphics LCD with +12V bias voltages, not the original -12V voltages.
FOR USE WITH NEW LCDF-55472 Series ONLY (old -12V circuit for use only with F-51852 Series ONLY)

R1 100
RED
BLACK
J25
HDR2x1

Graphics LCD Backlight Power Header (Hook black wire to pin 2)

2.5V
C13 1.0uF
C11 1.0uF
U1
SHUTDOWN
BYPASS
IN+
IN-
VDD
VO2
VO1
GND
LM4990
SP_INp
SP_INn
SPEAKER_OUT
R10 100, 1%
SPEAKER
C17 0.22uF
R5 20.0K
C18 0.1uF
R7 20.0K
2.5V
R3 0
R8 0
R4 DNI
R9 DNI
HDR4X1
J1

ALTERA

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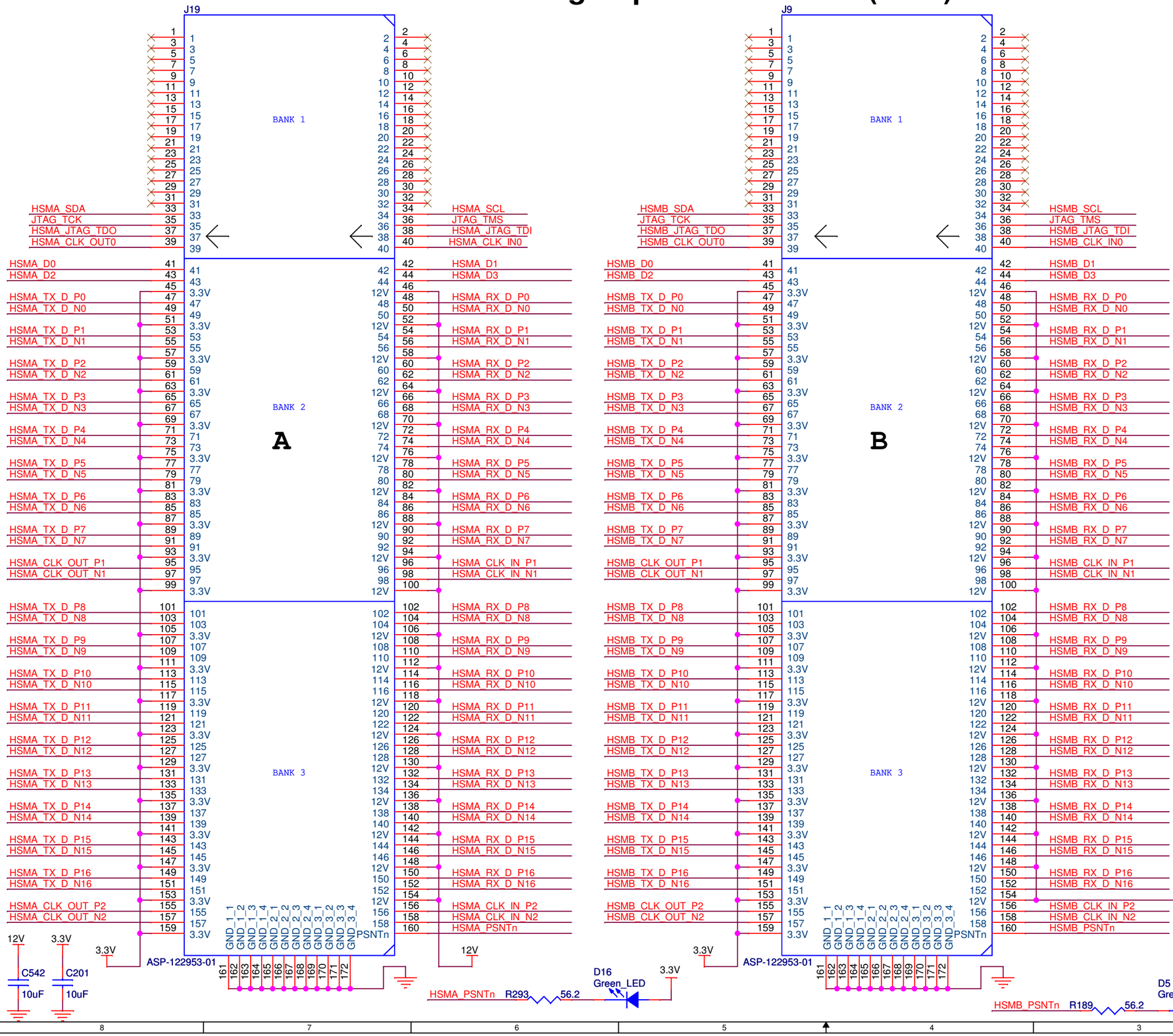
High Speed Mezzanine (HSM) Interface



HSMC JTAG INTERFACE

HSMA_JTAG_TDO — HSMA_JTAG_TDO 12
HSMB_JTAG_TDO — HSMB_JTAG_TDO 12

JTAG_TCK — JTAG_TCK 12,13,23
JTAG_TMS — JTAG_TMS 12,13,23

HSMA_JTAG_TDI — HSMA_JTAG_TDI 12
HSMB_JTAG_TDI — HSMB_JTAG_TDI 12

HSMC PORT A

HSMA_SDA — HSMA_SDA 16
HSMA_SCL — HSMA_SCL 16

HSMA_CLK_IN0 — HSMA_CLK_IN0 10
HSMA_CLK_OUT0 — HSMA_CLK_OUT0 16

HSMA_CLK_IN_P[2:1] — HSMA_CLK_IN_P[2:1] 10

HSMA_CLK_IN_N[2:1] — HSMA_CLK_IN_N[2:1] 10

HSMA_CLK_OUT_P[2:1] — HSMA_CLK_OUT_P[2:1] 10,16

HSMA_CLK_OUT_N[2:1] — HSMA_CLK_OUT_N[2:1] 10,16

HSMA_D[3:0] — HSMA_D[3:0] 15

HSMA_TX_D_P[16:0] — HSMA_TX_D_P[16:0] 10,16

HSMA_TX_D_N[16:0] — HSMA_TX_D_N[16:0] 10,16

HSMA_RX_D_P[16:0] — HSMA_RX_D_P[16:0] 16

HSMA_RX_D_N[16:0] — HSMA_RX_D_N[16:0] 16

HSMC PORT B

HSMB_SDA — HSMB_SDA 10
HSMB_SCL — HSMB_SCL 14

HSMB_CLK_IN0 — HSMB_CLK_IN0 10
HSMB_CLK_OUT0 — HSMB_CLK_OUT0 16

HSMB_CLK_IN_P[2:1] — HSMB_CLK_IN_P[2:1] 10

HSMB_CLK_IN_N[2:1] — HSMB_CLK_IN_N[2:1] 10

HSMB_CLK_OUT_P[2:1] — HSMB_CLK_OUT_P[2:1] 10,16

HSMB_CLK_OUT_N[2:1] — HSMB_CLK_OUT_N[2:1] 10,16

HSMB_D[3:0] — HSMB_D[3:0] 16

HSMB_TX_D_P[16:0] — HSMB_TX_D_P[16:0] 16

HSMB_TX_D_N[16:0] — HSMB_TX_D_N[16:0] 16

HSMB_RX_D_P[16:0] — HSMB_RX_D_P[16:0] 16

HSMB_RX_D_N[16:0] — HSMB_RX_D_N[16:0] 16

HSMA_PSNTn — HSMA_PSNTn 23
HSMB_PSNTn — HSMB_PSNTn 23

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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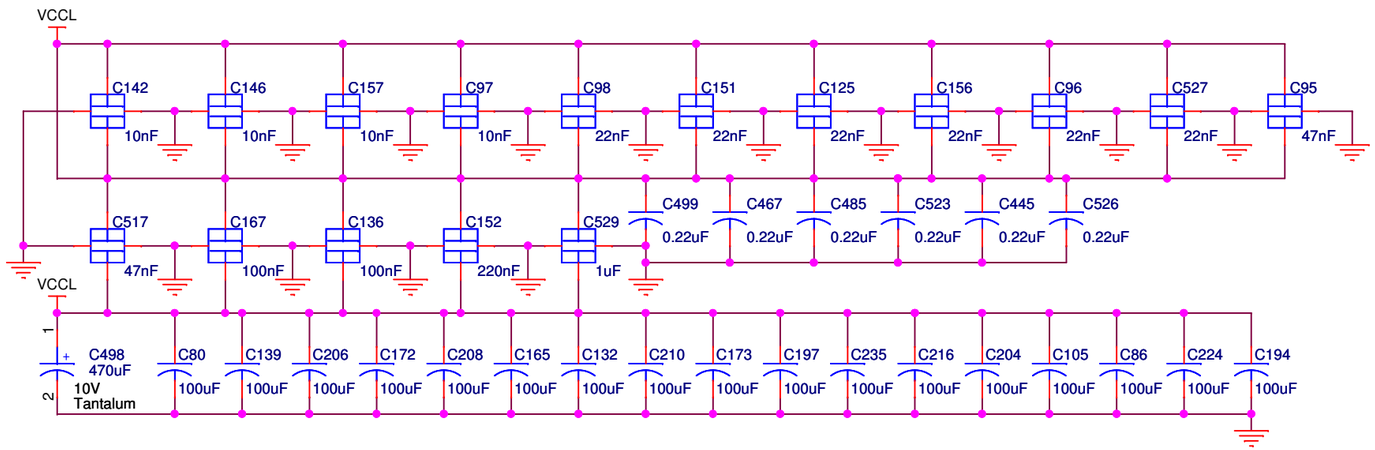
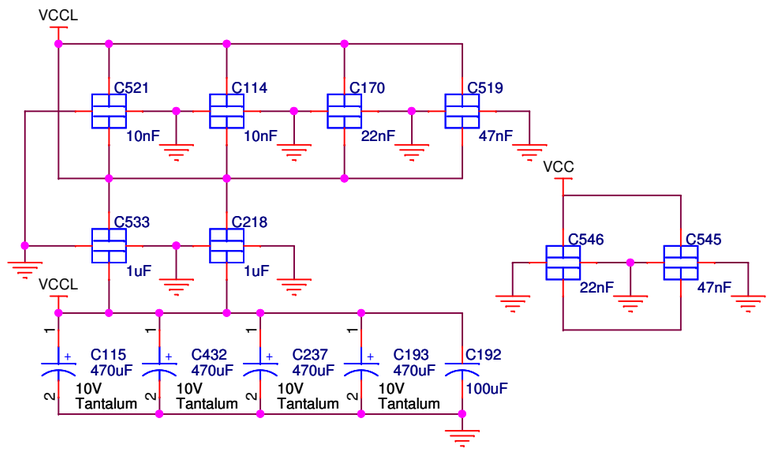
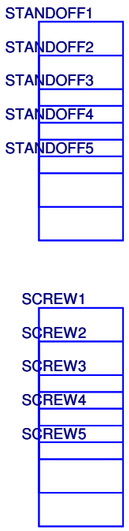
Place 6 vias minimum on each X2Y cap.

Decoupling 1

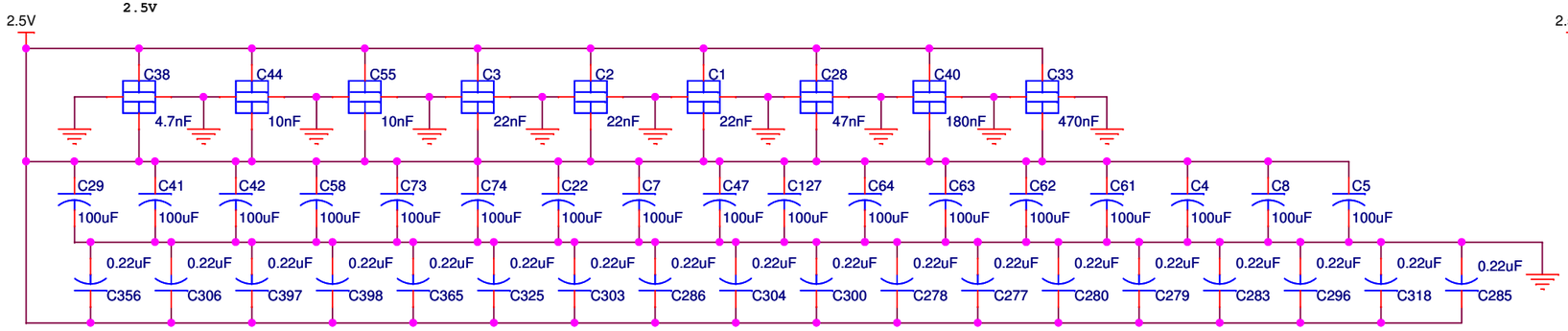
FPGA VCCL

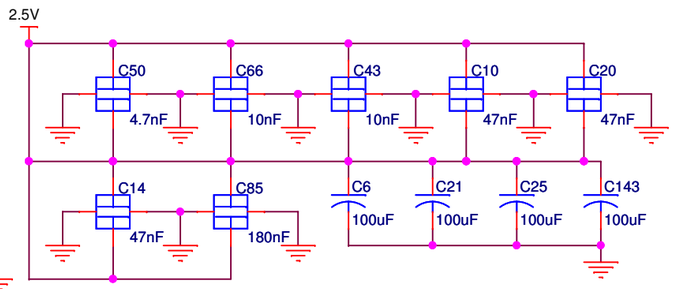




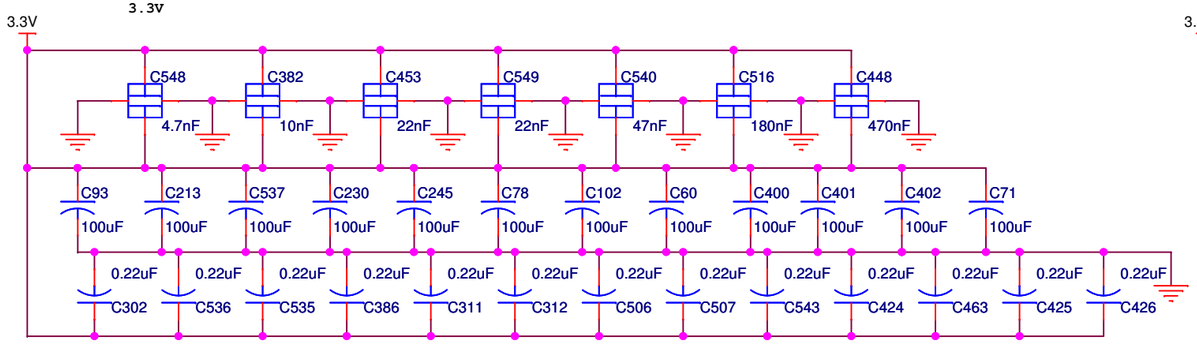


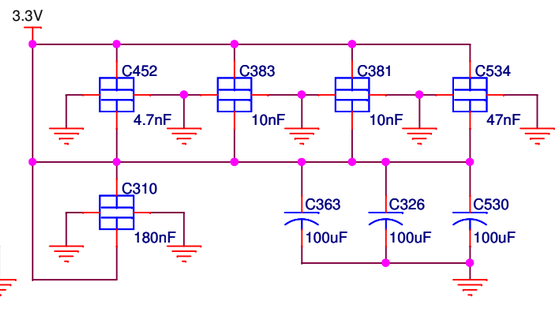
2.5V



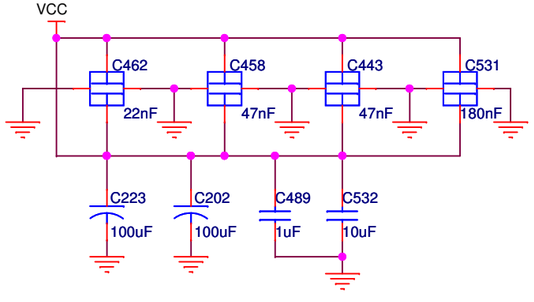


3.3V

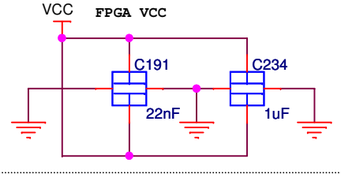




FPGA VCC



FPGA VCC



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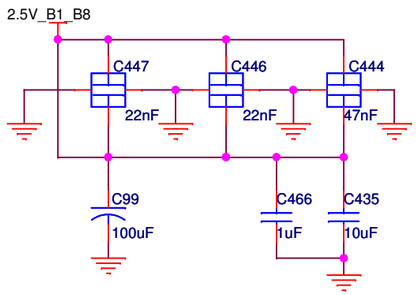
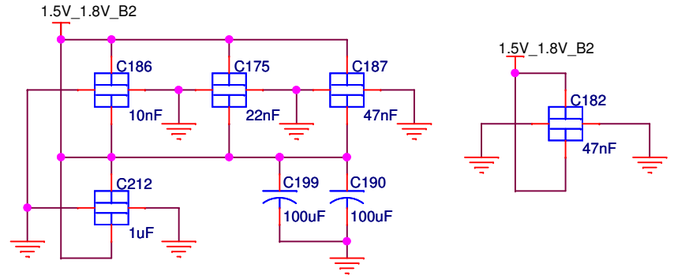
Place 6 vias minimum on each X2Y cap.

Decoupling 2

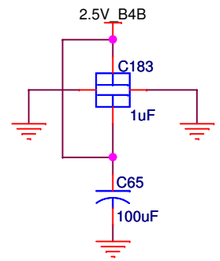
FPGA Banks 1 and 8



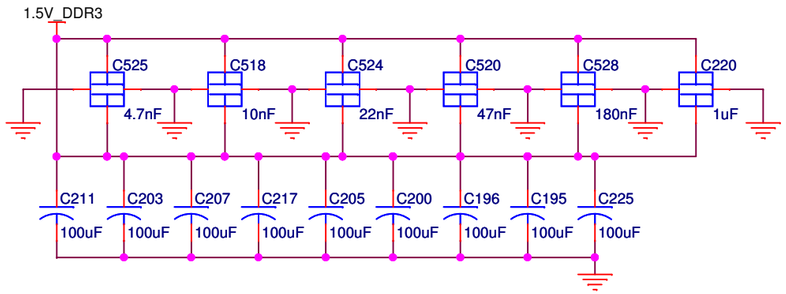
FPGA Bank 2

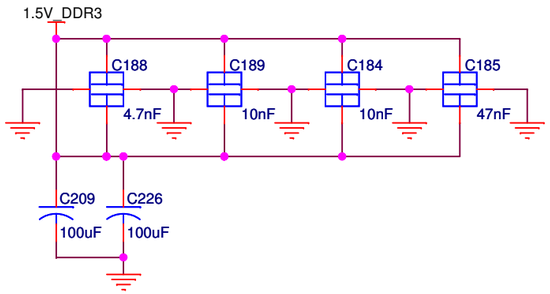


FPGA Bank 4B

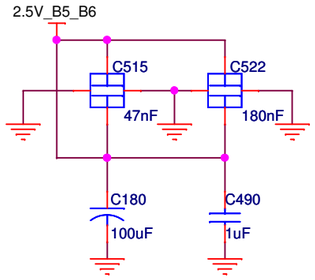


FPGA Banks 3 and 4, except 4B

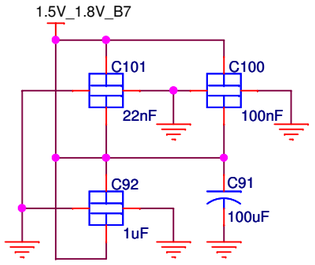


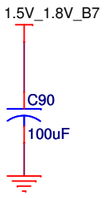


FPGA Banks 5 and 6



FPGA Bank 7





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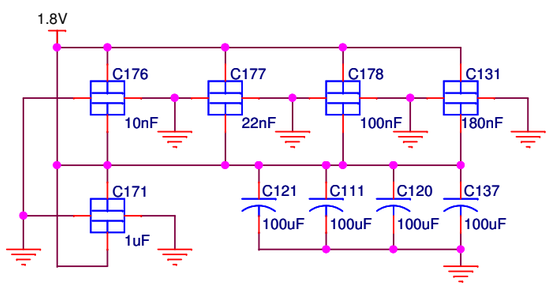

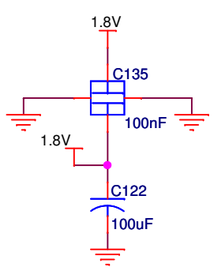

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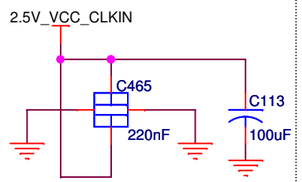

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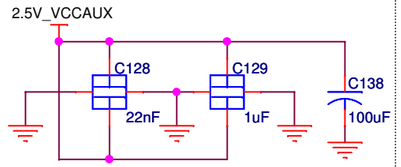

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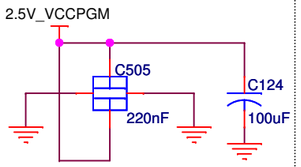

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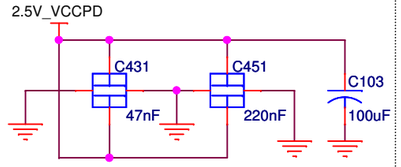

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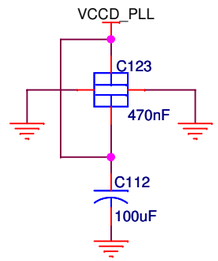

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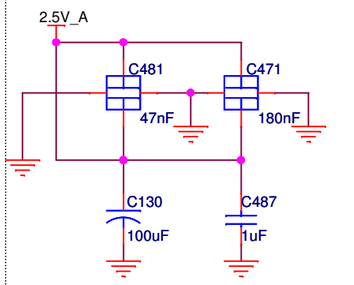

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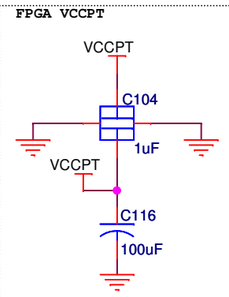

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Title: **Stratix IV E FPGA Development Kit Board**

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