REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

VIN0 J9-1 R0 51r LK0 1k S0 U31-A AD8034ARTZ
VIN1 J9-3 R1 51r LK1 1k S1 U31-B AD8034ARTZ
VIN2 J9-5 R2 51r LK2 1k S2 U32-A AD8034ARTZ
VIN3 J9-7 R3 51r LK3 1k S3 U32-B AD8034ARTZ
VIN4 R4 51r LK4 0R S4 U33-A AD8034ARTZ
VIN5 R5 51r LK5 0R S5 U33-B AD8034ARTZ
VIN6 R6 51r LK6 0R S6 U34-A AD8034ARTZ
VIN7 R7 51r LK7 0R S7 U34-B AD8034ARTZ
VIN8 J9-9 R8 51r LK8 0R S8 U35-A AD8034ARTZ
VIN9 J9-11 R9 51r LK9 0R S9 U35-B AD8034ARTZ
VIN10 J9-13 R10 51r LK10 0R S10 U36-A AD8034ARTZ
VIN11 J9-15 R11 51r LK11 0R S11 U36-B AD8034ARTZ
VIN12 J9-17 R12 51r LK12 0R S12 U37-A AD8034ARTZ
VIN13 J9-19 R13 51r LK13 0R S13 U37-B AD8034ARTZ
VIN14 J9-21 R14 51r LK14 0R S14 U38-A AD8034ARTZ
VIN15 J9-23 R15 51r LK15 0R S15 U38-B AD8034ARTZ

U1 AD7490
VIN0 13, VIN1 12, VIN2 11, VIN3 10, VIN4 9, VIN5 8, VIN6 7, VIN7 6, VIN8 5, VIN9 3, VIN10 2, VIN11 1, VIN12 28, VIN13 27, VIN14 26, VIN15 25
VDD 22, VDRIVE 17, CS 20, DOUT 15, SCLK 16, DIN 19, REFIN 23, AGND 24, AGND 14, AGND 21, NC 4, NC 18

VDD
VDRIVE_3V3
C5 0.1uF, C6 10uF
LK19 (A, B, C)
C7 0.1uF, C8 10uF
T_CS CS_SW
T_DOUT DOUT_SW
T_SCLK SCLK_SW
T_DIN DIN_SW
VREF
C11 0.1uF
LK17 (A, B, C)
STAR1
J8-1 VDRIVE
J8-2 DGND
C9 0.1uF, C10 10uF

U7 ADR3425
VOUT_FORCE 6, VOUT_SENSE 5, GND_SENSE 2, GND_FORCE 1, VIN 4, ENABLE 3
C3 0.1uF
C13 0.1uF, C14 10uF

VREF J5
C15 0.1uF, C16 10uF

REF192 U9
O/P 6, VIN 2, SLEEP 3, GND 4
C17 0.1uF, C18 10uF

Join under U1

AGND
J9-2, J9-4, J9-6, J9-8, J9-10, J9-12, J9-14, J9-16, J9-18, J9-20, J9-22, J9-24

DRAWN: Jimmy O'Callaghan	DATED: Feb' 12	COMPANY: Analog Devices Inc.	
CHECKED: Jimmy O'Callaghan	DATED: Feb' 12	TITLE: Evaluation board for AD7490	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: C
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: EVAL-AD7490-SDZ	REV: A
		SCALE: <Scale>	SHEET: 1 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

LAYOUT NOTE. This 10uF cap is placed near the +12V Supply

10uF C32

+AMP

U31-C AD8034ARTZ — C50 0.1uF, C12 0.1uF, C52 0.1uF

U32-C AD8034ARTZ — C51 0.1uF, C24 0.1uF, C53 0.1uF

U33-C AD8034ARTZ — C23 0.1uF, C30 0.1uF, C29 0.1uF

U34-C AD8034ARTZ — C45 0.1uF, C54 0.1uF, C46 0.1uF

U35-C AD8034ARTZ — C55 0.1uF, C57 0.1uF, C56 0.1uF

U36-C AD8034ARTZ — C58 0.1uF, C60 0.1uF, C59 0.1uF

U37-C AD8034ARTZ — C39 0.1uF, C41 0.1uF, C40 0.1uF

U38-C AD8034ARTZ — C42 0.1uF, C44 0.1uF, C43 0.1uF

-AMP

LAYOUT NOTE. Each set of 3 0.1uF CAPs should be as close as possible to the relevant IC

C34 10uF

LAYOUT NOTE. This 10uF cap is placed near the -12V Supply

R24 1k — U4-B AD8034ARTZ

VREF — U3-A AD8034ARTZ — R17 3k 0.1%

R18 1k 0.1% — U3-B AD8034ARTZ — R22 1k 0.1% — C48 68pF — J3 Biased Vin

Vin J1 — LK22 — R20 1k 0.1% — C47 68pF, R23 1k 0.1% — U4-A AD8034ARTZ — R21 1k 0.1%

R19 51r

LAYOUT NOTE. This 10uF cap is placed near the +12V Supply

10uF C19

+AMP

U3-C AD8034ARTZ — C38 0.1uF, C62 0.1uF, C61 0.1uF

U4-C AD8034ARTZ — C22 0.1uF, C35 0.1uF, C31 0.1uF

U4 wiring fixed

-AMP

C20 10uF

LAYOUT NOTE. This 10uF cap is placed near the -12V Supply

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REVISION RECORD			
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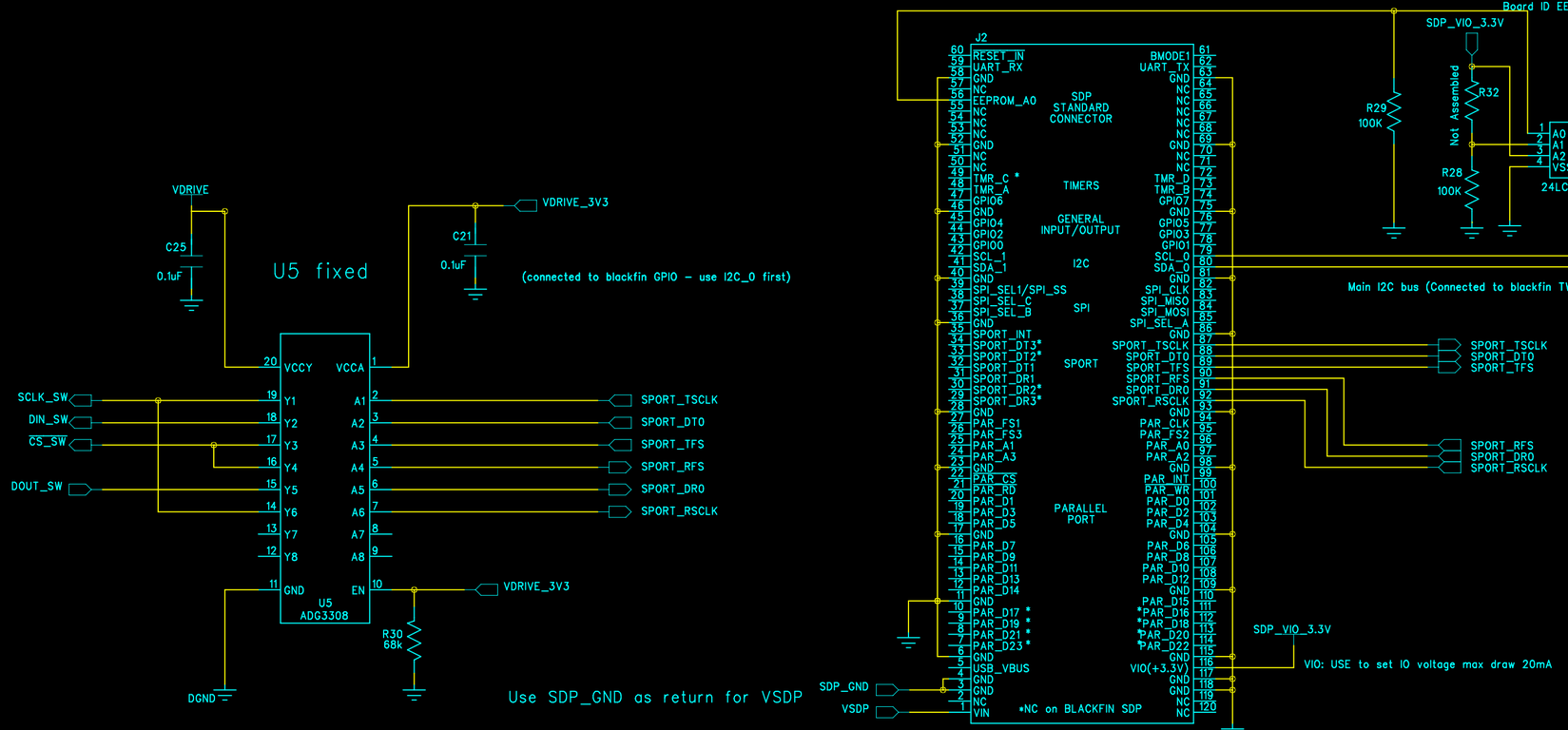
I2C bus 1 is common across both connectors on SDP – Pull up resistors required

BMODE1: Pull up with a 10K resistor to set SDP to boot from a SPI FLASH on the daughter board

Board ID EEPROM (24LC32) must be on I2C bus 0,

Board ID EEPROM (24LC32) must be on I2C bus 0,



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RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: EVAL-AD7490-SDZ	REV: A
		SCALE: <Scale>	SHEET: 3 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

R117 14R
R105 8R2
R104 2R2
L104 1.0uH 60mR LQH32CN1R0M33L
-12/-15V
C117 1uF 11mR
D101 B0540W-7-F
C107 10uF 14mR
C102 10uF 14mR
C103 10uF 14mR
C104 10uF 14mR
LK101
-AMP
J100-1
-12V
AGND
J100-2
+AMP
J100-3
+12V
LK102
L102 15uH DRQ73-150-R
C108 1uF 5.5mR
EXT_PWR
R807 470R
R102 63R4
C115 1uF 9mR 16V
C112 1uF 9mR 16V
C113 1uF 9mR 16V
C114 1uF 9mR 16V
L101 15uH DRQ73-150-R
R103 14R
R107 8R2
R106 2R2
C101 1uF 9mR 16V
D100 B0540W-7-F
+ 12/15V
L103 1.0uH 60mR LQH32CN1R0M33L
C100 1uF 11mR
C118 10uF 14mR
C119 10uF 14mR
C120 10uF 14mR
C121 10uF 14mR
Q101 MMBT3904LT1G
C126 1uF 5.5mR
D102 BZT52 5.1V
SGND
C124
R118
Q100 SI2304DDS-T1-GE3
ADP1613ARMZ
COMP
FB
EN
GND
SS
FREQ
VIN
SW
U100
+/-12V_EN
C111 1uF
C116 1uF
C109 6.8nF
C110 10pF
Join at U100.4
R100 150k
R113 8k25
R114 71k5
12V divider

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COMPANY: Analog Devices Inc.

TITLE: Evaluation board for AD7490

CODE:	SIZE:	DRAWING NO:	REV:
	C	EVAL-AD7490-SDZ	A

SCALE: <Scale> SHEET: 4 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

EXT_PWR
R715 2k4 1%
R707 68k 5%
R710 470R
R709 61R9
Q700 MMBT3904LT1G
C700 1uF 5.5mR
D701 BZT52 5.1V
PWR IN
LED1 GREEN

VDD J703-1
AGND J703-2
VDD_EN
EXT_PWR
ADP3303-5
IN1 IN2 SD OUT1 OUT2 ERROR NR GND
U704
R712 330k
R0402 5%
C721 1uF
C722 10nF
C720 10nF
LK701
C723 10nF
C711 10uF
VDD
Analog power supply

U703 ADM1185ARMZ
VDD VIN1 VIN2 VIN3 VIN4 OUT1 OUT2 OUT3 PWRGD GND
R716 10k 5%
R717 10k 5%
R718 10k 5%
R719 10k 5%
VDD_EN
+/-12V_EN
C715 DNP
R708 18k 5%
VDD
R701 68k 5%
C710 DNP
R705 18k 5%
+AMP
R704 68k 5%
C713 DNP
R702 18k 5%
VSDP
R703 68k 5%
C714 DNP
R706 18k 5%

C160–C163 placed only if specific delays needed

Power Up sequence
V_IN enables VCC Supply
VCC enables the +12V / −12V supplies
+12V enables the VSDP
If any power supply drops out then all PSUs are disabled

EXT_PWR
R713 2k4 1%
PWR GD
LED2 GREEN
Q701 2N7002

R742 100K
DNI R745 0r
ADP7104ARDZ
VIN EN/UVLO VOUT U707 N/C ADJ PG GND EP GND
R746 0r
R747 47k
R748 10k
R743 100K
C726 1uF
C727 10nF
C728 10nF
C729 1uF
EXT_PWR

SDP_VIO_3.3V
VSDP
R740 68k 5%
R741 18k 5%
U741 ADP190ACBZ
VIN EN VOUT GND
A1 B1 A2 B2
VDRIVE_3V3

ADP7104ARDZ-5.0
U706 VIN EN/UVLO VOUT N/C SENSE PG GND EP GND
VSDP
C730 10nF
C731 1uF
SDP_GND

EXT PWR 7–9V
J702-3
J702-4
J700-1
J700-2
J702-1
J702-2
EXT_PWR
Screw Block for V_IN. Remove if not needed
STAR2
STAR4
STAR6
STAR5
STAR3
AGND
SDP_GND
EXT_GND
Ground Star point. Place near to V_in jack plug J4/ J1

5V For SDP

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