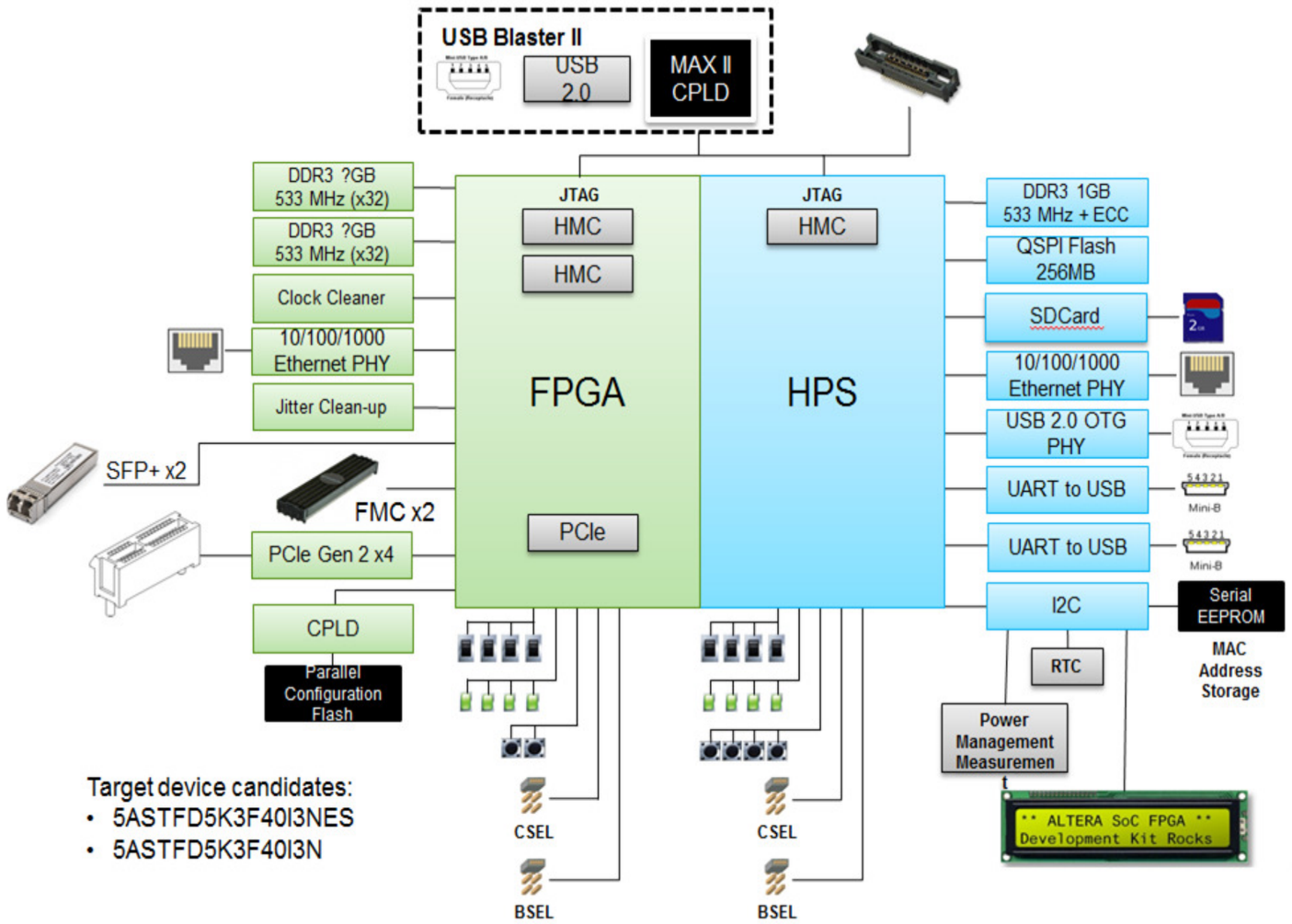
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0320807-C1
Gerber Files	110-0320807-C1
PCB Design Files	120-0320807-C1
Assembly Drawing	130-0320807-C1
Fab Drawing	140-0320807-C1
Schematic Drawing	150-0320807-C1
PCB Film	160-0320807-C1
Bill of Materials	170-0320807-C1
Schematic Design Files	180-0320807-C1
Functional Specification	210-0320807-C1
PCB Layout Guidelines	220-0320807-C1
Assembly Rework	320-0320807-C1

2. 1172 Parts, 88 Library Parts, 1330 Nets, 6643 Pins

Arria V SoC FPGA Development Kit Board



REV	DATE	PAGES	DESCRIPTION
A1		All	INITIAL REVISION A RELEASE
02		All	Changes for Rev B
B1		All	INITIAL RELEASE TO B
			Changes:
			Fixed connections for FPGA Power Monitor
			Added FMCB and LMK interface
			Added pull-ups for Power Monitor devices
			Added series resistor (0-ohm) between run pin and Power Monitor device
			Changed QSPI device to one with reset pin
C1		All	INITIAL RELEASE TO C
			Changes:
			Removed SPI signals from MAX device to LMK device
			Swapped pin locations for CLK_100M_FPGA and SPI_SDIO to remove critical warnings
			Added RC circuit for JTAG clocks (JTAG_MUX_TCK, JTAG_HPS_TCK)
			Added resistor mux for selecting clock and sync from LMK or FPGA for FMCA and FMCB
			Changed LTC2978 to LTC2977

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Title: **Arria V SoC FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0320807-C1 (6XX-44209R)	C1

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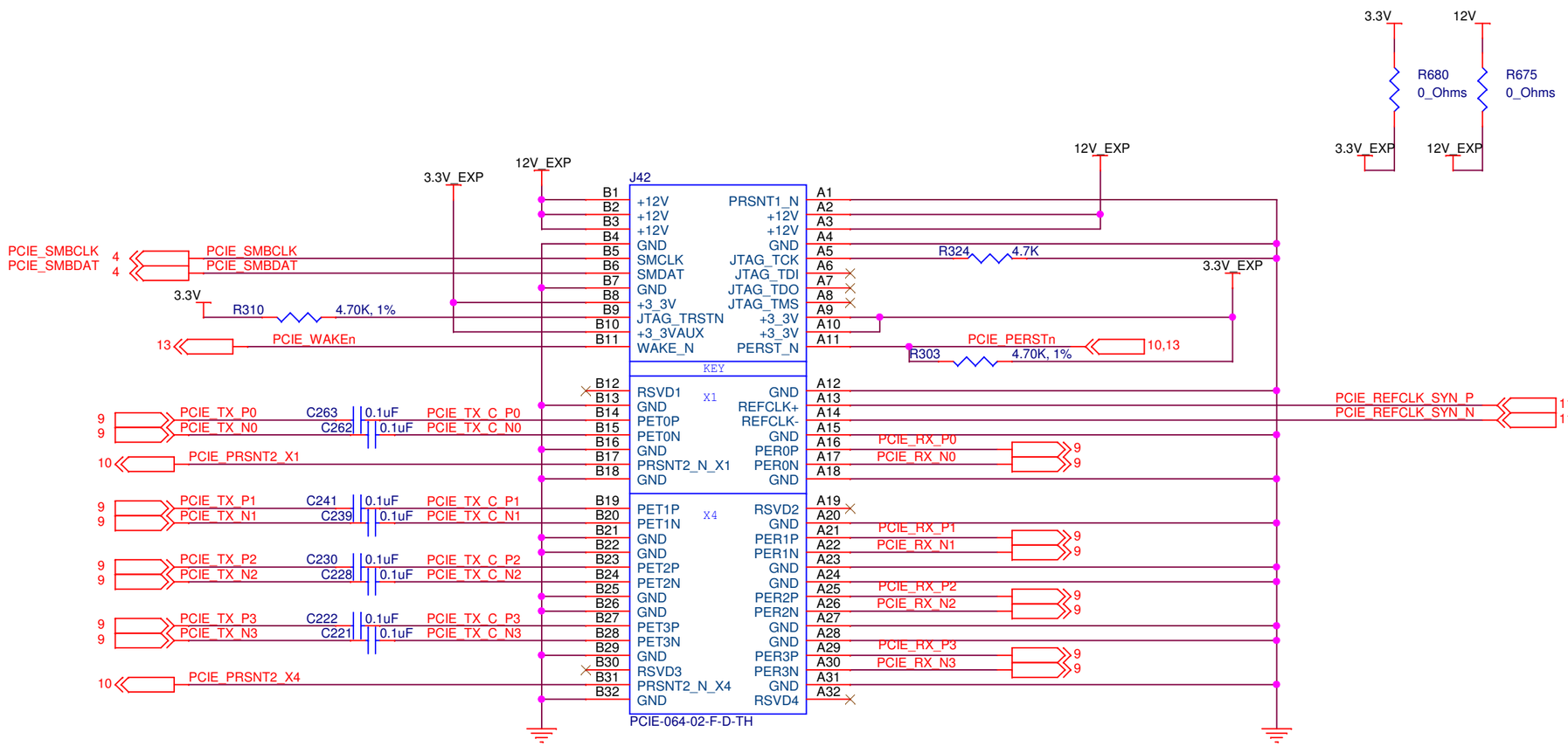
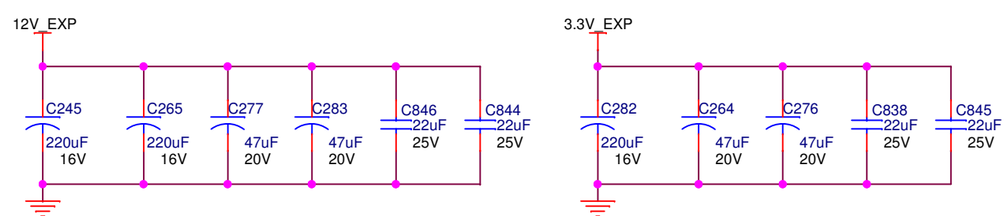
PCI Express Connector





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Title: **Arria V SoC FPGA Development Kit Board**

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Arria V ST Bank 3

R499
100, 1%

U41A

Arria V SX (SoC) Bank 3

Bank 3A
1.5 Volt

DDR3A_RZQ	AN33	RZQ_0,DIFFIO_TX_B1_N			
			HMC_CK#,DIFFIO_RX_B23_N	AN29	DDR3A_CLK_N
			HMC_CK,DIFFIO_RX_B23_P	AP29	DDR3A_CLK_P
DDR3A_A0	AU29	HMC_A_0,DIFFIO_RX_B21_P		AP30	DDR3A_CKE
DDR3A_A1	AT29	HMC_A_1,DIFFIO_RX_B21_N	HMC_CKE_0,HMC_RLD2_A_16,DIFFIO_TX_B22_P	AN30	
DDR3A_A2	AV30	HMC_A_2,DIFFIO_TX_B20_P	HMC_CKE_1,HMC_RLD2_A_17,DIFFIO_TX_B22_N		
DDR3A_A3	AU30	HMC_A_3,DIFFIO_TX_B20_N		AP32	DDR3A_CSn
DDR3A_A4	AT30	HMC_A_4,DIFFIO_RX_B19_P	HMC_CS#_0,DIFFIO_TX_B8_P	AN32	
DDR3A_A5	AR30	HMC_A_5,DIFFIO_RX_B19_N	HMC_CS#_1,DIFFIO_TX_B8_N		
DDR3A_A6	AL30	HMC_A_6,DIFFIO_TX_B18_P		AM31	DDR3A_ODT
DDR3A_A7	AK30	HMC_A_7,DIFFIO_TX_B18_N	HMC_ODT_0,HMC_RLD2_A_18,DIFFIO_TX_B10_P	AL31	
DDR3A_A8	AW31	HMC_A_8,DIFFIO_RX_B17_P	HMC_ODT_1,HMC_RLD2_A_20,DIFFIO_TX_B10_N		
DDR3A_A9	AW30	HMC_A_9,DIFFIO_RX_B17_N		AN31	DDR3A_RASn
DDR3A_A10	AV31	HMC_A_10,DIFFIO_TX_B16_P	HMC_RAS#,HMC_RLD2_A_21,DIFFIO_TX_B12_N	AW32	DDR3A_CASn
DDR3A_A11	AU31	HMC_A_11,DIFFIO_TX_B16_N	HMC_CAS#,HMC_RLD2_REF#,HMC_QDR2_WPS#,DIFFIO_RX_B11_P	AW33	DDR3A_WEn
DDR3A_A12	AH30	HMC_A_12,DIFFIO_RX_B15_P	HMC_WE#,DIFFIO_RX_B11_N		
DDR3A_A13	AG30	HMC_A_13,DIFFIO_RX_B15_N			
DDR3A_A14	AE29	HMC_A_14,DIFFIO_TX_B14_P		AP33	USB_B2_DATA0
	AD29	HMC_A_15,DIFFIO_TX_B14_N		AL32	USB_B2_DATA1
			DIFFIO_TX_B1_P,DQ1B	AK31	USB_B2_DATA2
DDR3A_BA0	AT31		DIFFIO_TX_B3_P,DQ1B		
DDR3A_BA1	AR31	HMC_BA_0,HMC_QDR2_A_16,DIFFIO_RX_B13_P	DQ1B	AK32	USB_B2_DATA3
DDR3A_BA2	AP31	HMC_BA_1,HMC_QDR2_A_17,DIFFIO_RX_B13_N			
		HMC_BA_2,HMC_QDR2_A_18,DIFFIO_TX_B12_P	DIFFIO_TX_B3_N		

Bank 3B
1.5 Volt

			HMC_DM2,DIFFIO_TX_B33_P	AK27	DDR3A_DM1
			HMC_DQS2,HMC_RLD2_QK#2,HMC_QDR2_CQ2/CQ#2,DIFFIO_RX_B34_P	AW28	DDR3A_DQS_P1
			HMC_DQS#2,HMC_RLD2_QK2,DIFFIO_RX_B34_N	AW29	DDR3A_DQS_N1
DDR3A_DM0	AL29				
DDR3A_DQS_P0	AJ28	HMC_DM1,DIFFIO_TX_B26_P			
DDR3A_DQS_N0	AH28	HMC_DQS1,HMC_RLD2_QK#1,HMC_QDR2_CQ1/CQ#1,DIFFIO_RX_B27_P			
		HMC_DQS#1,HMC_RLD2_QK1,DIFFIO_RX_B27_N			
			HMC_DQ2_0,DIFFIO_RX_B38_P	AW27	DDR3A_DQ8
			HMC_DQ2_1,DIFFIO_RX_B38_N	AV27	DDR3A_DQ9
DDR3A_DQ0	AD27		HMC_DQ2_2,DIFFIO_TX_B37_P	AN27	DDR3A_DQ10
DDR3A_DQ1	AC27	HMC_DQ1_0,DIFFIO_RX_B30_P	HMC_DQ2_3,DIFFIO_RX_B36_P	AU27	DDR3A_DQ11
DDR3A_DQ2	AM28	HMC_DQ1_1,DIFFIO_RX_B30_N	HMC_DQ2_4,DIFFIO_RX_B36_N	AT27	DDR3A_DQ12
DDR3A_DQ3	AB28	HMC_DQ1_2,	HMC_DQ2_5,DIFFIO_TX_B35_P	AR27	DDR3A_DQ13
DDR3A_DQ4	AB27	HMC_DQ1_3,DIFFIO_RX_B29_P	HMC_DQ2_6,DIFFIO_RX_B32_P	AV28	DDR3A_DQ14
DDR3A_DQ5	AE28	HMC_DQ1_4,DIFFIO_RX_B29_N	HMC_DQ2_7,DIFFIO_RX_B32_N	AU28	DDR3A_DQ15
DDR3A_DQ6	AG28	HMC_DQ1_5,DIFFIO_TX_B28_P	HMC_DQ2_8,DIFFIO_TX_B31_P	AR28	
DDR3A_DQ7	AF28	HMC_DQ1_6,DIFFIO_RX_B25_P			
	AC29	HMC_DQ1_7,DIFFIO_RX_B25_N		AP28	USB_B2_DATA4
		HMC_DQ1_8,DIFFIO_TX_B24_P	DIFFIO_TX_B31_N	AJ27	USB_B2_DATA5
DDR3A_RESETn	AB29		DIFFIO_TX_B33_N	AP27	USB_B2_DATA6
		HMC_RESET#,HMC_RLD2_A_19,DIFFIO_TX_B24_N	DIFFIO_TX_B35_N	AM27	USB_B2_DATA7
	AK29		DIFFIO_TX_B37_N		
	AD28	DIFFIO_TX_B26_N			
		DIFFIO_TX_B28_N			

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U41O

Arria V SX (SoC) Bank 3

Bank 3C
1.5 Volt

DDR3A_DM2	AF27	HMC_DM3,DIFFIO_TX_B41_P		AL24	USER_DIPSW_FPGA0
DDR3A_DQS_P2	AF25	HMC_DQS3,HMC_RLD2_QK#3,HMC_QDR2_CQ3/CQ#3,DIFFIO_RX_B42_P		AF24	USER_DIPSW_FPGA1
DDR3A_DQS_N2	AE25	HMC_DQS#3,HMC_RLD2_QK3,DIFFIO_RX_B42_N		AE24	USER_DIPSW_FPGA2
			HMC_DM5,DIFFIO_TX_B56_P		
			HMC_DQS5,HMC_RLD2_QK#5,HMC_QDR2_CQ5/CQ#5,DIFFIO_RX_B57_P	AU23	USER_DIPSW_FPGA3
			HMC_DQS#5,HMC_RLD2_QK5,DIFFIO_RX_B57_N	AT23	USER_PB_FPGA0
DDR3A_DQ16	AH25	HMC_DQ3_0,DIFFIO_RX_B46_P		AP24	USER_PB_FPGA1
DDR3A_DQ17	AG25	HMC_DQ3_1,DIFFIO_RX_B46_N	HMC_DQ5_0,DIFFIO_RX_B61_P	AW24	USER_PB_FPGA2
DDR3A_DQ18	AE26	HMC_DQ3_2,DIFFIO_TX_B45_P	HMC_DQ5_1,DIFFIO_RX_B61_N	AW23	USER_PB_FPGA3
DDR3A_DQ19	AH26	HMC_DQ3_3,DIFFIO_RX_B44_P	HMC_DQ5_2,DIFFIO_TX_B60_P	AH24	USER_LED_FPGA0
DDR3A_DQ20	AG26	HMC_DQ3_4,DIFFIO_RX_B44_N	HMC_DQ5_3,DIFFIO_RX_B59_P	AU24	USER_LED_FPGA1
DDR3A_DQ21	AD25	HMC_DQ3_5,DIFFIO_TX_B43_P	HMC_DQ5_4,DIFFIO_RX_B59_N	AT24	USER_LED_FPGA2
DDR3A_DQ22	AC25	HMC_DQ3_6,DIFFIO_RX_B40_P	HMC_DQ5_5,DIFFIO_TX_B58_P	AD24	USER_LED_FPGA3
DDR3A_DQ23	AB25	HMC_DQ3_7,DIFFIO_RX_B40_N	HMC_DQ5_6,DIFFIO_RX_B55_P		
	AH27	HMC_DQ3_8,DIFFIO_TX_B39_P	HMC_DQ5_7,DIFFIO_RX_B55_N		
			HMC_DQ5_8,DIFFIO_TX_B54_P		
DDR3A_DM3	AK25	HMC_DM4,DIFFIO_TX_B49_P			
DDR3A_DQS_P3	AU26	HMC_DQS4,HMC_RLD2_QK#4,HMC_QDR2_CQ4/CQ#4,DIFFIO_RX_B50_P		AG27	USB_FULL
DDR3A_DQS_N3	AT26	HMC_DQS#4,HMC_RLD2_QK4,DIFFIO_RX_B50_N	DIFFIO_TX_B39_N	AE27	USB_EMPTY
			DIFFIO_TX_B41_N	AC24	USB_SCL
DDR3A_DQ24	AV24	HMC_DQ4_0,DIFFIO_RX_B53_P	DIFFIO_TX_B43_N	AD26	USB_SDA
DDR3A_DQ25	AV25	HMC_DQ4_1,DIFFIO_RX_B53_N	DIFFIO_TX_B45_N	AN26	USB_B2_CLK
DDR3A_DQ26	AL26	HMC_DQ4_2	DIFFIO_TX_B47_N	AJ25	USB_RESETn
DDR3A_DQ27	AW26	HMC_DQ4_3,DIFFIO_RX_B52_P	DIFFIO_TX_B49_N	AR25	USB_OEn
DDR3A_DQ28	AW25	HMC_DQ4_4,DIFFIO_RX_B52_N	DIFFIO_TX_B51_N	AD23	USB_RDn
DDR3A_DQ29	AT25	HMC_DQ4_5,DIFFIO_TX_B51_P	DIFFIO_TX_B54_N	AK24	USB_WRn
DDR3A_DQ30	AN25	HMC_DQ4_6,DIFFIO_TX_B48_P	DIFFIO_TX_B56_N	AG24	
DDR3A_DQ31	AM25	HMC_DQ4_7,DIFFIO_RX_B48_N	DIFFIO_TX_B58_N	AN24	
	AP26	HMC_DQ4_8,DIFFIO_TX_B47_P	DIFFIO_TX_B60_N		

Bank 3D
2.5 Volt

			DIFFIO_RX_B73_P,DQS10B	AT21	ENET2_TX_D0
			DIFFIO_RX_B73_N,DQSn10B	AR21	ENET2_TX_D1
			DQ10B	AK21	ENET2_TX_D2
			DIFFIO_TX_B70_P,DQ10B	AP22	ENET2_TX_D3
		DIFFIO_RX_B65_P,DQS9B	DIFFIO_RX_B71_P,DQ10B	AW20	ENET2_TX_EN
		DIFFIO_RX_B65_N,DQSn9B	DIFFIO_RX_B71_N,DQ10B	AW19	ENET2_RX_D0
ENET1_TX_D0	AU22	DIFFIO_RX_B63_P,DQ9B	DIFFIO_TX_B72_P,DQ10B	AL22	ENET2_RX_D1
ENET1_TX_D1	AT22	DIFFIO_RX_B63_N,DQ9B	DIFFIO_TX_B74_P,DQ10B	AH22	ENET2_RX_D2
ENET1_TX_D2	AE23	DIFFIO_TX_B62_P,DQ9B	DIFFIO_RX_B75_P,DQ10B	AU20	ENET2_RX_D3
ENET1_TX_D3	AD22	DIFFIO_TX_B64_P,DQ9B	DIFFIO_RX_B75_N,DQ10B	AT20	ENET2_RX_CLK
ENET1_TX_EN	AP23	DIFFIO_TX_B66_P,DQ9B			
ENET1_RX_D0	AL23	DIFFIO_RX_B67_P,DQ9B	DIFFIO_TX_B77_P,DQ11B	AN21	ENET2_TX_CLK_FB
ENET1_RX_D1	AW22	DIFFIO_RX_B67_N,DQ9B	DIFFIO_TX_B81_P,DQ11B	AP20	ENET2_RX_DV
ENET1_RX_D2	AW21	DIFFIO_TX_B68_P,DQ9B	DIFFIO_TX_B83_P,DQ11B	AH20	P1TXERR
ENET1_RX_D3	AV21	DIFFIO_RX_B69_P,DQ9B			
ENET1_RX_ERROR	AH23	DIFFIO_RX_B69_N,DQ9B	DIFFIO_TX_B70_N	AN22	ENET2_RX_ERROR
ENET1_RX_DV	AF22		DIFFIO_TX_B72_N	AK22	ENET_FPGA_MDIO
ENET1_RX_CLK	AE22		DIFFIO_TX_B74_N	AG22	ENET_FPGA_MDC
		DIFFIO_TX_B62_N	DIFFIO_TX_B77_N	AM21	SDI_CLK148_UP
ENET1_TX_CLK_FB	AN23	DIFFIO_TX_B64_N	DIFFIO_TX_B81_N	AN20	SDI_CLK148_DN
P0TXERR	AK23	DIFFIO_TX_B66_N	DIFFIO_TX_B83_N	AG20	PCIE_SMBCLK
ENET_DUAL_RESETn	AV22	DIFFIO_TX_B68_N			
PCIE_SMBDAT	AG23				

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ETHERNET FPGA

ENET1_TX_D[3..0]
ENET1_RX_D[3..0]
ENET2_TX_D[3..0]
ENET2_RX_D[3..0]

1.5V Signals

USER_DIPSW_FPGA[3:0]
USER_PB_FPGA[3:0]
USER_LED_FPGA[3:0]
USB_B2_DATA[7:0]
USB_FULL
USB_EMPTY
USB_SCL
USB_SDA
USB_B2_CLK
USB_RESETn
USB_OEn
USB_RDn
USB_WRn

DDR3 PORT A

DDR3A_A[14:0]
DDR3A_BA[2:0]
DDR3A_CASn
DDR3A_CLK_P
DDR3A_CLK_N
DDR3A_CKE
DDR3A_CSn
DDR3A_ODT
DDR3A_RASn
DDR3A_RESETn
DDR3A_WEn
DDR3A_DQ[31:0]
DDR3A_DM[3:0]
DDR3A_DQS_P[3:0]
DDR3A_DQS_N[3:0]

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Title: Arria V SoC FPGA Development Kit Board

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Arria V ST Bank 4

U41B

Arria V SX (SoC) Bank 4

Bank 4A
2.5 Volt

SFPA_TXDISABLE	AP7	RZQ_1,DIFFIO_TX_B167_P,DQ22B	DIFFIO_TX_B146_N	AL9	SFPA_TXFAULT
SFPA_RATESEL0	AU6	DIFFIO_TX_B163_P,DQ22B	DIFFIO_TX_B148_N	AV7	SFPA_LOS
SFPA_RATESEL1	AL8	DIFFIO_TX_B165_P,DQ22B	DIFFIO_TX_B163_N	AT6	SFPB_TXDISABLE
			DIFFIO_TX_B165_N	AK8	SFPB_RATESEL0
SFPA_MOD0_PRSNTn	AR9	DIFFIO_RX_B153_P,DQ20B	DIFFIO_TX_B167_N	AN7	SFPB_RATESEL1
SFPA_MOD1_SCL	AT8	DIFFIO_RX_B153_N,DQ20B			
SFPA_MOD2_SDA	AH8	DQ21B			

Bank 4B
1.5 Volt

			HMC_DM5,DIFFIO_TX_B140_P	AU9	
		HMC_DQS5,HMC_RLD2_QK#5,HMC_QDR2_CQ5/CQ#5,DIFFIO_RX_B141_P		AH11	
		HMC_DQS#5,HMC_RLD2_QK5,DIFFIO_RX_B141_N		AG11	
DDR3B_DM2	AU12	HMC_DM3,DIFFIO_TX_B125_P			
DDR3B_DQS_P2	AW12	HMC_DQS3,HMC_RLD2_QK#3,HMC_QDR2_CQ3/CQ#3,DIFFIO_RX_B126_P			
DDR3B_DQS_N2	AV12	HMC_DQS#3,HMC_RLD2_QK3,DIFFIO_RX_B126_N			
DDR3B_DQ16	AJ13	HMC_DQ3_0,DIFFIO_RX_B130_P	HMC_DQ5_0,DIFFIO_RX_B145_P	AM10	
DDR3B_DQ17	AH13	HMC_DQ3_1,DIFFIO_RX_B130_N	HMC_DQ5_1,DIFFIO_RX_B145_N	AL10	
DDR3B_DQ18	AP12	HMC_DQ3_2,DIFFIO_TX_B129_P	HMC_DQ5_2,DIFFIO_TX_B144_P	AL11	
DDR3B_DQ19	AW11	HMC_DQ3_3,DIFFIO_RX_B128_P	HMC_DQ5_3,DIFFIO_RX_B143_P	AR10	
DDR3B_DQ20	AW10	HMC_DQ3_4,DIFFIO_RX_B128_N	HMC_DQ5_4,DIFFIO_RX_B143_N	AP10	
DDR3B_DQ21	AM13	HMC_DQ3_5,DIFFIO_TX_B127_P	HMC_DQ5_5,DIFFIO_TX_B142_P	AE12	
DDR3B_DQ22	AE13	HMC_DQ3_6,DIFFIO_RX_B124_P	HMC_DQ5_6,DIFFIO_RX_B139_P	AG12	
DDR3B_DQ23	AE14	HMC_DQ3_7,DIFFIO_RX_B124_N	HMC_DQ5_7,DIFFIO_RX_B139_N	AF12	
	AR13	HMC_DQ3_8,DIFFIO_TX_B123_P	HMC_DQ5_8,DIFFIO_TX_B138_P	AD11	
DDR3B_DM3	AV10	HMC_DM4,DIFFIO_TX_B133_P			
DDR3B_DQS_P3	AU11	HMC_DQS4,HMC_RLD2_QK#4,HMC_QDR2_CQ4/CQ#4,DIFFIO_RX_B134_P		AP13	
DDR3B_DQS_N3	AT11	HMC_DQS#4,HMC_RLD2_QK4,DIFFIO_RX_B134_N	DIFFIO_TX_B123_N	AT12	
			DIFFIO_TX_B125_N	AL13	
DDR3B_DQ24	AW9	HMC_DQ4_0,DIFFIO_RX_B137_P	DIFFIO_TX_B127_N	AN12	
DDR3B_DQ25	AV9	HMC_DQ4_1,DIFFIO_RX_B137_N	DIFFIO_TX_B129_N	AH12	
DDR3B_DQ26	AP11	HMC_DQ4_2,	DIFFIO_TX_B131_N	AU10	
DDR3B_DQ27	AD13	HMC_DQ4_3,DIFFIO_RX_B136_P	DIFFIO_TX_B133_N	AK12	
DDR3B_DQ28	AC13	HMC_DQ4_4,DIFFIO_RX_B136_N	DIFFIO_TX_B135_N	AC12	
DDR3B_DQ29	AL12	HMC_DQ4_5,DIFFIO_TX_B135_P	DIFFIO_TX_B138_N	AT9	
DDR3B_DQ30	AG13	HMC_DQ4_6,DIFFIO_RX_B132_P	DIFFIO_TX_B140_N	AD12	
DDR3B_DQ31	AF13	HMC_DQ4_7,DIFFIO_RX_B132_N	DIFFIO_TX_B142_N	AK11	
	AJ12	HMC_DQ4_8,DIFFIO_TX_B131_P	DIFFIO_TX_B144_N		

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U41P

Arria V SX (SoC) Bank 4

Bank 4C
1.5 Volt

			HMC_DM2,DIFFIO_TX_B117_P	AU13	DDR3B_DM1
		HMC_DQS2,HMC_RLD2_QK#2,HMC_QDR2_CQ2/CQ#2,DIFFIO_RX_B118_P		AF15	DDR3B_DQS_P1
		HMC_DQS#2,HMC_RLD2_QK2,DIFFIO_RX_B118_N		AE16	DDR3B_DQS_N1
DDR3B_DM0	AD16	HMC_DM1,DIFFIO_TX_B110_P			
DDR3B_DQS_P0	AH16	HMC_DQS1,HMC_RLD2_QK#1,HMC_QDR2_CQ1/CQ#1,DIFFIO_RX_B111_P			
DDR3B_DQS_N0	AG16	HMC_DQS#1,HMC_RLD2_QK1,DIFFIO_RX_B111_N	HMC_DQ2_8,DIFFIO_TX_B115_P	AD14	
DDR3B_DQ2	AH15	HMC_DQ1_2,	HMC_DQ2_6,DIFFIO_RX_B116_P	AU14	DDR3B_DQ14
	AP15	HMC_DQ1_8,DIFFIO_TX_B108_P	HMC_DQ2_7,DIFFIO_RX_B116_N	AT14	DDR3B_DQ15
DDR3B_DQ6	AW15	HMC_DQ1_6,DIFFIO_RX_B109_P	HMC_DQ2_5,DIFFIO_TX_B119_P	AL14	DDR3B_DQ13
DDR3B_DQ7	AW14	HMC_DQ1_7,DIFFIO_RX_B109_N	HMC_DQ2_3,DIFFIO_RX_B120_P	AP14	DDR3B_DQ11
DDR3B_DQ5	AL15	HMC_DQ1_5,DIFFIO_TX_B112_P	HMC_DQ2_4,DIFFIO_RX_B120_N	AN14	DDR3B_DQ12
DDR3B_DQ3	AW13	HMC_DQ1_3,DIFFIO_RX_B113_P	HMC_DQ2_2,DIFFIO_TX_B121_P	AH14	DDR3B_DQ10
DDR3B_DQ4	AV13	HMC_DQ1_4,DIFFIO_RX_B113_N	HMC_DQ2_0,DIFFIO_RX_B122_P	AE15	DDR3B_DQ8
DDR3B_DQ0	AU15	HMC_DQ1_0,DIFFIO_RX_B114_P	HMC_DQ2_1,DIFFIO_RX_B122_N	AD15	DDR3B_DQ9
DDR3B_DQ1	AT15	HMC_DQ1_1,DIFFIO_RX_B114_N			
			DIFFIO_TX_B115_N	AC15	
DDR3B_RESETn	AN15	HMC_RESET#,HMC_RLD2_A_19,DIFFIO_TX_B108_N	DIFFIO_TX_B117_N	AT13	
	AC16	DIFFIO_TX_B110_N	DIFFIO_TX_B119_N	AK14	
	AK15	DIFFIO_TX_B112_N	DIFFIO_TX_B121_N	AG14	

Bank 4D
1.5 Volt

			HMC_CK,DIFFIO_RX_B107_P	AF16	DDR3B_CLK_P
DDR3B_A0	AP16	HMC_A_0,DIFFIO_RX_B105_P	HMC_CK#,DIFFIO_RX_B107_N	AE17	DDR3B_CLK_N
DDR3B_A1	AN16	HMC_A_1,DIFFIO_RX_B105_N	HMC_CKE_0,HMC_RLD2_A_16,DIFFIO_TX_B106_P	AM16	DDR3B_CKE
DDR3B_A2	AK16	HMC_A_2,DIFFIO_TX_B104_P	HMC_CKE_1,HMC_RLD2_A_17,DIFFIO_TX_B106_N	AL16	
DDR3B_A3	AJ16	HMC_A_3,DIFFIO_TX_B104_N			
DDR3B_A4	AV16	HMC_A_4,DIFFIO_RX_B103_P	HMC_CS#_0,DIFFIO_TX_B93_P	AL17	DDR3B_CSn
DDR3B_A5	AU16	HMC_A_5,DIFFIO_RX_B103_N	HMC_CS#_1,DIFFIO_TX_B93_N	AK17	
DDR3B_A6	AT16	HMC_A_6,DIFFIO_TX_B102_P			
DDR3B_A7	AR16	HMC_A_7,DIFFIO_TX_B102_N	HMC_ODT_0,HMC_RLD2_A_18,DIFFIO_TX_B95_P	AD19	DDR3B_ODT
DDR3B_A8	AP17	HMC_A_8,DIFFIO_RX_B101_P	HMC_ODT_1,HMC_RLD2_A_20,DIFFIO_TX_B95_N	AC19	
DDR3B_A9	AN17	HMC_A_9,DIFFIO_RX_B101_N			
DDR3B_A10	AH17	HMC_A_10,DIFFIO_TX_B100_P			
			HMC_RAS#,HMC_RLD2_A_15,DIFFIO_TX_B97_N	AD17	DDR3B_RASn
			HMC_CAS#,HMC_RLD2_REF#,HMC_QDR2_WPS#,DIFFIO_RX_B96_P	AR18	DDR3B_CASn
			HMC_WE#,HMC_RLD2_WE#,HMC_QDR2_RPS#,DIFFIO_RX_B96_N	AP18	DDR3B_WEn
DDR3B_A11	AG17	HMC_A_11,DIFFIO_TX_B100_N	DIFFIO_TX_B85_P,DQ12B	AW18	
DDR3B_A12	AM18	HMC_A_12,DIFFIO_RX_B99_P	DIFFIO_RX_B86_P,DQ12B	AH19	
DDR3B_A13	AL18	HMC_A_13,DIFFIO_RX_B99_N	DIFFIO_TX_B87_P,DQ12B	AP19	
DDR3B_A14	AG18	HMC_A_14	DIFFIO_RX_B86_N,DQ12B	AG19	
	AU17	HMC_A_15,DIFFIO_RX_B94_P	DIFFIO_RX_B88_P,DQS12B	AL19	
DDR3B_BA0	AE18	HMC_BA_0,DIFFIO_RX_B98_P	DIFFIO_RX_B88_N,DQSn12B	AK19	
DDR3B_BA1	AD18	HMC_BA_1,DIFFIO_RX_B98_N	DIFFIO_TX_B89_P,DQ12B	AJ18	
DDR3B_BA2	AC18	HMC_BA_2,DIFFIO_RX_B97_P	DIFFIO_RX_B90_P,DQ12B	AT19	
			DIFFIO_RX_B90_N,DQ12B	AU18	
	AV18	DIFFIO_TX_B85_N	DIFFIO_TX_B91_P,DQ12B	AF19	
	AN19	DIFFIO_TX_B87_N	DIFFIO_RX_B92_P,DQ12B	AW16	
	AH18	DIFFIO_TX_B89_N	DIFFIO_RX_B92_N,DQ12B	AW17	
	AE19	DIFFIO_TX_B91_N	DIFFIO_RX_B94_N,DQ13B	AT17	

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SFPA_TXDISABLE — 22 — SFPA_TXDISABLE

SFPA_RATESEL0 — 22 — SFPA_RATESEL0
SFPA_RATESEL1 — 22 — SFPA_RATESEL1

SFPA_MOD0_PRSNTn — 22 — SFPA_MOD0_PRSNTn
SFPA_MOD1_SCL — 22 — SFPA_MOD1_SCL
SFPA_MOD2_SDA — 22 — SFPA_MOD2_SDA
SFPA_TXFAULT — 22 — SFPA_TXFAULT
SFPA_LOS — 22 — SFPA_LOS

SFPB_TXDISABLE — 23 — SFPB_TXDISABLE
SFPB_RATESEL0 — 23 — SFPB_RATESEL0
SFPB_RATESEL1 — 23 — SFPB_RATESEL1

DDR3B_A[14:0] — 17
DDR3B_BA[2:0] — 17
DDR3B_CASn — 17
DDR3B_CLK_P — 17
DDR3B_CLK_N — 17
DDR3B_CKE — 17
DDR3B_CSn — 17
DDR3B_ODT — 17
DDR3B_RASn — 17
DDR3B_RESETn — 17
DDR3B_WEn — 17

DDR3B_DQ[31:0] — 17
DDR3B_DM[3:0] — 17
DDR3B_DQS_P[3:0] — 17
DDR3B_DQS_N[3:0] — 17

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Arria V ST Bank 6 & 7G

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Arria V SX (SoC) Bank 7G

Bank 7G
Variable Voltage

	R19	DIFFIO_RX_T16_P	DIFFIO_RX_T19_P	P20	FMCB_GPIO4
	T19	DIFFIO_RX_T16_N	DIFFIO_RX_T19_N	R20	FMCB_GPIO5
FMCB_GPIO2	U19	DIFFIO_RX_T17_P	DIFFIO_RX_T21_P	L20	FMCB_GPIO6
FMCB_GPIO3	U20	DIFFIO_RX_T17_N	DIFFIO_RX_T21_N	M20	FMCB_GPIO7
FMCB_PRSNTn	L19	DIFFIO_TX_T18_P	DIFFIO_TX_T20_P	M19	FMCB_SDA
			IO	N19	FMCB_SCL

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U41C

Arria V SX (SoC) Bank 6

100, 1% R576 DDR3_HPS_RZQIN K9 — HPS_RZQ_0

Bank 6A
1.5 Volt

DDR3_HPS_A0	N9	HPS_A_0	HPS_DM_0	C6	DDR3_HPS_DM0
DDR3_HPS_A1	M9	HPS_A_1	HPS_DQS_0	F7	DDR3_HPS_DQS_P0
DDR3_HPS_A2	N10	HPS_A_2	HPS_DQS#_0	E7	DDR3_HPS_DQS_N0
DDR3_HPS_A3	M10	HPS_A_3			
DDR3_HPS_A4	A8	HPS_A_4	HPS_DQ_0	D7	DDR3_HPS_DQ0
DDR3_HPS_A5	B7	HPS_A_5	HPS_DQ_1	C7	DDR3_HPS_DQ1
DDR3_HPS_A6	B9	HPS_A_6	HPS_DQ_2	R10	DDR3_HPS_DQ2
DDR3_HPS_A7	A9	HPS_A_7	HPS_DQ_3	G7	DDR3_HPS_DQ3
DDR3_HPS_A8	D9	HPS_A_8	HPS_DQ_4	A6	DDR3_HPS_DQ4
DDR3_HPS_A9	C10	HPS_A_9	HPS_DQ_5	A7	DDR3_HPS_DQ5
DDR3_HPS_A10	K7	HPS_A_10	HPS_DQ_6	L6	DDR3_HPS_DQ6
DDR3_HPS_A11	J7	HPS_A_11	HPS_DQ_7	D6	DDR3_HPS_DQ7
DDR3_HPS_A12	F9	HPS_A_12			
DDR3_HPS_A13	E9	HPS_A_13			
DDR3_HPS_A14	D11	HPS_A_14	HPS_DM_1	E4	DDR3_HPS_DM1
	D10	HPS_A_15	HPS_DQS_1	D5	DDR3_HPS_DQS_P1
			HPS_DQS#_1	E6	DDR3_HPS_DQS_N1
DDR3_HPS_BA0	L7	HPS_BA_0			
DDR3_HPS_BA1	C9	HPS_BA_1	HPS_DQ_8	H6	DDR3_HPS_DQ8
DDR3_HPS_BA2	D8	HPS_BA_2	HPS_DQ_9	G6	DDR3_HPS_DQ9
			HPS_DQ_10	N8	DDR3_HPS_DQ10
DDR3_HPS_CLK_P	A11	HPS_CK	HPS_DQ_11	G5	DDR3_HPS_DQ11
DDR3_HPS_CLK_N	B10	HPS_CK#	HPS_DQ_12	A4	DDR3_HPS_DQ12
DDR3_HPS_CKE	R8	HPS_CKE_0	HPS_DQ_13	A5	DDR3_HPS_DQ13
	F5	HPS_CKE_1	HPS_DQ_14	R9	DDR3_HPS_DQ14
			HPS_DQ_15	F4	DDR3_HPS_DQ15
DDR3_HPS_CSn	H9	HPS_CS#_0			
	J9	HPS_CS#_1			
DDR3_HPS_ODT	H7	HPS_ODT_0			
	K6	HPS_ODT_1			
DDR3_HPS_RASn	G8	HPS_RAS#	HPS_GPI0	B6	
DDR3_HPS_CASn	G9	HPS_CAS#	HPS_GPI1	M7	
DDR3_HPS_WEn	J8	HPS_WE#	HPS_GPI2	B4	
			HPS_GPI3	C4	

Bank 6B
1.5 Volt

DDR3_HPS_DM2	D3	HPS_DM_2	HPS_DM_4	T7	DDR3_HPS_DM4
DDR3_HPS_DQS_P2	G4	HPS_DQS_2	HPS_DQS_4	J1	DDR3_HPS_DQS_P4
DDR3_HPS_DQS_N2	H4	HPS_DQS#_2	HPS_DQS#_4	H1	DDR3_HPS_DQS_N4
DDR3_HPS_DQ16	J5	HPS_DQ_16	HPS_DQ_32	G1	DDR3_HPS_DQ32
DDR3_HPS_DQ17	K5	HPS_DQ_17	HPS_DQ_33	F1	DDR3_HPS_DQ33
DDR3_HPS_DQ18	N7	HPS_DQ_18	HPS_DQ_34	P6	DDR3_HPS_DQ34
DDR3_HPS_DQ19	F3	HPS_DQ_19	HPS_DQ_35	L1	DDR3_HPS_DQ35
DDR3_HPS_DQ20	H3	HPS_DQ_20	HPS_DQ_36	M2	DDR3_HPS_DQ36
DDR3_HPS_DQ21	J4	HPS_DQ_21	HPS_DQ_37	M1	DDR3_HPS_DQ37
DDR3_HPS_DQ22	M5	HPS_DQ_22	HPS_DQ_38	N1	DDR3_HPS_DQ38
DDR3_HPS_DQ23	C3	HPS_DQ_23	HPS_DQ_39	R6	DDR3_HPS_DQ39
DDR3_HPS_DM3	D1	HPS_DM_3	HPS_RESET#	E3	DDR3_HPS_RESETn
DDR3_HPS_DQS_P3	C2	HPS_DQS_3		M6	
DDR3_HPS_DQS_N3	D2	HPS_DQS#_3	HPS_GPI4	L4	
DDR3_HPS_DQ24	A2	HPS_DQ_24	HPS_GPI5	K4	
DDR3_HPS_DQ25	A3	HPS_DQ_25	HPS_GPI6	K3	
DDR3_HPS_DQ26	P7	HPS_DQ_26	HPS_GPI7	N6	
DDR3_HPS_DQ27	C1	HPS_DQ_27	HPS_GPI8	B1	
DDR3_HPS_DQ28	G2	HPS_DQ_28	HPS_GPI9	K2	
DDR3_HPS_DQ29	F2	HPS_DQ_29	HPS_GPI10	J2	
DDR3_HPS_DQ30	M3	HPS_DQ_30	HPS_GPI11	R7	
DDR3_HPS_DQ31	E1	HPS_DQ_31	HPS_GPI12	K1	
			HPS_GPI13		

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DDR3_HPS_A[14:0] 15
DDR3_HPS_BA[2:0] 15
DDR3_HPS_CASn 15
DDR3_HPS_CLK_P 15
DDR3_HPS_CLK_N 15
DDR3_HPS_CKE 15
DDR3_HPS_CSn 15
DDR3_HPS_ODT 15
DDR3_HPS_RASn 15
DDR3_HPS_RESETn 15
DDR3_HPS_WEn 15

DDR3_HPS_DQ[39:0] 15
DDR3_HPS_DM[4:0] 15
DDR3_HPS_DQS_P[4:0] 15
DDR3_HPS_DQS_N[4:0] 15

FMC PORT B INTERFACE

FMCB_SDA 25
FMCB_SCL 25
FMCB_PRSNTn 25,28
FMCB_GPIO[7:0] 25

Si571 VCXO

SDI_CLK148_DN 4,9

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Arria V ST Bank 7

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Arria V SX (SoC) Bank 7

Bank 7A — 3.3 Volt

HPS_nRST		R11	SPIS0_SS0,HPS_GPIO70	D14	
HPS_nPOR		K10	SPIS0_MISO,HPS_GPIO69	J13	
HPS_PORSEL		C12	SPIS0_MOSI,HPS_GPIO68	C14	
			SPIS0_CLK,SPIM0_SS1,HPS_GPIO67	H13	
HPS_TMS	JTAG_HPS_TMS	F10	SPIM0_SS0,SPIM0_SS0,HPS_GPIO66	P13	
HPS_TCK	JTAG_HPS_TCK	G10	I2C1_SCL,SPIM0_MISO,HPS_GPIO65	M14	
HPS_TRST	JTAG_HPS_TRST	F11	I2C1_SDA,SPIM0_MOSI,HPS_GPIO64	R13	
HPS_TDI	JTAG_HPS_TDI	H10	UART1_TX,SPIM0_CLK,HPS_GPIO63	N13	UARTB_TX
HPS_TDO	JTAG_HPS_TDO	T11	UART1_RX,SPIM1_SS1,HPS_GPIO62	G13	UARTB_RX
			SPIS1_SS0,SPIM1_SS0,HPS_GPIO70	D13	
HPS_CLK1	CLK_OSC1	N11	SPIS1_MISO,SPIM1_MISO,HPS_GPIO69	F13	
HPS_CLK2	CLK_OSC2	D12	SPIS1_MOSI,SPIM1_MOSI,HPS_GPIO68	E13	
			SPIS1_CLK,SPIM1_CLK,HPS_GPIO67	L12	
			UART0_TX*,CLKSEL0,UART0_TX,SPIM1_SS0,HPS_GPIO66	M13	UARTA_TX
			UART0_RX*,UART0_RX,SPIM1_MISO,HPS_GPIO65	M12	UARTA_RX
TRACE_CLK,HPS_GPIO48	TRACE_CLK_MIC R564 0	J11	I2C0_SCL,UART1_TX,SPIM1_MOSI,HPS_GPIO64	L13	I2C_SCL_HPS
TRACE_D0,SPIS0_CLK,UART0_RX,HPS_GPIO49	TRACE_DATA0 R558 22	K12	I2C0_SDA,UART1_RX,SPIM1_CLK,HPS_GPIO63	C13	I2C_SDA_HPS
TRACE_D1,SPIS0_MOSI,UART0_TX,HPS_GPIO50	TRACE_DATA1 R563 22	K11	UART0_TX,CLKSEL1,SPIM1_SS1,HPS_GPIO62	A15	CLKSEL1
TRACE_D2,SPIS0_MISO,I2C1_SDA,HPS_GPIO51	TRACE_DATA2 R541 22	J12	UART0_RX,SPIM0_SS1,HPS_GPIO61	B14	
TRACE_D3,SPIS0_SS0,I2C1_SCL,HPS_GPIO52	TRACE_DATA3 22 R538	H12	SPIM0_SS0,BOOTSEL0,UART1_RTS,HPS_GPIO60	B15	BOOTSEL0
TRACE_D4,SPIS1_CLK,HPS_GPIO53	TRACE_DATA4 22 R547	E12	SPIM0_MISO,UART1_CTS,HPS_GPIO59	N12	
TRACE_D5,SPIS1_MOSI,HPS_GPIO54	TRACE_DATA5 22 R557	G11	SPIM0_MOSI,I2C1_SCL,UART0_RTS,HPS_GPIO58	A14	
TRACE_D6,SPIS1_SS0,I2C0_SDA,HPS_GPIO55	TRACE_DATA6 22 R540	F12	SPIM0_CLK,I2C1_SDA,UART0_CTS,HPS_GPIO57	P12	
TRACE_D7,SPIS1_MISO,I2C0_SCL,HPS_GPIO56	TRACE_DATA7 22 R546	A13			

Bank 7B — 3.3 Volt

	USER_LED_HPS3	C16	NAND_RE,RGMII1_TXD2,USB1_D2,HPS_GPIO17	R15	USER_LED_HPS2
NAND_RB,RGMII1_TXD3,USB1_D3,HPS_GPIO18		G14	NAND_CLE,RGMII1_TXD1,USB1_D1,HPS_GPIO16	A17	
NAND_DQ0,RGMII1_RXD0,HPS_GPIO19		B17	NAND_CE,RGMII1_TXD0,USB1_D0,HPS_GPIO15	P15	
NAND_DQ1,RGMII1_MDIO,I2C3_SDA,HPS_GPIO20		H14	NAND_ALE,RGMII1_TX_CLK,QSPI_SS3,HPS_GPIO14	A16	
NAND_DQ2,RGMII1_MDC,I2C3_SCL,HPS_GPIO21	USER_DIPSW_HPS0	L15	QSPI_IO0,USB1_CLK,HPS_GPIO29	D15	QSPI_IO0
NAND_DQ3,RGMII1_RX_CTL,USB1_D4,HPS_GPIO22		P14	QSPI_IO1,USB1_STP,HPS_GPIO30	G15	QSPI_IO1
NAND_DQ4,RGMII1_TX_CTL,USB1_D5,HPS_GPIO23	USER_DIPSW_HPS1	K15	QSPI_IO2,USB1_DIR,HPS_GPIO31	M15	QSPI_IO2
NAND_DQ5,RGMII1_RX_CLK,USB1_D6,HPS_GPIO24		R14	QSPI_IO3,USB1_NXT,HPS_GPIO32	H15	QSPI_IO3
NAND_DQ6,RGMII1_RXD1,USB1_D7,HPS_GPIO25	USER_DIPSW_HPS2	K14	QSPI_SS0,BOOTSEL1,HPS_GPIO33	N15	QSPI_SS0
NAND_DQ7,RGMII1_RXD2,HPS_GPIO26	USER_DIPSW_HPS3	C15	QSPI_CLK,HPS_GPIO34	F15	QSPI_CLK
NAND_WP,RGMII1_RXD3,QSPI_SS2,HPS_GPIO27	BOOTSEL2	L14	QSPI_SS1,HPS_GPIO35	E15	USER_PB_HPS0
NAND_WE,BOOTSEL2,QSPI_SS1,HPS_GPIO28					

Bank 7C — 3.3 Volt

SDMMC_CMD,USB0_D0,HPS_GPIO36	SD_CMD	D16	SDMMC_D4,USB0_D4,HPS_GPIO40	F16	USER_LED_HPS1
SDMMC_PWREN,USB0_D1,HPS_GPIO37		P16	SDMMC_D5,USB0_D5,HPS_GPIO41	G16	USER_PB_HPS1
SDMMC_D0,USB0_D2,HPS_GPIO38	SD_DAT0	C17	SDMMC_D6,USB0_D6,HPS_GPIO42	E16	USER_PB_HPS2
SDMMC_D1,USB0_D3,HPS_GPIO39	SD_DAT1	N16	SDMMC_D7,USB0_D7,HPS_GPIO43	H16	USER_PB_HPS3
SDMMC_D2,USB0_DIR,HPS_GPIO46	SD_DAT2	J16	SDMMC_FB_CLK_IN,USB0_CLK,HPS_GPIO44	K16	
SDMMC_D3,USB0_NXT,HPS_GPIO47	SD_CD_DAT3	M16	SDMMC_CCLK_OUT,USB0_STP,HPS_GPIO45	L16	SD_CLK

Bank 7D — 3.3 Volt

RGMII0_RXD0,USB1_D4,HPS_GPIO5	USB_DATA4	J17	RGMII0_TXD0,USB1_D0,HPS_GPIO1	F17	USB_DATA0
RGMII0_RXD1,USB1_STP,HPS_GPIO11	USB_STP	A19	RGMII0_TXD1,USB1_D1,HPS_GPIO2	P17	USB_DATA1
RGMII0_RXD2,USB1_DIR,HPS_GPIO12	USB_DIR	C19	RGMII0_TXD2,USB1_D2,HPS_GPIO3	F18	USB_DATA2
RGMII0_RXD3,USB1_NXT,HPS_GPIO13	USB_NXT	G18	RGMII0_TXD3,USB1_D3,HPS_GPIO4	E18	USB_DATA3
RGMII0_MDC ,USB1_D6,I2C2_SCL,HPS_GPIO7	USB_DATA6	K17	RGMII1_TX_CLK,HPS_GPIO48	D19	ENET_HPS_GTX_CLK
RGMII0_MDIO,USB1_D5,I2C2_SDA,HPS_GPIO6	USB_DATA5	D18	RGMII1_TX_CTL,HPS_GPIO51	N18	ENET_HPS_TX_EN
RGMII0_RX_CTL,USB1_D7,HPS_GPIO8	USB_DATA7	B19	RGMII1_RXD0,HPS_GPIO52	E19	ENET_HPS_RXD0
RGMII0_RX_CLK,USB1_CLK,HPS_GPIO10	USB_CLK	C18	RGMII1_RXD1,HPS_GPIO53	M17	ENET_HPS_RXD1
RGMII0_TX_CLK,HPS_GPIO0	USER_LED_HPS0	R17	RGMII1_TXD0,HPS_GPIO49	H18	ENET_HPS_TXD0
RGMII0_TX_CTL,HPS_GPIO9	ENET_HPS_INTn	A18	RGMII1_TXD1,HPS_GPIO50	F19	ENET_HPS_TXD1

Bank 7E — 3.3 Volt

RGMII1_MDC,SPIM0_MOSI,SPIS0_MOSI,HPS_GPIO55	ENET_HPS_MDC	L18	RGMII1_RXD2,SPIS1_MISO,SPIM1_MISO,HPS_GPIO60	G20	ENET_HPS_RXD2
RGMII1_MDIO,SPIM0_CLK,SPIS0_CLK,HPS_GPIO54	ENET_HPS_MDIO	J18	RGMII1_RXD3,SPIS1_SS0,SPIM1_SS0,HPS_GPIO61	G19	ENET_HPS_RXD3
RGMII1_RX_CLK,SPIS1_CLK,SPIM1_CLK,HPS_GPIO58	ENET_HPS_RX_CLK	G21	RGMII1_TXD2,SPIM0_MISO,SPIS0_MISO,HPS_GPIO56	K18	ENET_HPS_TXD2
RGMII1_RX_CTL,SPIS1_MOSI,SPIM1_MOSI,HPS_GPIO59	ENET_HPS_RX_DV	H19	RGMII1_TXD3,SPIM0_SS0,SPIS0_SS0,HPS_GPIO57	M18	ENET_HPS_TXD3

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3.3V — R551 4.70K, 1% — 2.5V_HPS — R550 4.70K, 1%

JTAG_HPS_TMS, JTAG_HPS_TCK, JTAG_HPS_TRST, JTAG_HPS_TDI, JTAG_HPS_TDO (14)

CLK_OSC1, CLK_OSC2 (11)

HEADER, 1x3-PIN J37: 1 10.0K R254 3.3V; 2 UARTA_TX; 3 1.00K R255 — CLKSEL0

HEADER, 1x3-PIN J38: 1 10.0K R256 3.3V; 2 CLKSEL1; 3 1.00K R257 — CLKSEL1

XJ8, XJ9 — 881545-2

JTAG_HPS_TCK — C849 39pF — R4001 37.4

3.3V — R75 4.70K, 1% JTAG_MICTOR_TMS — R76 4.70K, 1% JTAG_MICTOR_TDI

Micro SD / USB INTERFACE

USB_DATA[7..0] — 27 USB_DATA[7..0]

ETHERNET INTERFACE

ENET_HPS_TXD[3..0]	20	ENET_HPS_TXD[3..0]
ENET_HPS_GTX_CLK	20	ENET_HPS_GTX_CLK
ENET_HPS_TX_EN	20	ENET_HPS_TX_EN
ENET_HPS_MDC	20	ENET_HPS_MDC
ENET_HPS_RESETn	20,26	ENET_HPS_RESETn
ENET_HPS_RXD[3..0]	20	ENET_HPS_RXD[3..0]
ENET_HPS_RX_CLK	20	ENET_HPS_RX_CLK
ENET_HPS_RX_DV	20	ENET_HPS_RX_DV
ENET_HPS_MDIO	20	ENET_HPS_MDIO
ENET_HPS_INTn	20	ENET_HPS_INTn
HPS_RESETn	19,26	HPS_RESETn
USER_LED_HPS[3:0]	28	USER_LED_HPS[3:0]
USER_DIPSW_HPS[3:0]	28	USER_DIPSW_HPS[3:0]
USER_PB_HPS[3:0]	28	USER_PB_HPS[3:0]

3.3V — HEADER, 1x3-PIN J39: R258 10.0K 1; BOOTSEL0 2; R259 1.00K 3 — BOOTSEL0

3.3V — R260 10.0K — QSPI_SS0 2; R261 1.00K 3 — J40 — BOOTSEL1 — HEADER, 1x3-PIN

3.3V — R262 10.0K — BOOTSEL2 2; R263 1.00K 3 — J41 — BOOTSEL2 — HEADER, 1x3-PIN

3.3V — C242 2.2uF — C243 0.1uF

XJ10, XJ11, XJ12 — 881545-2

2.5V_REG_HPS — R150 4.70K, 1%

XJ4 J28: 1 JTAG_MIC_SEL; 2 — 881545-2 CON2

Logic 0 = pin 10 <--> pin 9 (TRST from JTAG)
Logic 1 = pin 10 <--> pin 2 (TRST from MICTOR)

Logic 0 = pin 6 <--> pin 7 (Bypass)
Logic 1 = pin 6 <--> pin 4 (Enable)

U67 — TS5A23157

JTAG_MIC_SEL	1	IN1	COM1 — 10 — MICTR_TRST — 0 R406 — JTAG_HPS_TRST
MICTOR_TRST	2	NO1	NC1 — 9 — JTAG_TRST — 14,19
	3	GND	V+ — 8 — 2.5V_REG_HPS — C320 0.1uF
	4	NO2	NC2 — 7
	5	IN2	COM2 — 6

MIC_34 R427 DNI; MIC_36 R430 DNI

3.3V — C73 0.1uF — C72 0.001uf

J17 — Mictor38P

1	5VDC	SCL	2
3	GND	SDA	4
5	CLKE	CLKO	6 — TRACE_CLK_MIC — R436 10.0K — R101 — 3.3V
7	D15E	D15O	8 — R397 10.0K — MICTOR_RSTn
9	D14E	D14O	10
11	D13E	D13O	12 — MICTOR_PWR1 — 0_Ohms
13	D12E	D12O	14 — MICTOR_PWR2 — DNI
15	D11E	D11O	16 — TRACE_DATA7 — R100
17	D10E	D10O	18 — TRACE_DATA6
19	D9E	D9O	20 — TRACE_DATA5
21	D8E	D8O	22 — TRACE_DATA4
23	D7E	D7O	24 — TRACE_DATA3
25	D6E	D6O	26 — TRACE_DATA2
27	D5E	D5O	28 — TRACE_DATA1
29	D4E	D4O	30 — R425 10K
31	D3E	D3O	32 — R426 10K
33	D2E	D2O	34 — MIC_34 R428 10K — 3.3V
35	D1E	D1O	36 — MIC_36 R429 10K
37	D0E	D0O	38 — TRACE_DATA0
		GND1	39
		GND2	40
		GND3	41
		GND4	42
		GND5	43

MICTOR_RSTn 14,19,26; JTAG_MICTOR_TDI 14; JTAG_MICTOR_TCK 14; JTAG_MICTOR_TMS 14; JTAG_MICTOR_TDO 14; MICTOR_TRST

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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Arria V ST Bank 8

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Arria V SX (SoC) Bank 8

Bank 8A
Variable Voltage

FMCB_LA_TX_N9	F33	RZQ_6,DIFFIO_TX_T114_N	
FMCB_LA_RX_P0	B31		HMC_BA_0,DIFFIO_RX_T102_P
FMCB_LA_RX_N0	A30		HMC_BA_1,DIFFIO_RX_T102_N
FMCB_LA_TX_P0	A31	HMC_A_0,DIFFIO_RX_T94_P	HMC_BA_2,DIFFIO_TX_T103_P
FMCB_LA_TX_N0	A32	HMC_A_1,DIFFIO_RX_T94_N	
FMCB_LA_RX_P1	A33	HMC_A_2,DIFFIO_RX_T95_P	
FMCB_LA_RX_N1	B33	HMC_A_3,DIFFIO_TX_T95_N	HMC_CK,DIFFIO_RX_T92_P
FMCB_LA_TX_P1	H31	HMC_A_4,DIFFIO_RX_T96_P	HMC_CK#,DIFFIO_RX_T92_N
FMCB_LA_TX_N1	J31	HMC_A_5,DIFFIO_RX_T96_N	HMC_CKE_0,HMC_RLD2_A_16,DIFFIO_TX_T93_P
FMCB_LA_RX_P2	C31	HMC_A_6,DIFFIO_TX_T97_P	HMC_CKE_1,HMC_RLD2_A_17,DIFFIO_TX_T93_N
FMCB_LA_RX_N2	D31	HMC_A_7,DIFFIO_TX_T97_N	
FMCB_LA_TX_P2	C32	HMC_A_8,DIFFIO_RX_T98_P	HMC_CS#_0,DIFFIO_TX_T107_P
FMCB_LA_TX_N2	D32	HMC_A_9,DIFFIO_RX_T98_N	HMC_CS#_1,DIFFIO_TX_T107_N
FMCB_LA_RX_P3	N31	HMC_A_10,DIFFIO_TX_T99_P	HMC_ODT_0,HMC_RLD2_A_18,DIFFIO_TX_T105_P
FMCB_LA_RX_N3	P31	HMC_A_11,DIFFIO_TX_T99_N	HMC_ODT_1,HMC_RLD2_A_20,DIFFIO_TX_T105_N
		HMC_A_12,DIFFIO_RX_T100_P	
		HMC_A_13,DIFFIO_RX_T100_N	HMC_RAS#,HMC_RLD2_A_21,DIFFIO_TX_T103_N
			HMC_CAS#,HMC_RLD2_REF#,HMC_QDR2_WPS#,DIFFIO_RX_T104_P
			HMC_WE#,HMC_RLD2_WE#,HMC_QDR2_RPS#,DIFFIO_RX_T104_N
FMCB_LA_TX_P3	J32		
FMCB_LA_TX_N3	K32	HMC_A_14,DIFFIO_TX_T101_P	DQ11T
		HMC_A_15,DIFFIO_TX_T101_N	DIFFIO_TX_T112_P,DQ11T
FMCB_GPIO1	G32		DIFFIO_TX_T114_P,DQ11T
		DIFFIO_TX_T112_N	

Bank 8B
Variable Voltage

FMCB_LA_TX_P10	J30	HMC_DM1,DIFFIO_TX_T89_P	
FMCB_LA_RX_P8	N30	HMC_DQS1,HMC_RLD2_QK#1,HMC_QDR2_CQ1/CQ#1,DIFFIO_RX_T88_P	
FMCB_LA_RX_N8	P30	HMC_DQS#1,HMC_RLD2_QK1,DIFFIO_RX_T88_N	
			HMC_DM2,DIFFIO_TX_T82_P
			HMC_DQS2,HMC_RLD2_QK#2,HMC_QDR2_CQ2/CQ#2,DIFFIO_RX_T81_P
			HMC_DQS#2,HMC_RLD2_QK2,DIFFIO_RX_T81_N
FMCB_LA_RX_P9	B28	HMC_DQ1_0,DIFFIO_RX_T85_P	
FMCB_LA_RX_N9	C29	HMC_DQ1_1,DIFFIO_RX_T85_N	HMC_DQ2_0,DIFFIO_RX_T77_P
FMCB_GA1	R30	HMC_DQ1_2	HMC_DQ2_1,DIFFIO_RX_T77_N
FMCB_LA_RX_P10	A29	HMC_DQ1_3,DIFFIO_RX_T86_P	HMC_DQ2_2,DIFFIO_RX_T78_P
FMCB_LA_RX_N10	A28	HMC_DQ1_4,DIFFIO_RX_T86_N	HMC_DQ2_3,DIFFIO_RX_T79_P
FMCB_LA_TX_CLK_P	L30	HMC_DQ1_5,DIFFIO_TX_T87_P	HMC_DQ2_4,DIFFIO_RX_T79_N
FMCB_LA_RX_P11	D30	HMC_DQ1_6,DIFFIO_RX_T90_P	HMC_DQ2_5,DIFFIO_TX_T80_P
FMCB_LA_RX_N11	D29	HMC_DQ1_7,DIFFIO_RX_T90_N	HMC_DQ2_6,DIFFIO_RX_T83_P
FMCB_LA_TX_P12	F30	HMC_DQ1_8,DIFFIO_TX_T91_P	HMC_DQ2_7,DIFFIO_RX_T83_N
			HMC_DQ2_8,DIFFIO_TX_T84_P
FMCB_LA_TX_N12	G30	HMC_RESET#,HMC_RLD2_A_19,DIFFIO_TX_T91_N	
			DIFFIO_TX_T78_N
FMCB_LA_TX_CLK_N	M30	DIFFIO_TX_T87_N	DIFFIO_TX_T80_N
FMCB_LA_TX_N10	K30	DIFFIO_TX_T89_N	DIFFIO_TX_T82_N
			DIFFIO_TX_T84_N

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M32	FMCB_LA_RX_P4		
N32	FMCB_LA_RX_N4		
J34	FMCB_LA_TX_P4		
B30	FMCB_LA_RX_P5		
C30	FMCB_LA_RX_N5		
E31	FMCB_LA_TX_P5		
F31	FMCB_LA_TX_N5		
L34	FMCB_LA_TX_P6		
M34	FMCB_LA_TX_N6		
L31	FMCB_LA_TX_P7		
M31	FMCB_LA_TX_N7		
K34	FMCB_LA_TX_N4		
L33	FMCB_LA_RX_P6		
M33	FMCB_LA_RX_N6		
J33	FMCB_GA0		
F32	FMCB_GPIO0		
E33	FMCB_LA_TX_P9		
J29	FMCB_LA_TX_P16		
R29	FMCB_LA_RX_P12		
T29	FMCB_LA_RX_N12		
L28	USB_FPGA_WR		
M28	USB_FPGA_RDn		
H28	FMCB_LA_TX_P13		
C28	FMCB_LA_RX_P14		
D28	FMCB_LA_RX_N14		
F28	FMCB_LA_TX_P14		
M29	FMCB_LA_RX_P15		
N29	FMCB_LA_RX_N15		
F29	FMCB_LA_TX_P15		
J28	FMCB_LA_TX_N13		
G28	FMCB_LA_TX_N14		
K29	FMCB_LA_TX_N16		
G29	FMCB_LA_TX_N15		

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Arria V SX (SoC) Bank 8

Bank 8C
Variable Voltage

FMC_LA_TX_P6	K27	HMC_DM3,DIFFIO_TX_T74_P	
FMC_LA_RX_P0	R28	HMC_DQS3,HMC_RLD2_QK#3,HMC_QDR2_CQ3/CQ#3,DIFFIO_RX_T73_P	
FMC_LA_RX_N0	T28	HMC_DQS#3,HMC_RLD2_QK3,DIFFIO_RX_T73_N	
			HMC_DM5,DIFFIO_TX_T59_P
			HMC_DQS5,HMC_RLD2_QK#5,HMC_QDR2_CQ5/CQ#5,DIFFIO_RX_T58_P
			HMC_DQS#5,HMC_RLD2_QK5,DIFFIO_RX_T58_N
FMC_LA_RX_P1	P27	HMC_DQ3_0,DIFFIO_RX_T69_P	
FMC_LA_RX_N1	R27	HMC_DQ3_1,DIFFIO_RX_T69_N	HMC_DQ5_0,DIFFIO_RX_T54_P
FMC_LA_TX_P0	H27	HMC_DQ3_2,DIFFIO_TX_T70_P	HMC_DQ5_1,DIFFIO_RX_T54_N
FMC_GPIO6	B27	HMC_DQ3_3,DIFFIO_RX_T71_P	HMC_DQ5_2,DIFFIO_TX_T55_P
FMC_GPIO7	C27	HMC_DQ3_4,DIFFIO_RX_T71_N	HMC_DQ5_3,DIFFIO_RX_T56_P
FMC_LA_TX_P2	E27	HMC_DQ3_5,DIFFIO_TX_T72_P	HMC_DQ5_4,DIFFIO_RX_T56_N
FMC_LA_RX_P2	M27	HMC_DQ3_6,DIFFIO_RX_T75_P	HMC_DQ5_5,DIFFIO_TX_T57_P
FMC_LA_RX_N2	N27	HMC_DQ3_7,DIFFIO_RX_T75_N	HMC_DQ5_6,DIFFIO_RX_T60_P
FMC_LA_TX_P3	N28	HMC_DQ3_8,DIFFIO_TX_T76_P	HMC_DQ5_7,DIFFIO_RX_T60_N
			HMC_DQ5_8,DIFFIO_TX_T61_P
FMC_LA_TX_P1	J26	HMC_DM4,DIFFIO_TX_T66_P	
FMC_LA_RX_P3	M26	HMC_DQS4,HMC_RLD2_QK#4,HMC_QDR2_CQ4/CQ#4,DIFFIO_RX_T65_P	
FMC_LA_RX_N3	N26	HMC_DQS#4,HMC_RLD2_QK4,DIFFIO_RX_T65_N	DIFFIO_TX_T55_N
FMC_LA_RX_P4	C26	HMC_DQ4_0,DIFFIO_RX_T62_P	DIFFIO_TX_T57_N
FMC_LA_RX_N4	D26	HMC_DQ4_1,DIFFIO_RX_T62_N	DIFFIO_TX_T59_N
FMC_PRSNTn	K25	HMC_DQ4_2	DIFFIO_TX_T61_N
FMC_LA_RX_P5	R26	HMC_DQ4_3,DIFFIO_RX_T63_P	DIFFIO_TX_T64_N
FMC_LA_RX_N5	T27	HMC_DQ4_4,DIFFIO_RX_T63_N	DIFFIO_TX_T66_N
FMC_LA_TX_P4	A26	HMC_DQ4_5,DIFFIO_TX_T64_P	DIFFIO_TX_T68_N
FMC_LA_RX_P6	F26	HMC_DQ4_6,DIFFIO_RX_T67_P	DIFFIO_TX_T70_N
FMC_LA_RX_N6	G26	HMC_DQ4_7,DIFFIO_RX_T67_N	DIFFIO_TX_T72_N
FMC_LA_TX_P5	M25	HMC_DQ4_8,DIFFIO_TX_T68_P	DIFFIO_TX_T74_N
			DIFFIO_TX_T76_N

Bank 8D
Variable Voltage

FMC_LA_TX_P7	N21	DIFFIO_TX_T32_P,DQ1T	
USB_FPGA_DATA0	D21	DIFFIO_TX_T34_P,DQ1T	DIFFIO_RX_T50_P,DQS3T
FMC_LA_TX_P9	R21	DIFFIO_TX_T38_P,DQ1T	DIFFIO_RX_T50_N,DQSn3T
FMC_GA0	C23	DIFFIO_RX_T42_P,DQS2T	DIFFIO_RX_T46_P,DQ3T
FMC_SDA	D23	DIFFIO_RX_T42_N,DQSn2T	DIFFIO_RX_T46_N,DQ3T
FMC_SCL	J22		DIFFIO_TX_T47_P,DQ3T
FMC_LA_RX_P8	E22	DQ2T	DIFFIO_RX_T48_P,DQ3T
FMC_LA_RX_N8	F22	DIFFIO_RX_T40_P,DQ2T	DIFFIO_RX_T48_N,DQ3T
FMC_LA_TX_P10	A23	DIFFIO_RX_T40_N,DQ2T	DIFFIO_TX_T49_P,DQ3T
USB_FPGA_DATA1	L22	DIFFIO_TX_T41_P,DQ2T	DIFFIO_TX_T51_P,DQ3T
FMC_LA_RX_P9	N22	DIFFIO_TX_T43_P,DQ2T	DIFFIO_RX_T52_P,DQ3T
FMC_LA_RX_N9	P22	DIFFIO_RX_T44_P,DQ2T	DIFFIO_TX_T53_P,DQ3T
FMC_LA_TX_P12	R22	DIFFIO_RX_T44_N,DQ2T	DIFFIO_RX_T52_N,DQ3T
		DIFFIO_TX_T45_P,DQ2T	
FMC_LA_TX_N7	P21	DIFFIO_TX_T32_N	DIFFIO_TX_T47_N
USB_FPGA_DATA2	E21	DIFFIO_TX_T34_N	DIFFIO_TX_T49_N
FMC_LA_TX_N9	T21	DIFFIO_TX_T38_N	DIFFIO_TX_T51_N
FMC_LA_TX_N10	A24	DIFFIO_TX_T41_N	DIFFIO_TX_T53_N
USB_FPGA_DATA3	M22	DIFFIO_TX_T43_N	
FMC_LA_TX_N12	T22	DIFFIO_TX_T45_N	

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K24	FMC_LA_TX_P13		
A25	FMC_LA_RX_P10		
B25	FMC_LA_RX_N10		
T26	FMC_LA_RX_P11		
T25	FMC_LA_RX_N11		
G25	FMC_LA_TX_P14		
N24	FMC_LA_RX_P12		
P24	FMC_LA_RX_N12		
R24	FMC_LA_TX_P15		
D25	FMC_LA_RX_P13		
E25	FMC_LA_RX_N13		
P25	FMC_GA1		
H25	FMC_LA_TX_N14		
T24	FMC_LA_TX_N15		
L24	FMC_LA_TX_N13		
R25	USB_FPGA_TXEn		
A27	FMC_LA_TX_N4		
K26	FMC_LA_TX_N1		
N25	FMC_LA_TX_N5		
J27	FMC_LA_TX_N0		
F27	FMC_LA_TX_N2		
L27	FMC_LA_TX_N6		
P28	FMC_LA_TX_N3		
D24	FMC_LA_RX_P14		
E24	FMC_LA_RX_N14		
F23	FMC_LA_RX_P15		
G23	FMC_LA_RX_N15		
R23	FMC_LA_TX_P16		
B24	FMC_GPIO0		
C24	FMC_GPIO1		
M23	FMC_LA_TX_CLK_P		
J23	FMC_LA_TX_P17		
F24	FMC_GPIO2		
H24	FMC_GPIO4		
G24	FMC_GPIO3		
T23	FMC_LA_TX_N16		
N23	FMC_LA_TX_CLK_N		
K23	FMC_LA_TX_N17		
J24	FMC_GPIO5		

FMC PORT A INTERFACE

FMC_SDA	24
FMC_SCL	24
FMC_PRSNTn	24,28
FMC_LA_TX_CLK_P	24
FMC_LA_TX_CLK_N	24
FMC_LA_TX_P[17:0]	24
FMC_LA_TX_N[17:0]	24
FMC_LA_RX_P[15:0]	10,24
FMC_LA_RX_N[15:0]	10,24
FMC_GA[1:0]	24
FMC_GPIO[7:0]	24

USB FPGA INTERFACE

USB_FPGA_DATA[7..0]	10,27
USB_FPGA_WR	27
USB_FPGA_RDn	27
USB_FPGA_TXEn	27

FMC PORT B INTERFACE

FMCB_LA_TX_P[17:0]	10,25
FMCB_LA_TX_N[17:0]	10,25
FMCB_LA_RX_P[15:0]	10,25
FMCB_LA_RX_N[15:0]	10,25
FMCB_GA[1:0]	25
FMCB_LA_TX_CLK_P	25
FMCB_LA_TX_CLK_N	25
FMCB_GPIO[7:0]	6,25

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Arria V ST Transceivers

FMCB_DP_M2C_P[3:0] 25
FMCB_DP_M2C_N[3:0] 25
FMCB_DP_C2M_P[3:0] 25
FMCB_DP_C2M_N[3:0] 25

FMC_DP_M2C_P[7:0] 24
FMC_DP_M2C_N[7:0] 24
FMC_DP_C2M_P[7:0] 24
FMC_DP_C2M_N[7:0] 24

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Arria V SX (SoC) Transceiver - Left

GXB_L0

FMCB_DP_M2C_P0	AW37	GXB_RX_L0p,GXB_REFCLK_L0p	GXB_TX_L0p	AU37	FMCB_DP_C2M_P0
FMCB_DP_M2C_N0	AW36	GXB_RX_L0n,GXB_REFCLK_L0n	GXB_TX_L0n	AU36	FMCB_DP_C2M_N0
	AT39	GXB_RX_L1p,GXB_REFCLK_L1p	GXB_TX_L1p	AR37	
	AT38	GXB_RX_L1n,GXB_REFCLK_L1n	GXB_TX_L1n	AR36	
FMCB_DP_M2C_P1	AP39	GXB_RX_L2p,GXB_REFCLK_L2p	GXB_TX_L2p	AN37	FMCB_DP_C2M_P1
FMCB_DP_M2C_N1	AP38	GXB_RX_L2n,GXB_REFCLK_L2n	GXB_TX_L2n	AN36	FMCB_DP_C2M_N1
FMCB_DP_M2C_P2	AM39	GXB_RX_L3p,GXB_REFCLK_L3p	GXB_TX_L3p	AL37	FMCB_DP_C2M_P2
FMCB_DP_M2C_N2	AM38	GXB_RX_L3n,GXB_REFCLK_L3n	GXB_TX_L3n	AL36	FMCB_DP_C2M_N2
	AK39	GXB_RX_L4p,GXB_REFCLK_L4p	GXB_TX_L4p	AJ37	
	AK38	GXB_RX_L4n,GXB_REFCLK_L4n	GXB_TX_L4n	AJ36	
FMCB_DP_M2C_P3	AH39	GXB_RX_L5p,GXB_REFCLK_L5p	GXB_TX_L5p	AG37	FMCB_DP_C2M_P3
FMCB_DP_M2C_N3	AH38	GXB_RX_L5n,GXB_REFCLK_L5n	GXB_TX_L5n	AG36	FMCB_DP_C2M_N3
25 FMCB_GBTCLK_M2C_P0	AG32	REFCLK0Lp			
25 FMCB_GBTCLK_M2C_N0	AG33	REFCLK0Ln			
25 FMCB_GBTCLK_M2C_P1	AE31	REFCLK1Lp			
25 FMCB_GBTCLK_M2C_N1	AE32	REFCLK1Ln			

GXB_L1

FMC_DP_M2C_P0	AF39	GXB_RX_L6p,GXB_REFCLK_L6p	GXB_TX_L6p	AE37	FMC_DP_C2M_P0
FMC_DP_M2C_N0	AF38	GXB_RX_L6n,GXB_REFCLK_L6n	GXB_TX_L6n	AE36	FMC_DP_C2M_N0
	AD39	GXB_RX_L7p,GXB_REFCLK_L7p	GXB_TX_L7p	AC37	
	AD38	GXB_RX_L7n,GXB_REFCLK_L7n	GXB_TX_L7n	AC36	
FMC_DP_M2C_P1	AB39	GXB_RX_L8p,GXB_REFCLK_L8p	GXB_TX_L8p	AA37	FMC_DP_C2M_P1
FMC_DP_M2C_N1	AB38	GXB_RX_L8n,GXB_REFCLK_L8n	GXB_TX_L8n	AA36	FMC_DP_C2M_N1
FMC_DP_M2C_P2	Y39	GXB_RX_L9p,GXB_REFCLK_L9p	GXB_TX_L9p	W37	FMC_DP_C2M_P2
FMC_DP_M2C_N2	Y38	GXB_RX_L9n,GXB_REFCLK_L9n	GXB_TX_L9n	W36	FMC_DP_C2M_N2
	V39	GXB_RX_L10p,GXB_REFCLK_L10p	GXB_TX_L10p	U37	
	V38	GXB_RX_L10n,GXB_REFCLK_L10n	GXB_TX_L10n	U36	
FMC_DP_M2C_P3	T39	GXB_RX_L11p,GXB_REFCLK_L11p	GXB_TX_L11p	R37	FMC_DP_C2M_P3
FMC_DP_M2C_N3	T38	GXB_RX_L11n,GXB_REFCLK_L11n	GXB_TX_L11n	R36	FMC_DP_C2M_N3
24 FMC_GBTCLK_M2C_P0	AC31	REFCLK2Lp			
24 FMC_GBTCLK_M2C_N0	AC32	REFCLK2Ln			
24 FMC_GBTCLK_M2C_P1	AA31	REFCLK3Lp			
24 FMC_GBTCLK_M2C_N1	AA32	REFCLK3Ln			

GXB_L2

FMC_DP_M2C_P4	P39	GXB_RX_L12p,GXB_REFCLK_L12p	GXB_TX_L12p	N37	FMC_DP_C2M_P4
FMC_DP_M2C_N4	P38	GXB_RX_L12n,GXB_REFCLK_L12n	GXB_TX_L12n	N36	FMC_DP_C2M_N4
	M39	GXB_RX_L13p,GXB_REFCLK_L13p	GXB_TX_L13p	L37	
	M38	GXB_RX_L13n,GXB_REFCLK_L13n	GXB_TX_L13n	L36	
FMC_DP_M2C_P5	K39	GXB_RX_L14p,GXB_REFCLK_L14p	GXB_TX_L14p	J37	FMC_DP_C2M_P5
FMC_DP_M2C_N5	K38	GXB_RX_L14n,GXB_REFCLK_L14n	GXB_TX_L14n	J36	FMC_DP_C2M_N5
FMC_DP_M2C_P6	H39	GXB_RX_L15p,GXB_REFCLK_L15p	GXB_TX_L15p	G37	FMC_DP_C2M_P6
FMC_DP_M2C_N6	H38	GXB_RX_L15n,GXB_REFCLK_L15n	GXB_TX_L15n	G36	FMC_DP_C2M_N6
	F39	GXB_RX_L16p,GXB_REFCLK_L16p	GXB_TX_L16p	E37	
	F38	GXB_RX_L16n,GXB_REFCLK_L16n	GXB_TX_L16n	E36	
FMC_DP_M2C_P7	D39	GXB_RX_L17p,GXB_REFCLK_L17p	GXB_TX_L17p	C37	FMC_DP_C2M_P7
FMC_DP_M2C_N7	D38	GXB_RX_L17n,GXB_REFCLK_L17n	GXB_TX_L17n	C36	FMC_DP_C2M_N7
12 LMK_FMCCLK_P	W31	REFCLK4Lp			
12 LMK_FMCCLK_N	W32	REFCLK4Ln			
CLK_148_P	U31	REFCLK5Lp			
CLK_148_N	U32	REFCLK5Ln	RREF_TL	B39	XCVR_RREF_TL

5ASTFD5K3_F1517

R505 2.00K 1%

CAD Note:
Place resistor near RREF_TL pins.
Route away frm aggressor

U41R

Arria V SX (SoC) Transceiver - Right

GXB_R0

3 PCIE_RX_P0	AU1	GXB_RX_R0p,GXB_REFCLK_R0p	GXB_TX_R0p	AT3	PCIE_TX_P0 3
3 PCIE_RX_N0	AU2	GXB_RX_R0n,GXB_REFCLK_R0n	GXB_TX_R0n	AT4	PCIE_TX_N0 3
3 PCIE_RX_P1	AR1	GXB_RX_R1p,GXB_REFCLK_R1p	GXB_TX_R1p	AP3	PCIE_TX_P1 3
3 PCIE_RX_N1	AR2	GXB_RX_R1n,GXB_REFCLK_R1n	GXB_TX_R1n	AP4	PCIE_TX_N1 3
3 PCIE_RX_P2	AN1	GXB_RX_R2p,GXB_REFCLK_R2p	GXB_TX_R2p	AM3	PCIE_TX_P2 3
3 PCIE_RX_N2	AN2	GXB_RX_R2n,GXB_REFCLK_R2n	GXB_TX_R2n	AM4	PCIE_TX_N2 3
3 PCIE_RX_P3	AL1	GXB_RX_R3p,GXB_REFCLK_R3p	GXB_TX_R3p	AK3	PCIE_TX_P3 3
3 PCIE_RX_N3	AL2	GXB_RX_R3n,GXB_REFCLK_R3n	GXB_TX_R3n	AK4	PCIE_TX_N3 3
	AJ1	GXB_RX_R4p,GXB_REFCLK_R4p	GXB_TX_R4p	AH3	
	AJ2	GXB_RX_R4n,GXB_REFCLK_R4n	GXB_TX_R4n	AH4	CMU PLL (PCIe)
	AG1	GXB_RX_R5p,GXB_REFCLK_R5p	GXB_TX_R5p	AF3	
	AG2	GXB_RX_R5n,GXB_REFCLK_R5n	GXB_TX_R5n	AF4	
11 PCIE_REFCLK_QR0_P	AF8	REFCLK0Rp			
11 PCIE_REFCLK_QR0_N	AF7	REFCLK0Rn			
	AD9	REFCLK1Rp			
R593 10.0K	AD8	REFCLK1Rn			

GXB_R1

22 SFPA_RX_P	AE1	GXB_RX_R6p,GXB_REFCLK_R6p	GXB_TX_R6p	AD3	SFPA_TX_P 22
22 SFPA_RX_N	AE2	GXB_RX_R6n,GXB_REFCLK_R6n	GXB_TX_R6n	AD4	SFPA_TX_N 22
	AC1	GXB_RX_R7p,GXB_REFCLK_R7p	GXB_TX_R7p	AB3	
	AC2	GXB_RX_R7n,GXB_REFCLK_R7n	GXB_TX_R7n	AB4	
23 SFPB_RX_P	AA1	GXB_RX_R8p,GXB_REFCLK_R8p	GXB_TX_R8p	Y3	SFPB_TX_P 23
23 SFPB_RX_N	AA2	GXB_RX_R8n,GXB_REFCLK_R8n	GXB_TX_R8n	Y4	SFPB_TX_N 23
SMA_XCVR_RX_P	W1	GXB_RX_R9p,GXB_REFCLK_R9p	GXB_TX_R9p	V3	SMA_XCVR_TX_P
SMA_XCVR_RX_N	W2	GXB_RX_R9n,GXB_REFCLK_R9n	GXB_TX_R9n	V4	SMA_XCVR_TX_N
	U1	GXB_RX_R10p,GXB_REFCLK_R10p	GXB_TX_R10p	T3	
	U2	GXB_RX_R10n,GXB_REFCLK_R10n	GXB_TX_R10n	T4	
	R1	GXB_RX_R11p,GXB_REFCLK_R11p	GXB_TX_R11p	P3	
	R2	GXB_RX_R11n,GXB_REFCLK_R11n	GXB_TX_R11n	P4	
12 LMK_SFPCLK_P	AB9	REFCLK2Rp			
12 LMK_SFPCLK_N	AB8	REFCLK2Rn			
11 REFCLK_QR2_P	Y9	REFCLK3Rp			
11 REFCLK_QR2_N	Y8	REFCLK3Rn	RREF_BR	AW2	XCVR_RREF_BR

5ASTFD5K3_F1517

R575 2.00K 1%

CAD Note:
Place resistor near RREF_TL pins.
Route away frm aggressor

SMA_XCVR_RX_P C150 0.1uF SMA_XCVR_RX_C_P
SMA_XCVR_RX_N C151 0.1uF SMA_XCVR_RX_C_N

RX
SMA Connector Interface

J31
J32

TX
SMA Connector
Interface

J24
J25

SDI Reference Clocks

2.5V_REG_HPS
R120 10.0K
C114 0.1uF
C117 10uF

From MAXV
19 SI571_EN
11,19 I2C_SDA_MAX
11,19 I2C_SCL_MAX

X3 Si571
OE (2) VDD (6)
SDA (7) CLK+ (4) CLK_148_CP C115 0.1uF CLK_148_P
SCL (8) CLK- (5) CLK_148_CN C116 0.1uF CLK_148_N
GND (3) VC (1) SI571_VCONTROL

LVDS

Si571 Programmable Oscillator
Use Clock Control GUI
(Default 148.5MHz)
I2C Address 55 HEX

4 SDI_CLK148_UP R127 4.99K C112 1000pF

From FPGA
4 SDI_CLK148_DN R129 4.99K R126 180K C104 0.1uF

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Arria V ST Clocks

24 FMC_CLK_M2C_P[1:0]
24 FMC_CLK_M2C_N[1:0]
25 FMCB_CLK_M2C_P[1:0]
25 FMCB_CLK_M2C_N[1:0]

U41N

Arria V SX (SoC) Clocks

Bank 3A
1.5 Volt

CLK_BOT1 11 → CLK_BOT1 AP34 / AN34 → CLK0_P,DIFFIO_RX_B2_P,DQ1B / CLK0_N,DIFFIO_RX_B2_N,DQ1B
CLK_TOP1 11 → CLK_TOP1 AK34 / AJ34 → CLK1_P,DIFFIO_RX_B4_P,DQS1B / CLK1_N,DIFFIO_RX_B4_N,DQSn1B
CLK_ENET_FPGA_PHY → CLK_ENET_FPGA_PHY AM33 / AL33 → CLK2_P,DIFFIO_RX_B7_P,DQ1B / CLK2_N,DIFFIO_RX_B7_N,DQ1B
CLK_50M_FPGA 11 → CLK_50M_FPGA AU32 / AT32 → CLK3_P,DIFFIO_RX_B9_P,DQ2B / CLK3_N,DIFFIO_RX_B9_N,DQ2B

FPLL_BL_CLKOUT0,FPLL_BL_CLKOUT_P,FPLL_BL_FB0,DIFFIO_TX_B5_P,DQ1B → AM34
FPLL_BL_CLKOUT1,FPLL_BL_CLKOUT_N,DIFFIO_TX_B5_N → AL34
FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1,DIFFIO_RX_B6_P,DQ1B → AK33
FPLL_BL_CLKOUT3,FPLL_BL_FBn,DIFFIO_RX_B6_N,DQ1B → AJ33

Bank 3D
2.5 Volt

CLK_ENET_FPGA_P 11 / CLK_ENET_FPGA_N 11 → CLK_ENET_FPGA_P AV19 / CLK_ENET_FPGA_N AU19 → CLK4_P,DIFFIO_RX_B76_P,DQ10B / CLK4_N,DIFFIO_RX_B76_N,DQ10B
19 SPI_CLK / 19 SPI_CSn → AF21 / AE21 → CLK5_P,DIFFIO_RX_B78_P,DQ11B / CLK5_N,DIFFIO_RX_B78_N,DQ11B
CLK_100M_FPGA 11 / 23 SFPB_TXFAULT → CLK_100M_FPGA AL20 / AK20 → CLK7_P,DIFFIO_RX_B84_P,DQ11B / CLK7_N,DIFFIO_RX_B84_N,DQ11B
12 LMK_CLEAN_CLK_P / 12 LMK_CLEAN_CLK_N → AD20 / AC21 → CLK6_P,DIFFIO_RX_B82_P,DQ11B / CLK6_N,DIFFIO_RX_B82_N,DQ11B

FPLL_BC_CLKOUT0,FPLL_BC_CLKOUT_P,FPLL_BC_FB0,DIFFIO_TX_B79_P,DQ11B → AC22 PCIE_PRSNT2_X1 → 3
FPLL_BC_CLKOUT1,FPLL_BC_CLKOUT_N,DIFFIO_TX_B79_N → AD21 PCIE_PRSNT2_X4 → 3
FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1,DIFFIO_RX_B80_P,DQS11B → AH21 PCIE_PERSTn → 3,13
FPLL_BC_CLKOUT3,FPLL_BC_FBn,DIFFIO_RX_B80_N,DQSn11B → AG21 SFPB_LOS → 23

Bank 4A
2.5 Volt

12 LMK_SYSREF_P / 12 LMK_SYSREF_N → AR6 / AP6 → CLK8_P,DIFFIO_RX_B168_P,DQ22B / CLK8_N,DIFFIO_RX_B168_N,DQ22B
19,31,32 I2C_SCL → 0 R591 → I2C_SCL_FPGA AW4
19,31,32 I2C_SDA → 0 R592 → I2C_SDA_FPGA AV4 → CLK9_P,DIFFIO_RX_B166_P,DQ22B / CLK9_N,DIFFIO_RX_B166_N,DQ22B
19 SPI_SDIO → AT7 → CLK10_P,DIFFIO_RX_B164_P,DQS22B / CLK10_N,DIFFIO_RX_B164_N,DQSn22B
19 LMK_RESET → AR7 → CLK11_P,DIFFIO_RX_B160_P,DQ21B / CLK11_N,DIFFIO_RX_B160_N,DQ21B

J15 1 SMA_CLKIN → AK7
23 SFPB_MOD2_SDA → AJ7
R353 49.9

FPLL_BR_CLKOUT0,FPLL_BR_CLKOUT_P,FPLL_BR_FB0,DIFFIO_TX_B161_P,DQ22B → AM7 RCLOCK_OUT_P → 12 RCLOCK_OUT_P
FPLL_BR_CLKOUT1,FPLL_BR_CLKOUT_N,DIFFIO_TX_B161_N → AL7 RCLOCK_OUT_N → 12 RCLOCK_OUT_N
FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1,DIFFIO_RX_B162_P,DQ22B → AP8 SFPB_MOD0_PRSNTn → 23 SFPB_MOD0_PRSNTn
FPLL_BR_CLKOUT3,FPLL_BR_FBn,DIFFIO_RX_B162_N,DQ22B → AN8 SFPB_MOD1_SCL → 23 SFPB_MOD1_SCL

Bank 8A
Variable Voltage

FMC PORT B
DEVCLKB
Alt. DEVCLK

FMCB_CLK_M2C_P0 C34 / FMCB_CLK_M2C_N0 D34 → CLK20_P,DIFFIO_RX_T113_P,DQ11T / CLK20_N,DIFFIO_RX_T113_N,DQ11T
FMCB_CLK_M2C_P1 G34 / FMCB_CLK_M2C_N1 H34 → CLK21_P,DIFFIO_RX_T111_P,DQS11T / CLK21_N,DIFFIO_RX_T111_N,DQSn11T
25 FMCB_LA_RX_CLK_P E34 / 25 FMCB_LA_RX_CLK_N F34 → CLK22_P,DIFFIO_RX_T108_P,DQ11T / CLK22_N,DIFFIO_RX_T108_N,DQ11T
25 FMCB_LA_RX_P7 N34 / 25 FMCB_LA_RX_N7 N33 → CLK23_P,DIFFIO_RX_T106_P,DQ10T / CLK23_N,DIFFIO_RX_T106_N,DQ10T

FPLL_TL_CLKOUT0,FPLL_TL_CLKOUT_P,FPLL_TL_FB0,DIFFIO_TX_T110_P,DQ11T → C33 FMCB_LA_TX_P17 → 25
FPLL_TL_CLKOUT1,FPLL_TL_CLKOUT_N,DIFFIO_TX_T110_N → D33 FMCB_LA_TX_N17 → 25
FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1,DIFFIO_RX_T109_P,DQ11T → B34 FMCB_LA_RX_P13 → 25 FMCB_LA_RX_P13
FPLL_TL_CLKOUT3,FPLL_TL_FBn,DIFFIO_RX_T109_N,DQ11T → A35 FMCB_LA_RX_N13 → 25 FMCB_LA_RX_N13

Bank 8D
Variable Voltage

FMCPORT A
DEVCLKB
Alt. DEVCLK

FMC_CLK_M2C_P0 B22 / FMC_CLK_M2C_N0 C22 → CLK16_P,DIFFIO_RX_T39_P,DQ2T / CLK16_N,DIFFIO_RX_T39_N,DQ2T
FMC_CLK_M2C_P1 A22 / FMC_CLK_M2C_N1 A21 → CLK17_P,DIFFIO_RX_T37_P,DQ1T / CLK17_N,DIFFIO_RX_T37_N,DQ1T
24 FMC_LA_RX_CLK_P H21 / 24 FMC_LA_RX_CLK_N J21 → CLK18_P,DIFFIO_RX_T33_P,DQ1T / CLK18_N,DIFFIO_RX_T33_N,DQ1T
24 FMC_LA_RX_P7 C20 / 24 FMC_LA_RX_N7 D20 → CLK19_P,DIFFIO_RX_T31_P,DQ1T / CLK19_N,DIFFIO_RX_T31_N,DQ1T

FPLL_TC_CLKOUT0,FPLL_TC_CLKOUT_P,FPLL_TC_FB0,DIFFIO_TX_T36_P,DQ1T → K21 USB_FPGA_DATA4
FPLL_TC_CLKOUT1,FPLL_TC_CLKOUT_N,DIFFIO_TX_T36_N → L21 USB_FPGA_DATA5
FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1,DIFFIO_RX_T35_P,DQS1T → A20 USB_FPGA_DATA6
FPLL_TC_CLKOUT3,FPLL_TC_FBn,DIFFIO_RX_T35_N,DQSn1T → B21 USB_FPGA_DATA7

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FMC_CLK_M2C_P0 R532 100, 1% FMC_CLK_M2C_N0
FMC_CLK_M2C_P1 R533 100, 1% FMC_CLK_M2C_N1
FMC_LA_RX_CLK_P R536 100, 1% FMC_LA_RX_CLK_N
FMC_LA_RX_P7 R537 100, 1% FMC_LA_RX_N7

FMCB_CLK_M2C_P0 R514 100, 1% FMCB_CLK_M2C_N0
FMCB_CLK_M2C_P1 R512 100, 1% FMCB_CLK_M2C_N1
FMCB_LA_RX_CLK_P R513 100, 1% FMCB_LA_RX_CLK_N
FMCB_LA_RX_P7 R517 100, 1% FMCB_LA_RX_N7

USB_FPGA_DATA[7..0] 8,27 → USB_FPGA_DATA[7..0]

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Title: Arria V SoC FPGA Development Kit Board

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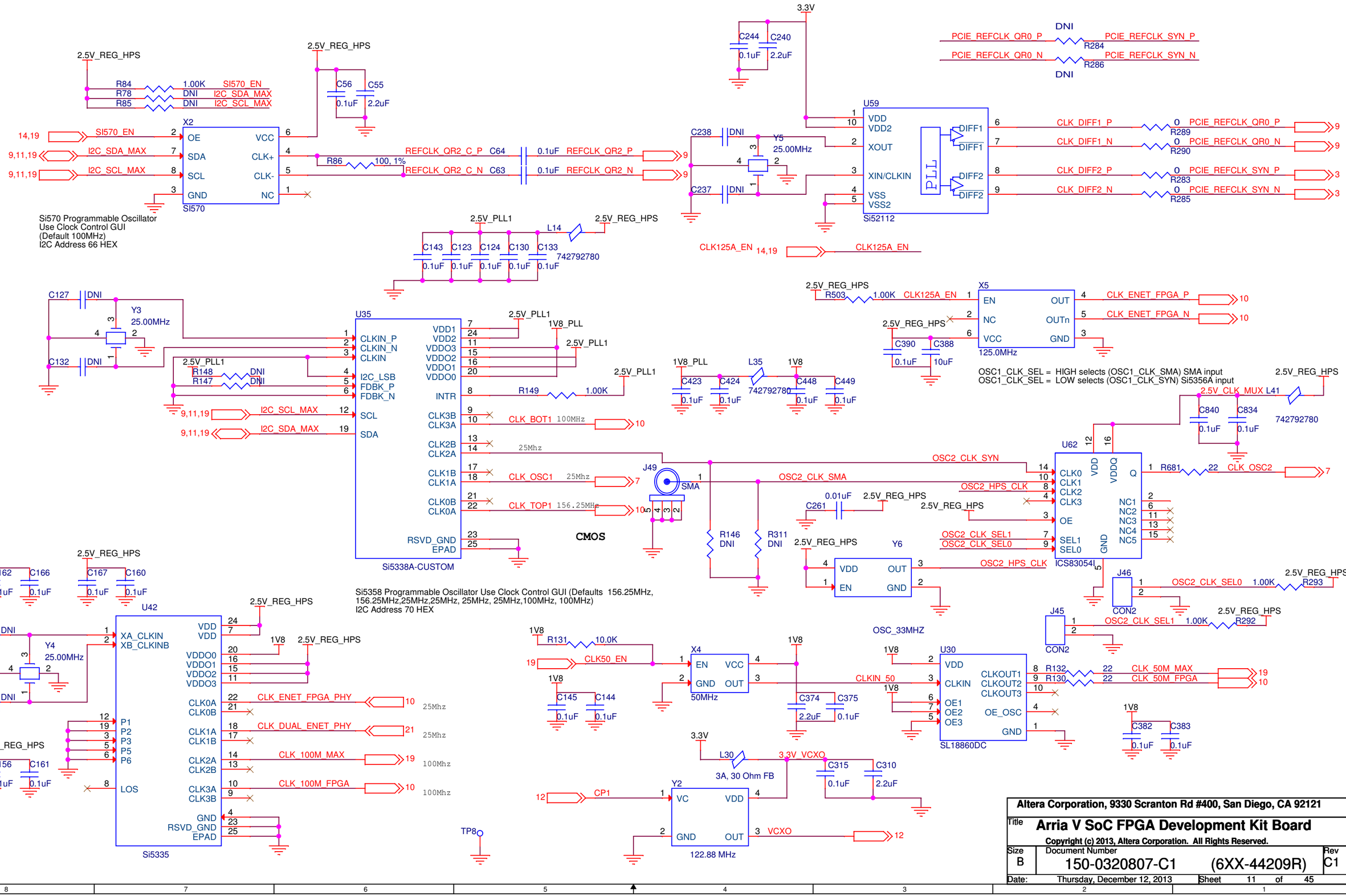
PLL



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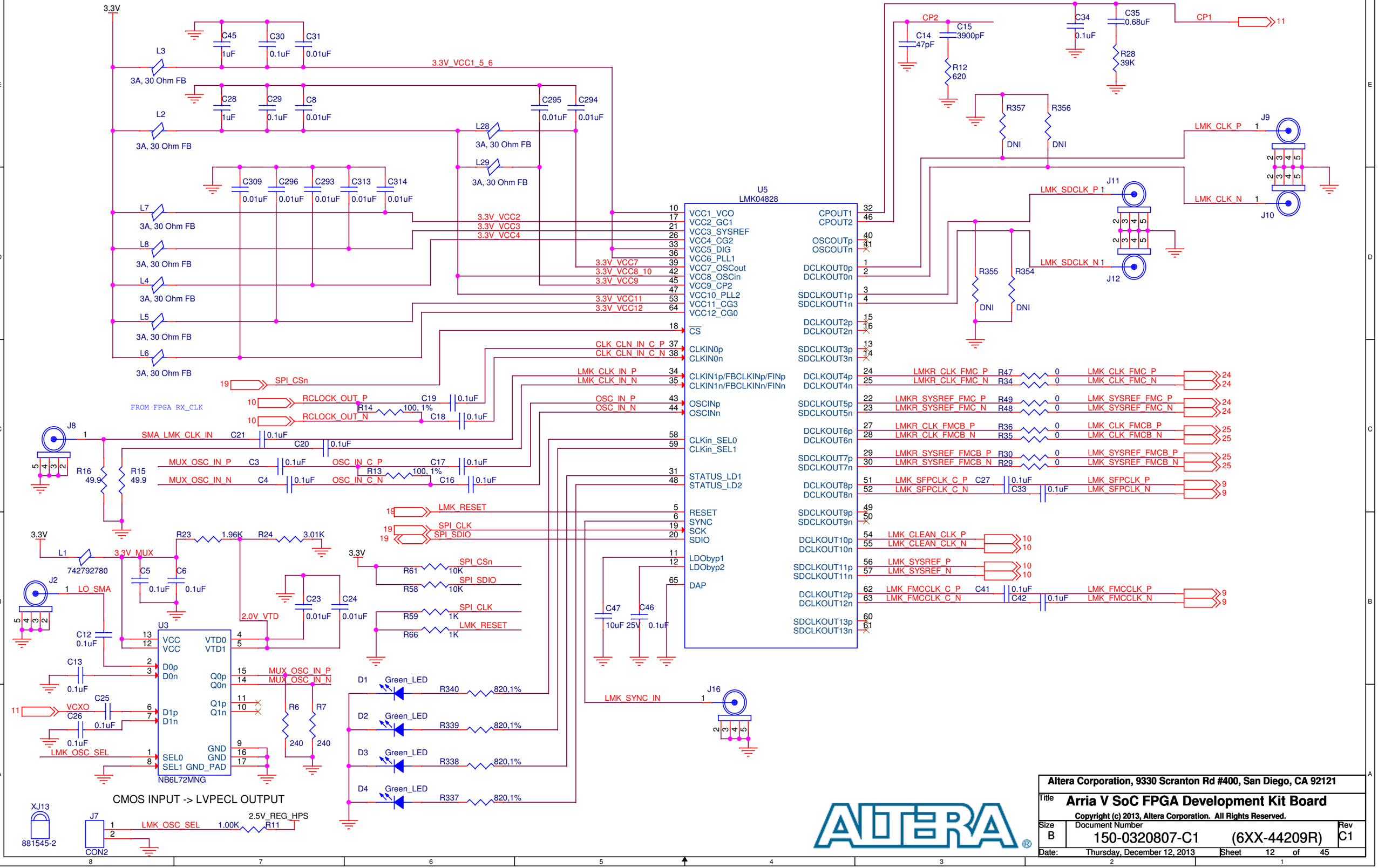

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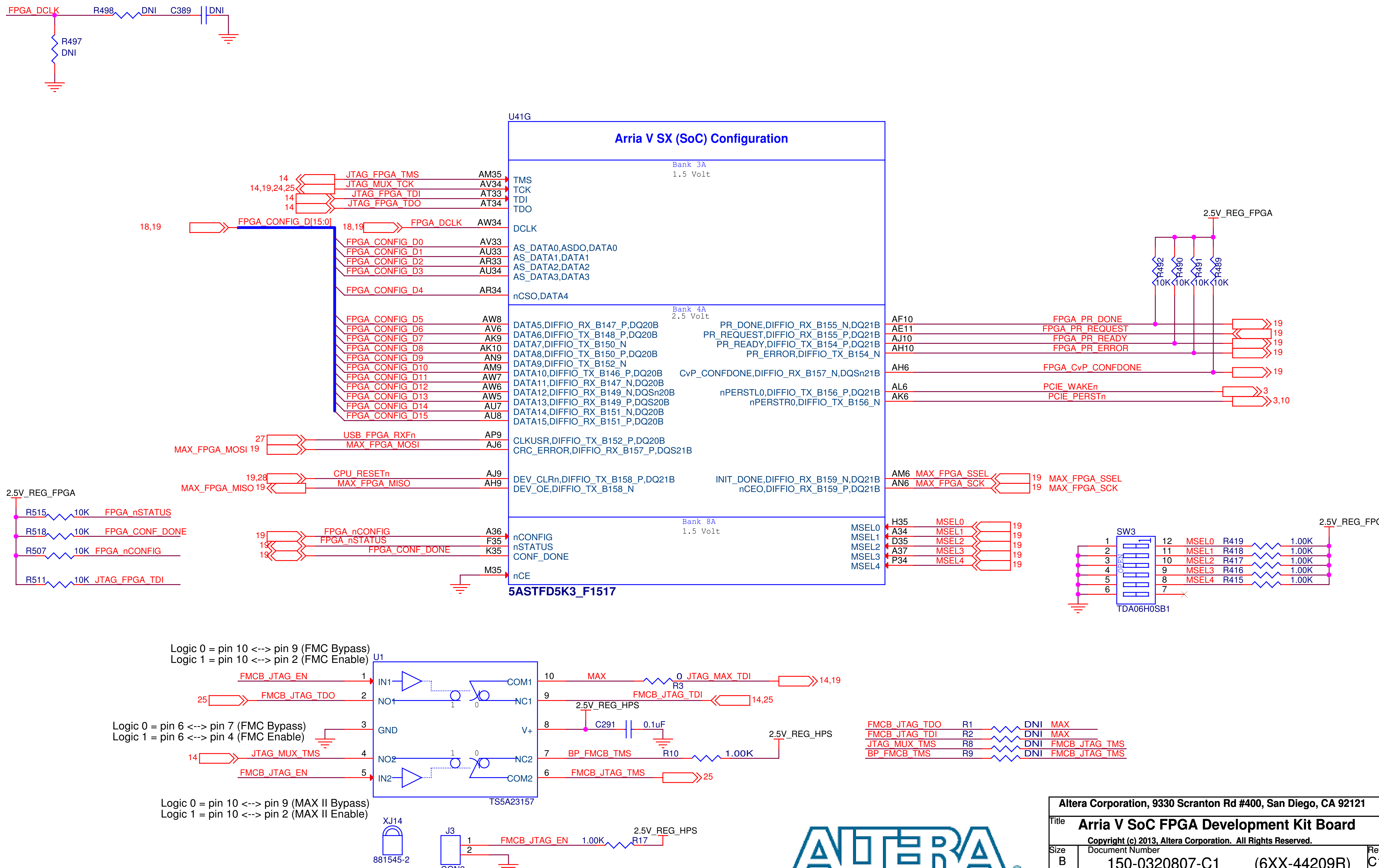
Arria V ST Configuration



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JTAG

USB Blaster Programming Header
(uses JTAG mode only)

2.5V_REG_HPS
R644 1.00K
USB_DISABLEn
J35
JTAG_TCK 14,30
JTAG_BLASTER_TDI
JTAG_TMS 14,30
JTAG_BLASTER_TDO 14,30
R654 0
JTAG_SMD
JTAG_TRST
MICTOR_RSTn 7,19 7,19,26
R655 1.00K
R668 1.00K
JTAG_BLASTER_TDO R667 DNI JTAG_BLASTER_TDI

Populate R183 if you would like to Master the JTAG chain through FMC

JTAG Chain Control

SW4 TDA04H0SB1
HPS_JTAG_EN R423 1.00K
FPGA_JTAG_EN R422 1.00K
FMC_JTAG_EN R421 1.00K
MAX_JTAG_EN R420 1.00K

ON = not-in-chain
OFF = in-chain

SW2 TDA04H0SB1
CLK125A_EN R413 10.0K
SI570_EN R405 10.0K
FACTORY_LOAD R404 10.0K
SECURITY_MODE R396 10.0K
1V8

CLK125A_EN 11,19 CLK125A_EN
SI570_EN 11,19 SI570_EN
FACTORY_LOAD 19 FACTORY_LOAD
SECURITY_MODE 19 SECURITY_MODE

U24 IDTQS3VH257
JTAG_MUX_TCK 13,14,19,24,25
JTAG_MICTOR_TCK 7,14
JTAG_MUX_TMS 14
JTAG_MICTOR_TMS 7,14
JTAG_MUX_HPS_TDI 11
JTAG_MICTOR_TDO 7,14
JTAG_FPGA_TDI 13,14
JTAG_MICTOR_TDI 7,14
R113 1.00K JTAG_HPS_SEL
C92 2.2uF C93 0.1uF
XJ5 881545-2 J19 CON2

JTAG_MUX_TCK R461 DNI JTAG_HPS_TCK
JTAG_MICTOR_TCK R460 DNI JTAG_HPS_TCK
JTAG_MUX_TMS R472 DNI JTAG_HPS_TMS
JTAG_MICTOR_TMS R471 DNI JTAG_HPS_TMS
JTAG_MUX_HPS_TDI R469 DNI JTAG_HPS_TDI
JTAG_MICTOR_TDO R470 DNI JTAG_HPS_TDI
JTAG_FPGA_TDI R458 DNI JTAG_HPS_TDO
JTAG_MICTOR_TDI R459 DNI JTAG_HPS_TDO

U23 IDTQS3VH257
JTAG_TCK 14,30
JTAG_MICTOR_TCK 7,14
JTAG_TMS 14,30
JTAG_MICTOR_TMS 7,14
JTAG_BLASTER_TDI 30
JTAG_MICTOR_TDI 7,14
JTAG_BLASTER_TDO 14,30
JTAG_MICTOR_TDO 7,14
R114 1.00K JTAG_SEL
C90 2.2uF C91 0.1uF
XJ6 881545-2 J21 CON2

JTAG_TCK R465 DNI JTAG_MUX_TCK
JTAG_MICTOR_TCK R464 DNI JTAG_MUX_TCK
JTAG_TMS R476 DNI JTAG_MUX_TMS
JTAG_MICTOR_TMS R475 DNI JTAG_MUX_TMS
JTAG_BLASTER_TDI R473 DNI JTAG_MUX_TDI
JTAG_MICTOR_TDI R474 DNI JTAG_MUX_TDI
JTAG_BLASTER_TDO R462 DNI JTAG_MUX_TDO
JTAG_MICTOR_TDO R463 DNI JTAG_MUX_TDO

When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

TS5A23157 Switch Functions

Logic 0 = pin 10 <--> pin 9 (HPS Bypass)
Logic 1 = pin 10 <--> pin 2 (HPS Enable)
Logic 0 = pin 6 <--> pin 7 (HPS Bypass)
Logic 1 = pin 6 <--> pin 4 (HPS Enable)

U15 TS5A23157
HPS_JTAG_EN
JTAG_MUX_HPS_TDI 0 R111 HPS
JTAG_MUX_TMS
HPS_JTAG_EN
JTAG_MUX_TDO
FPGA 0 R92 JTAG_FPGA_TDI 13,14
C335 0.1uF
BP_HPS_TMS R93 1.00K
JTAG_HPS_TMS 7,14

Logic 0 = pin 10 <--> pin 9 (FPGA Bypass)
Logic 1 = pin 10 <--> pin 2 (FPGA Enable)
Logic 0 = pin 6 <--> pin 7 (FPGA Bypass)
Logic 1 = pin 6 <--> pin 4 (FPGA Enable)

U16 TS5A23157
FPGA_JTAG_EN
13 JTAG_FPGA_TDO
JTAG_MUX_TMS
FPGA_JTAG_EN
FMC 0 R94 FMC_JTAG_TDI 24
JTAG_FPGA_TDI 13,14
C334 0.1uF
BP_FPGA_TMS R95 1.00K
JTAG_FPGA_TMS 13

Logic 0 = pin 10 <--> pin 9 (FMC Bypass)
Logic 1 = pin 10 <--> pin 2 (FMC Enable)
Logic 0 = pin 6 <--> pin 7 (FMC Bypass)
Logic 1 = pin 6 <--> pin 4 (FMC Enable)

U17 TS5A23157
FMC_JTAG_EN
24 FMC_JTAG_TDO
JTAG_MUX_TMS
FMC_JTAG_EN
FMCB 0 R96 FMCB_JTAG_TDI 19
FMC_JTAG_TDI
C333 0.1uF
BP_FMC_TMS R97 1.00K
FMC_JTAG_TMS 24

Logic 0 = pin 10 <--> pin 9 (MAX II Bypass)
Logic 1 = pin 10 <--> pin 2 (MAX II Enable)
Logic 0 = pin 6 <--> pin 7 (HSMBBypass)
Logic 1 = pin 6 <--> pin 4 (HSMB Enable)

U18 TS5A23157
MAX_JTAG_EN
19 JTAG_MAX_TDO
JTAG_MUX_TMS
MAX_JTAG_EN
MUX 0 R98 JTAG_MUX_TDI 14
JTAG_MAX_TDI 13,19
C332 0.1uF
BP_MAX_TMS R99 1.00K
JTAG_MAX_TMS 19

HPS R453 DNI JTAG_MUX_TDO
FPGA R440 DNI JTAG_MUX_TDO
BP_HPS_TMS R452 DNI JTAG_HPS_TMS

FMC_JTAG_TDO R448 DNI FMCB
FMC_JTAG_TDI R438 DNI FMCB
JTAG_MUX_TMS R447 DNI FMC_JTAG_TMS
BP_FMC_TMS R446 DNI FMC_JTAG_TMS

JTAG_FPGA_TDO R451 DNI FMC
JTAG_FPGA_TDI R439 DNI FMC
JTAG_MUX_TMS R450 DNI JTAG_FPGA_TMS
BP_FPGA_TMS R449 DNI JTAG_FPGA_TMS

JTAG_MAX_TDO R445 DNI MUX
JTAG_MAX_TDI R437 DNI MUX
JTAG_MUX_TMS R444 DNI JTAG_MAX_TMS
BP_MAX_TMS R443 DNI JTAG_MAX_TMS

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Title: **Arria V SoC FPGA Development Kit Board**

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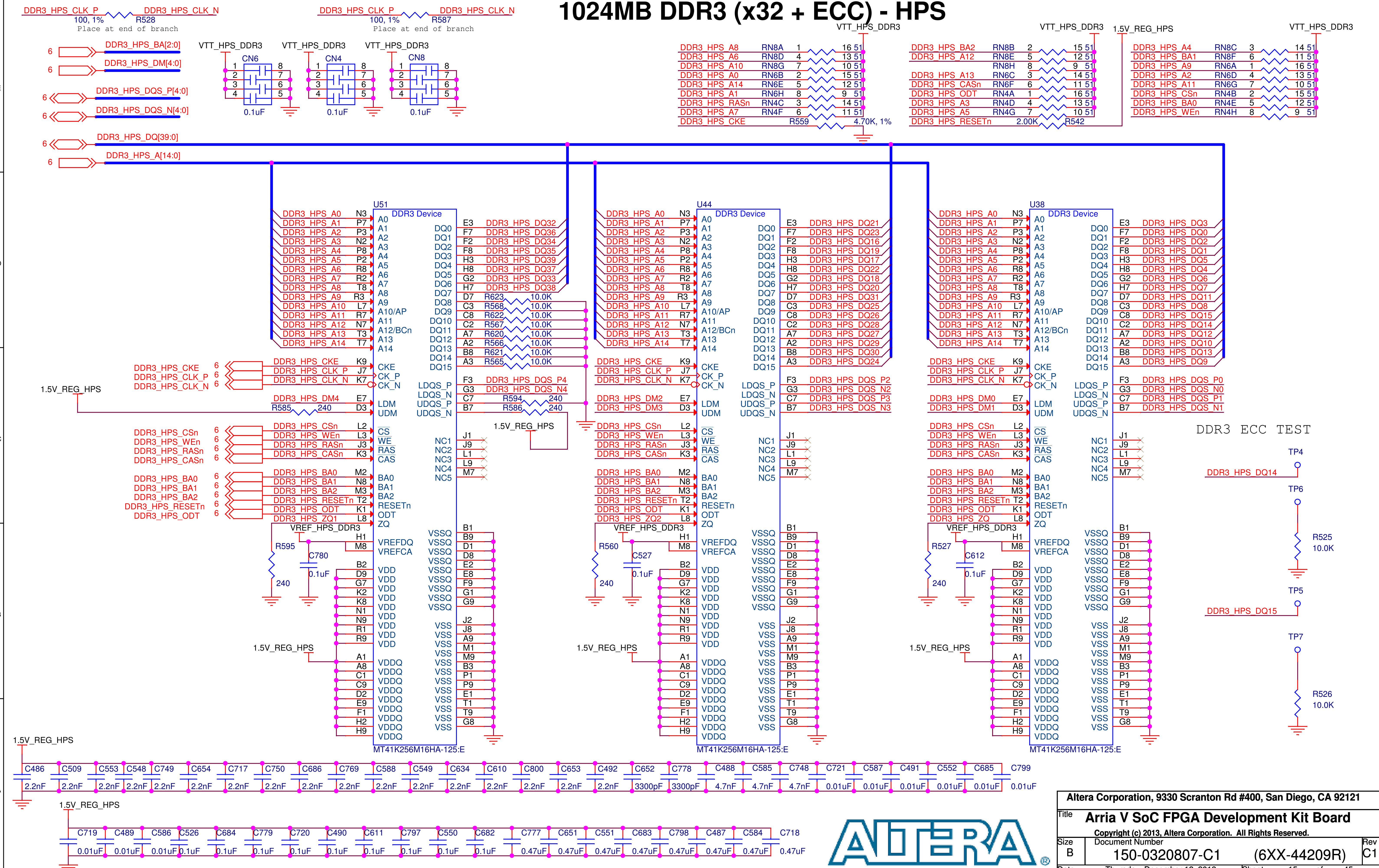
1024MB DDR3 (x32 + ECC) - HPS



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Title: **Arria V SoC FPGA Development Kit Board**

Size	Document Number		Rev
B	150-0320807-C1	(6XX-44209R)	C1

Date: Thursday, December 12, 2013 — Sheet 15 of 45

1024MB DDR3 (x32) - FPGA PORT A

DDR3A_CLK_P — 100, 1% — R488 — DDR3A_CLK_N

4 DDR3A_BA[2:0]
4 DDR3A_DM[3:0]
4 DDR3A_DQS_P[3:0]
4 DDR3A_DQS_N[3:0]
4 DDR3A_DQ[31:0]
4 DDR3A_A[14:0]

VTT_FPGA_DDR3A — CN3 — 0.1uF
VTT_FPGA_DDR3A — CN1 — 0.1uF
VTT_FPGA_DDR3A — CN2 — 0.1uF

V21	DDR3A_A11	RN1A	1	16	51
V19	DDR3A_A1	RN1D	4	13	51
V8	DDR3A_BA1	RN1G	7	10	51
V22	DDR3A_A9	RN2B	2	15	51
V25	DDR3A_ODT	RN2E	5	12	51
V23	DDR3A_A14	RN2H	8	9	51
V16	DDR3A_BA2	RN3C	3	14	51
V29	DDR3A_A5	RN3F	6	11	51
V7	DDR3A_CKE	R487		4.70K, 1%	

VTT_FPGA_DDR3A

V11	DDR3A_A8	RN1B	2	15	51
V9	DDR3A_A4	RN1E	5	12	51
V14	DDR3A_A10	RN1H	8	9	51
V24	DDR3A_A13	RN2C	3	14	51
V13	DDR3A_CASn	RN2F	6	11	51
V26	DDR3A_CSn	RN3A	1	16	51
V28	DDR3A_A3	RN3D	4	13	51
		RN3G	7	10	51
V31	DDR3A_RESETn	2.00K		R502	

1.5V_REG_FPGA

VTT_FPGA_DDR3A

V10	DDR3A_A6	RN1C	3	14	51
V18	DDR3A_A12	RN1F	6	11	51
V30	DDR3A_A7	RN2A	1	16	51
V15	DDR3A_WEn	RN2D	4	13	51
V12	DDR3A_RASn	RN2G	7	10	51
V27	DDR3A_BA0	RN3B	2	15	51
V18	DDR3A_A0	RN3E	5	12	51
V20	DDR3A_A2	RN3H	8	9	51

U37 — DDR3 Device — MT41K256M16HA-125:E

DDR3A_A0	N3	A0	DQ0	E3	DDR3A_DQ17
DDR3A_A1	P7	A1	DQ1	F7	DDR3A_DQ16
DDR3A_A2	P3	A2	DQ2	F2	DDR3A_DQ21
DDR3A_A3	N2	A3	DQ3	F8	DDR3A_DQ18
DDR3A_A4	P8	A4	DQ4	H3	DDR3A_DQ23
DDR3A_A5	P2	A5	DQ5	H8	DDR3A_DQ19
DDR3A_A6	R8	A6	DQ6	G2	DDR3A_DQ22
DDR3A_A7	R2	A7	DQ7	H7	DDR3A_DQ20
DDR3A_A8	T8	A8	DQ8	D7	DDR3A_DQ28
DDR3A_A9	R3	A9	DQ9	C3	DDR3A_DQ25
DDR3A_A10	L7	A10/AP	DQ10	C8	DDR3A_DQ26
DDR3A_A11	R7	A11	DQ11	C2	DDR3A_DQ24
DDR3A_A12	N7	A12/BCn	DQ12	A7	DDR3A_DQ30
DDR3A_A13	T3	A13	DQ13	A2	DDR3A_DQ29
DDR3A_A14	T7	A14	DQ14	B8	DDR3A_DQ31
			DQ15	A3	DDR3A_DQ27
DDR3A_CKE	K9	CKE	LDQS_P	F3	DDR3A_DQS_P2
DDR3A_CLK_P	J7	CK_P	LDQS_N	G3	DDR3A_DQS_N2
DDR3A_CLK_N	K7	CK_N	UDQS_P	C7	DDR3A_DQS_P3
DDR3A_DM2	E7	LDM	UDQS_N	B7	DDR3A_DQS_N3
DDR3A_DM3	D3	UDM			
DDR3A_CSn	L2	CS	NC1	J1	
DDR3A_WEn	L3	WE	NC2	J9	
DDR3A_RASn	J3	RAS	NC3	L1	
DDR3A_CASn	K3	CAS	NC4	L9	
			NC5	M7	
DDR3A_BA0	M2	BA0			
DDR3A_BA1	N8	BA1			
DDR3A_BA2	M3	BA2			
DDR3A_RESETn	T2	RESETn			
DDR3A_ODT	K1	ODT			
DDR3A_ZQ1	L8	ZQ			
VREF_FPGA_DDR3A	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
1.5V_REG_FPGA			VSS	A9	
	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

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U29 — DDR3 Device — MT41K256M16HA-125:E

DDR3A_A0	N3	A0	DQ0	E3	DDR3A_DQ6
DDR3A_A1	P7	A1	DQ1	F7	DDR3A_DQ5
DDR3A_A2	P3	A2	DQ2	F2	DDR3A_DQ7
DDR3A_A3	N2	A3	DQ3	F8	DDR3A_DQ1
DDR3A_A4	P8	A4	DQ4	H3	DDR3A_DQ0
DDR3A_A5	P2	A5	DQ5	H8	DDR3A_DQ3
DDR3A_A6	R8	A6	DQ6	G2	DDR3A_DQ2
DDR3A_A7	R2	A7	DQ7	H7	DDR3A_DQ4
DDR3A_A8	T8	A8	DQ8	D7	DDR3A_DQ10
DDR3A_A9	R3	A9	DQ9	C3	DDR3A_DQ15
DDR3A_A10	L7	A10/AP	DQ10	C8	DDR3A_DQ12
DDR3A_A11	R7	A11	DQ11	C2	DDR3A_DQ8
DDR3A_A12	N7	A12/BCn	DQ12	A7	DDR3A_DQ11
DDR3A_A13	T3	A13	DQ13	A2	DDR3A_DQ9
DDR3A_A14	T7	A14	DQ14	B8	DDR3A_DQ13
			DQ15	A3	DDR3A_DQ14
DDR3A_CKE	K9	CKE	LDQS_P	F3	DDR3A_DQS_P0
DDR3A_CLK_P	J7	CK_P	LDQS_N	G3	DDR3A_DQS_N0
DDR3A_CLK_N	K7	CK_N	UDQS_P	C7	DDR3A_DQS_P1
DDR3A_DM0	E7	LDM	UDQS_N	B7	DDR3A_DQS_N1
DDR3A_DM1	D3	UDM			
DDR3A_CSn	L2	CS	NC1	J1	
DDR3A_WEn	L3	WE	NC2	J9	
DDR3A_RASn	J3	RAS	NC3	L1	
DDR3A_CASn	K3	CAS	NC4	L9	
			NC5	M7	
DDR3A_BA0	M2	BA0			
DDR3A_BA1	N8	BA1			
DDR3A_BA2	M3	BA2			
DDR3A_RESETn	T2	RESETn			
DDR3A_ODT	K1	ODT			
DDR3A_ZQ	L8	ZQ			
VREF_FPGA_DDR3A	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
1.5V_REG_FPGA			VSS	A9	
	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

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1.5V_REG_FPGA

C364 2.2nF, C453 2.2nF, C431 2.2nF, C378 2.2nF, C402 2.2nF, C405 2.2nF, C376 2.2nF, C373 2.2nF, C455 2.2nF, C362 3300pF, C360 3300pF, C381 4.7nF, C363 4.7nF, C403 4.7nF

1.5V_REG_FPGA

C401 0.01uF, C377 0.01uF, C454 0.01uF, C404 0.1uF, C361 0.1uF, C380 0.1uF, C458 0.1uF, C372 0.47uF, C457 0.47uF, C418 0.47uF, C369 0.47uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: Arria V SoC FPGA Development Kit Board

Size	Document Number	Rev
B	150-0320807-C1 (6XX-44209R)	C1

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1024MB DDR3 (x32) - FPGA PORT B

DDR3B_CLK_P — 100, 1% — R545 — DDR3B_CLK_N

5 DDR3B_BA[2:0]
5 DDR3B_DM[3:0]
5 DDR3B_DQS_P[3:0]
5 DDR3B_DQS_N[3:0]
5 DDR3B_DQ[31:0]
5 DDR3B_A[14:0]

VTT_FPGA_DDR3B — CN9 — 0.1uF
VTT_FPGA_DDR3B — CN7 — 0.1uF
VTT_FPGA_DDR3B — CN5 — 0.1uF

VTT_FPGA_DDR3B

V56	DDR3B_A11	RN5A	1	16	51
V54	DDR3B_A1	RN5D	4	13	51
V53	DDR3B_BA1	RN5G	7	10	51
V57	DDR3B_A9	RN7B	2	15	51
V60	DDR3B_ODT	RN7E	5	12	51
V58	DDR3B_A14	RN7H	8	9	51
V51	DDR3B_BA2	RN9C	3	14	51
V64	DDR3B_A5	RN9F	6	11	51
V38	DDR3B_CKE	R539	4.70K, 1%		

VTT_FPGA_DDR3B

V42	DDR3B_A8	RN5B	2	15	51
V40	DDR3B_A4	RN5E	5	12	51
V49	DDR3B_A10	RN5H	8	9	51
V59	DDR3B_A13	RN7C	3	14	51
V48	DDR3B_CASn	RN7F	6	11	51
V61	DDR3B_CSn	RN9A	1	16	51
V63	DDR3B_A3	RN9D	4	13	51
		RN9G	7	10	51
V66	DDR3B_RESETn	2.00K	R556		

1.5V_REG_FPGA

VTT_FPGA_DDR3B

V41	DDR3B_A6	RN5C	3	14	51
V52	DDR3B_A12	RN5F	6	11	51
V65	DDR3B_A7	RN7A	1	16	51
V50	DDR3B_WEn	RN7D	4	13	51
V47	DDR3B_RASn	RN7G	7	10	51
V62	DDR3B_BA0	RN9B	2	15	51
V53	DDR3B_A0	RN9E	5	12	51
V55	DDR3B_A2	RN9H	8	9	51

U49 — DDR3 Device

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ18
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ20
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ17
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ19
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ16
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ21
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ22
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ23
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ29
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ30
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ24
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ27
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ26
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ28
DDR3B_A14	T7	A14	DQ14	B8	DDR3B_DQ25
			DQ15	A3	DDR3B_DQ31
DDR3B_CKE	K9	CKE	LDQS_P	F3	DDR3B_DQS_P2
DDR3B_CLK_P	J7	CK_P	LDQS_N	G3	DDR3B_DQS_N2
DDR3B_CLK_N	K7	CK_N	UDQS_P	C7	DDR3B_DQS_P3
DDR3B_DM2	E7	LDM	UDQS_N	B7	DDR3B_DQS_N3
DDR3B_DM3	D3	UDM			
DDR3B_CSn	L2	CS	NC1	J1	
DDR3B_WEn	L3	WE	NC2	J9	
DDR3B_RASn	J3	RAS	NC3	L1	
DDR3B_CASn	K3	CAS	NC4	L9	
			NC5	M7	
DDR3B_BA0	M2	BA0			
DDR3B_BA1	N8	BA1			
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ1	L8	ZQ			
VREF_FPGA_DDR3B	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
			VSS	A9	
1.5V_REG_FPGA	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

MT41K256M16HA-125:E

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U43 — DDR3 Device

DDR3B_A0	N3	A0	DQ0	E3	DDR3B_DQ7
DDR3B_A1	P7	A1	DQ1	F7	DDR3B_DQ6
DDR3B_A2	P3	A2	DQ2	F2	DDR3B_DQ5
DDR3B_A3	N2	A3	DQ3	F8	DDR3B_DQ1
DDR3B_A4	P8	A4	DQ4	H3	DDR3B_DQ2
DDR3B_A5	P2	A5	DQ5	H8	DDR3B_DQ0
DDR3B_A6	R8	A6	DQ6	G2	DDR3B_DQ4
DDR3B_A7	R2	A7	DQ7	H7	DDR3B_DQ3
DDR3B_A8	T8	A8	DQ8	D7	DDR3B_DQ13
DDR3B_A9	R3	A9	DQ9	C3	DDR3B_DQ12
DDR3B_A10	L7	A10/AP	DQ10	C8	DDR3B_DQ9
DDR3B_A11	R7	A11	DQ11	C2	DDR3B_DQ15
DDR3B_A12	N7	A12/BCn	DQ12	A7	DDR3B_DQ10
DDR3B_A13	T3	A13	DQ13	A2	DDR3B_DQ14
DDR3B_A14	T7	A14	DQ14	B8	DDR3B_DQ8
			DQ15	A3	DDR3B_DQ11
DDR3B_CKE	K9	CKE	LDQS_P	F3	DDR3B_DQS_P0
DDR3B_CLK_P	J7	CK_P	LDQS_N	G3	DDR3B_DQS_N0
DDR3B_CLK_N	K7	CK_N	UDQS_P	C7	DDR3B_DQS_P1
DDR3B_DM0	E7	LDM	UDQS_N	B7	DDR3B_DQS_N1
DDR3B_DM1	D3	UDM			
DDR3B_CSn	L2	CS	NC1	J1	
DDR3B_WEn	L3	WE	NC2	J9	
DDR3B_RASn	J3	RAS	NC3	L1	
DDR3B_CASn	K3	CAS	NC4	L9	
			NC5	M7	
DDR3B_BA0	M2	BA0			
DDR3B_BA1	N8	BA1			
DDR3B_BA2	M3	BA2			
DDR3B_RESETn	T2	RESETn			
DDR3B_ODT	K1	ODT			
DDR3B_ZQ	L8	ZQ			
VREF_FPGA_DDR3B	H1	VREFDQ	VSSQ	B1	
	M8	VREFCA	VSSQ	B9	
			VSSQ	D1	
	B2	VDD	VSSQ	D8	
	D9	VDD	VSSQ	E2	
	G7	VDD	VSSQ	E8	
	K2	VDD	VSSQ	F9	
	K8	VDD	VSSQ	G1	
	N1	VDD	VSSQ	G9	
	N9	VDD			
	R1	VDD	VSS	J2	
	R9	VDD	VSS	J8	
			VSS	A9	
1.5V_REG_FPGA	A1	VDDQ	VSS	M1	
	A8	VDDQ	VSS	M9	
	C1	VDDQ	VSS	B3	
	C9	VDDQ	VSS	P1	
	D2	VDDQ	VSS	P9	
	E9	VDDQ	VSS	E1	
	F1	VDDQ	VSS	T1	
	H2	VDDQ	VSS	T9	
	H9	VDDQ	VSS	G8	

MT41K256M16HA-125:E

R531 240 — C760 0.1uF

1.5V_REG_FPGA

C757 2.2nF, C759 2.2nF, C590 2.2nF, C730 2.2nF, C691 2.2nF, C572 2.2nF, C533 2.2nF, C694 2.2nF, C592 2.2nF, C529 3300pF, C531 3300pF, C692 4.7nF, C595 4.7nF, C532 4.7nF

1.5V_REG_FPGA

C758 0.01uF, C690 0.01uF, C591 0.01uF, C762 0.1uF, C693 0.1uF, C594 0.1uF, C530 0.1uF, C761 0.47uF, C710 0.47uF, C560 0.47uF, C571 0.47uF

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

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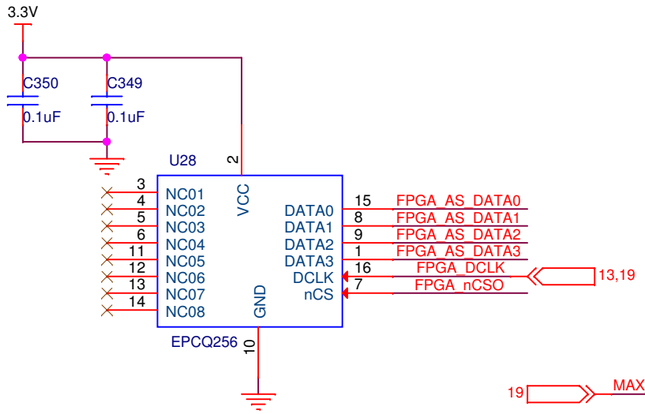
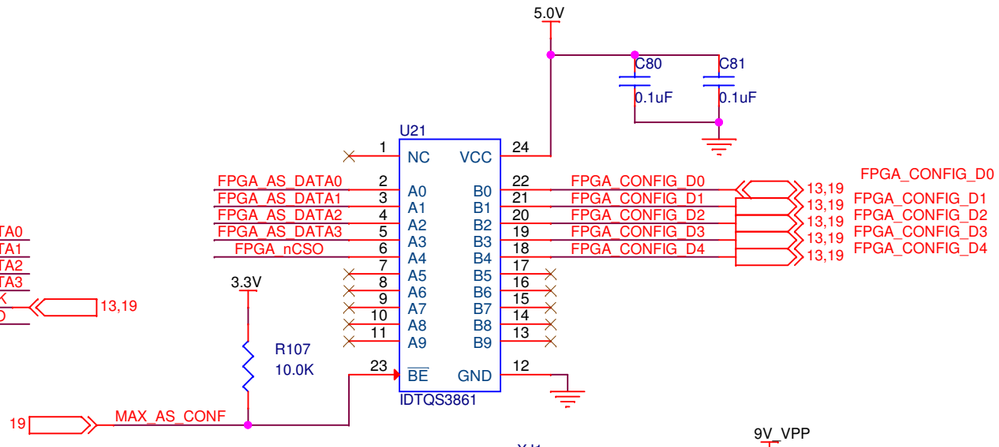
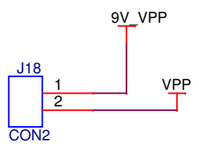
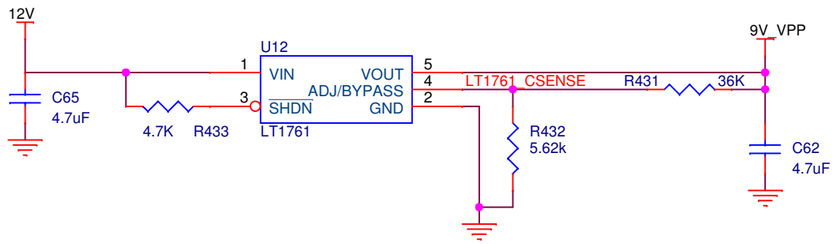
FLASH, EPCQ

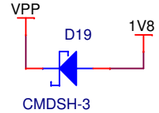
EPCQ



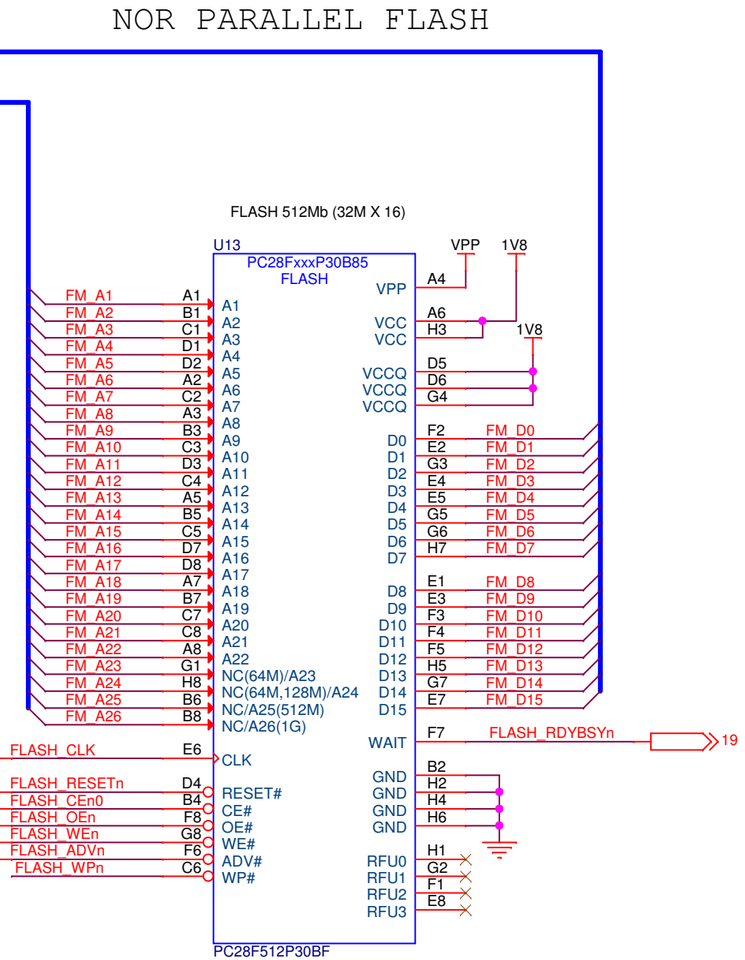


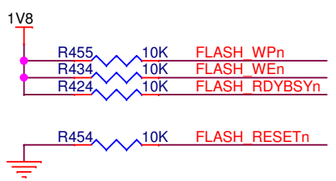


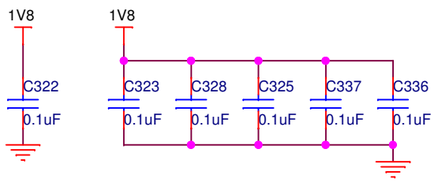




NOR PARALLEL FLASH







- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

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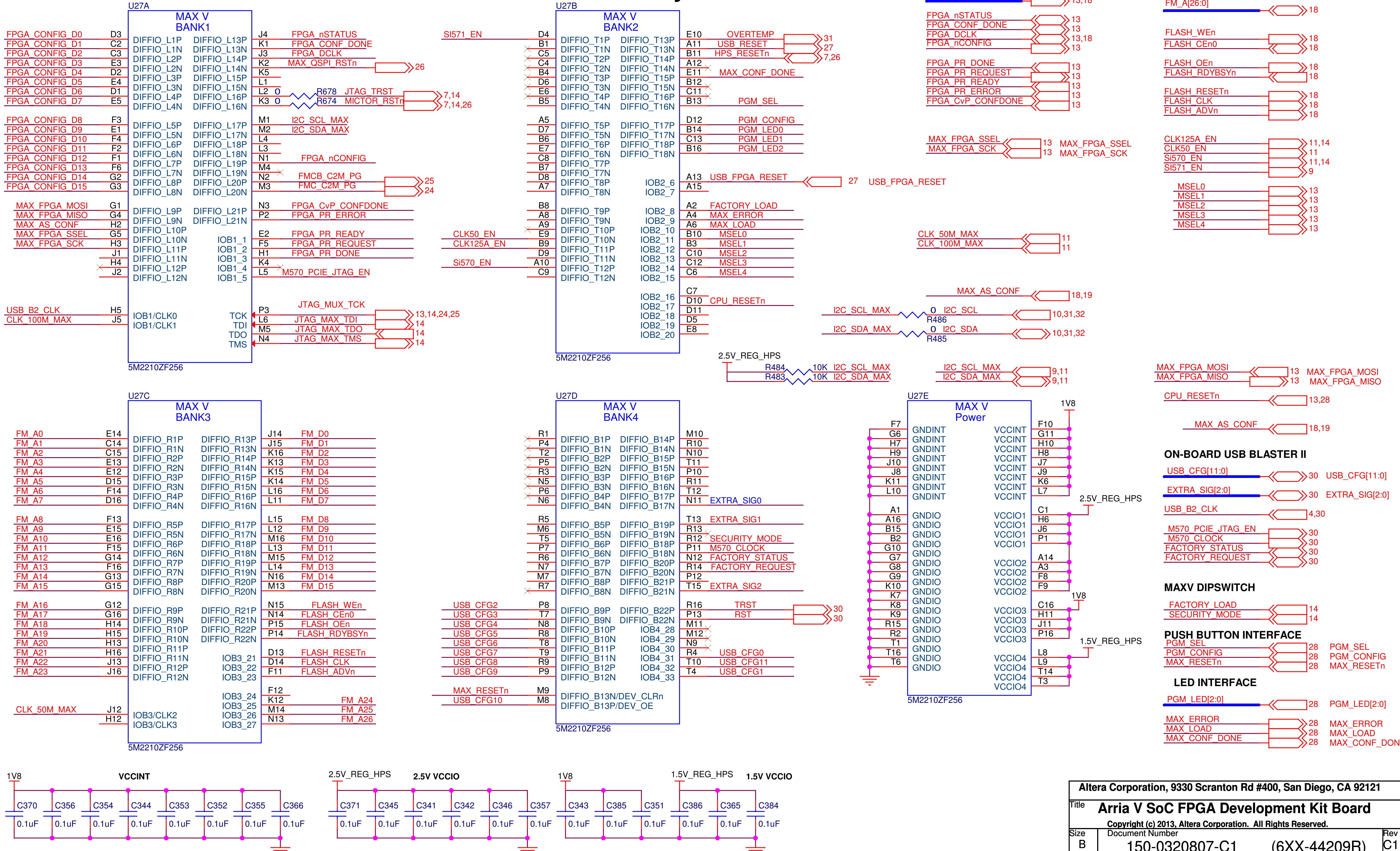
5M2210 System Controller



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10/100/1000 Ethernet - HPS

ETHERNET INTERFACE

ENET_HPS_TXD[3..0] 7 ENET_HPS_TXD[3..0]
ENET_HPS_GTX_CLK 7 ENET_HPS_GTX_CLK
ENET_HPS_TX_EN 7 ENET_HPS_TX_EN
ENET_HPS_MDC 7,20 ENET_HPS_MDC
ENET_HPS_RESETn 20,26 ENET_HPS_RESETn
ENET_HPS_RXD[3..0] 7 ENET_HPS_RXD[3..0]
ENET_HPS_RX_CLK 7 ENET_HPS_RX_CLK
ENET_HPS_RX_DV 7 ENET_HPS_RX_DV
ENET_HPS_MDIO 7,20 ENET_HPS_MDIO
ENET_HPS_INTn 7,20 ENET_HPS_INTn

ENET_HPS_LED2_LINK
ENET_HPS_LED1_LINK

J13 ENET_L829-1J1T-43
13 YK Yellow
14 YA
R74 220 3.3V_REG_HPS
18 GND_TAB
19 GND_TAB
15 OK Orange
17 GK Green
16 GOA
TD0_P 11 MDI_HPS_P0
CT0 12 CT0
TD0_N 10 MDI_HPS_N0
TD1_P 4 MDI_HPS_P1
CT1 6 CT1
TD1_N 5 MDI_HPS_N1
TD2_P 3 MDI_HPS_P2
CT2 1 CT2
TD2_N 2 MDI_HPS_N3
TD3_P 8 MDI_HPS_P3
CT3 7 CT3
TD3_N 9 MDI_HPS_N2
R31 220 3.3V_REG_HPS

U7A KSZ9021RN
ENET_HPS_MDC 36 MDC
ENET_HPS_MDIO 37 MDIO
ENET_HPS_RESETn 42 RESET_N
ENET_HPS_INTn 38 INT_N
MDI INTERFACE
TXRXP_A 2
TXRXM_A 3
TXRXP_B 5
TXRXM_B 6
TXRXP_C 7
TXRXM_C 8
TXRXP_D 10
TXRXM_D 11
R37 4.99K ENET_HPS_RSET 48 ISET
ENET_HPS_LED1_LINK 17 LED1_PHYAD0
ENET_HPS_LED2_LINK 15 LED2_PHYAD1
C38 DNI Y1 25.00MHz C40 DNI
3 4 2
46 XI
45 XO
RX_CLK_PHYAD2 35 ENET_HPS_RX_CLK
GTX_CLK 24 ENET_HPS_GTX_CLK
TX_EN 25 ENET_HPS_TX_EN
RX_DV_CLK125_EN 33 ENET_HPS_RX_DV
TXD3 22 ENET_HPS_TXD3
TXD2 21 ENET_HPS_TXD2
TXD1 20 ENET_HPS_TXD1
TXD0 19 ENET_HPS_TXD0
RXD0_MODE0 32 ENET_HPS_RXD0
RXD1_MODE1 31 ENET_HPS_RXD1
RXD2_MODE2 28 ENET_HPS_RXD2
RXD3_MODE3 27 ENET_HPS_RXD3
CLK125_NDO_LED_MODE 41 CLK125_NDO_LED_MODE

2.5V_REG_HPS U34 2.5V_REG_HPS
1 A0 VCC 8
2 A1 WP 7
3 A2 SCL 6 I2C_SCL_HPS 7,28,33
4 GND SDA 5 I2C_SDA_HPS 7,28,33
24LC32A

3.3V_REG_HPS C51 10uF C52 10uF

3.3V_REG_HPS L10 3A, 30 Ohm FB C74 22uF C68 2.2uF C77 0.1uF 3.3V_AVDDH
3.3V_REG_HPS L33 3A, 30 Ohm FB C331 22uF C329 2.2uF C338 0.1uF 3.3V_DVDDH

1.2V_AVDLL_PLL C95 22uF C96 2.2uF C109 0.1uF
L13 3A, 30 Ohm FB C110 22uF C113 2.2uF C111 0.1uF 1.2V_AVDDL
L12 3A, 30 Ohm FB C107 22uF C106 2.2uF C108 0.1uF 1.2V_DVDDL

C37 0.01uF CT0
C36 0.01uF CT1
C53 0.01uF CT2
C54 0.01uF CT3

U7B KSZ9021RN
3.3V_AVDDH 47 AVDDH 12 AVDDH 1 AVDDH
3.3V_DVDDH 40 DVDDH 16 DVDDH 34 DVDDH
49 P_GND 13 VSS_PS 29 VSS
1.2V_AVDLL_PLL 44 AVDDL_PLL 43 LDO_O
1.2V_AVDDL 9 AVDDL 4 AVDDL
1.2V_DVDDL 18 DVDDL 14 DVDDL 39 DVDDL 30 DVDDL 26 DVDDL 23 DVDDL

1.2V AVDLL_PLL

2.5V_REG_HPS C103 10uF
U26 LTC3026
1 IN1 2 IN2 4 SW 6 SHDN 3 GND 11 GND
BST 5 C99 1uF 5.0V
OUT2 10 OUT1 9 1.2V_AVDLL_PLL
ADJ 8 PG 7
R125 2.00K R124 1.00K
C97 22uF C98 2.2uF
2.5V_REG_HPS R116 10.0K

Place near KSZ9021RN PHY

3.3V
R368 DNI ENET_HPS_LED2_LINK R367 1.00K
R379 DNI ENET_HPS_LED1_LINK R378 1.00K
R366 4.70K, 1% ENET_HPS_RXD3 R364 DNI
R365 4.70K, 1% ENET_HPS_RXD2 R363 DNI
R361 4.70K, 1% ENET_HPS_RXD1 R359 DNI
R360 4.70K, 1% ENET_HPS_RXD0 R358 DNI
R351 DNI ENET_HPS_RX_DV R349 4.70K, 1%
R352 4.70K, 1% ENET_HPS_RX_CLK R350 DNI
R344 4.70K, 1% CLK125_NDO_LED_MODE R343 DNI
BOOT-STRAPS

3.3V_REG_HPS
R40 4.70K, 1% ENET_HPS_MDIO 7,20
R50 4.70K, 1% ENET_HPS_MDC 7,20
R39 4.70K, 1% ENET_HPS_INTn 7,20
R38 4.70K, 1% ENET_HPS_RESETn 20,26

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Title: Arria V SoC FPGA Development Kit Board

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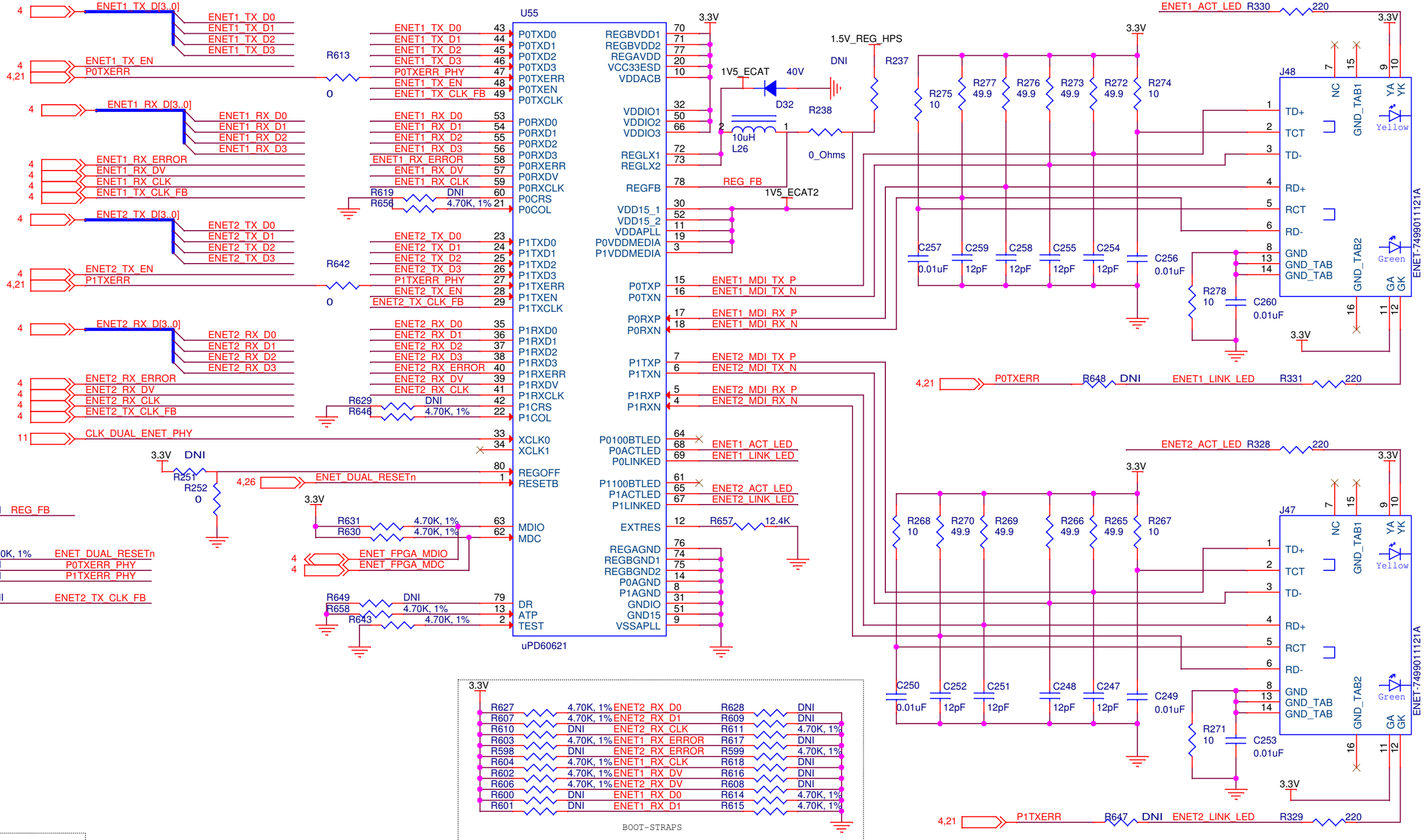
10/100M Ethernet - FPGA



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Title	Arria V SoC FPGA Development Kit Board
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Size: B	Document Number: 150-0320807-C1 (6XX-44209R) Rev: C1
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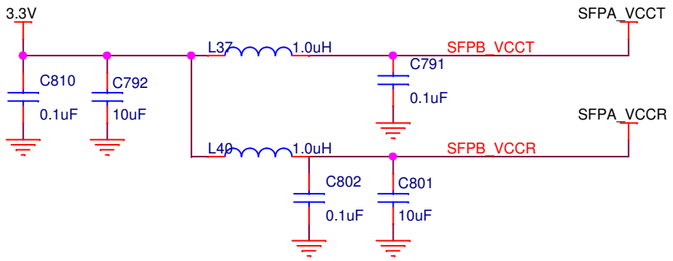
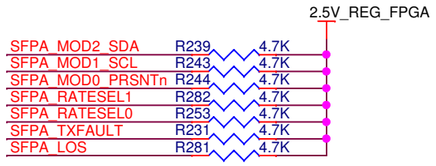
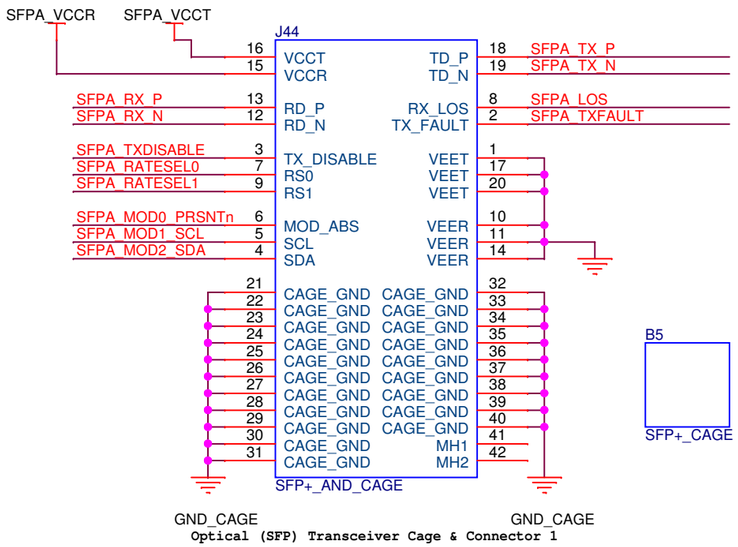
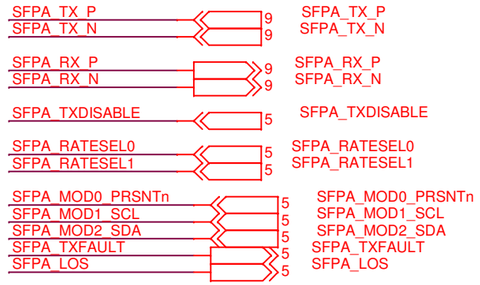
Small Form Factor Pluggable Plus (SFP+) Port A





Optical (SFP+) Transceiver Cage & Connector 0





Optical (SFP) Transceiver Cage & Connector 1

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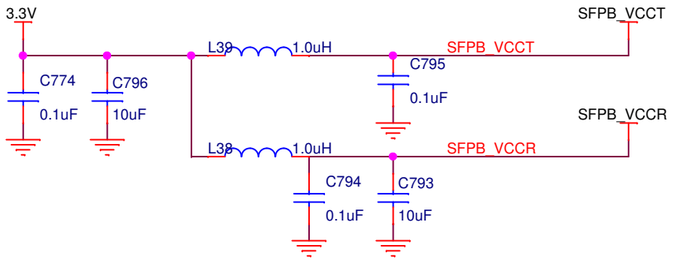
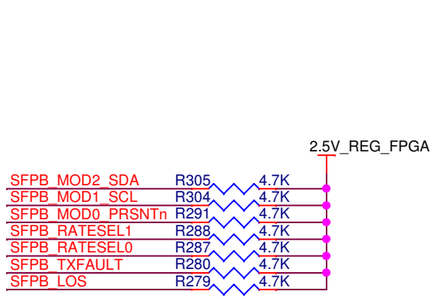
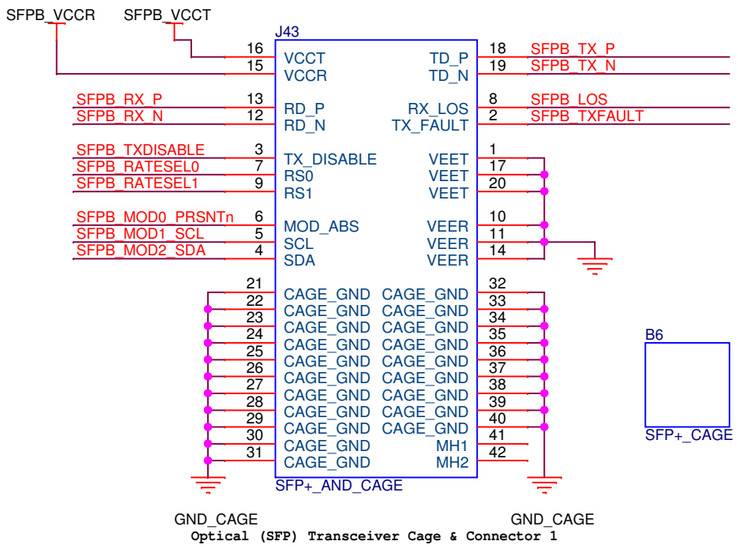
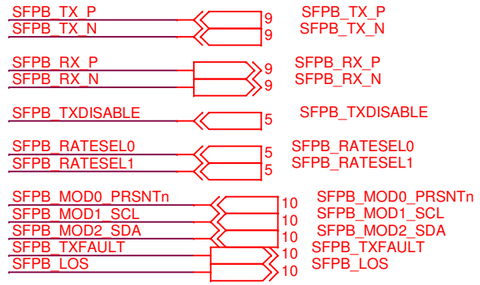
Small Form Factor Pluggable Plus (SFP+) Port B





Optical (SFP+) Transceiver Cage & Connector 0





Optical (SFP) Transceiver Cage & Connector 1

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FMC PORT A

Blue means change from current Altera FMC spec

J26A

DEVCLKB	FMC_LA_RX_CLK_P	G6	LA_P0_CC	LA_P16	G18	FMC_LA_RX_P6	
	FMC_LA_RX_CLK_N	G7	LA_N0_CC	LA_N16	G19	FMC_LA_RX_N6	
DEVCLK	FMC_DEVCLK_P	D8	LA_P1_CC	LA_P17	D20	FMC_LA_RX_P7	
	FMC_DEVCLK_N	D9	LA_N1_CC	LA_N17	D21	FMC_LA_RX_N7	
	FMC_LA_TX_P0	H7	LA_P2	LA_P18_CC	C22		
	FMC_LA_TX_N0	H8	LA_N2	LA_N18_CC	C23		
SYSREF (M->C)	FMC_LA_RX_P0	G9	LA_P3	LA_P19	H22	FMC_LA_TX_P9	
	FMC_LA_RX_N0	G10	LA_N3	LA_N19	H23	FMC_LA_TX_N9	
	FMC_LA_TX_P1	H10			G21	FMC_LA_RX_P8	
	FMC_LA_TX_N1	H11	LA_P4	LA_P20	G22	FMC_LA_RX_N8	
SYSREF (C->M)	FMC_SYSREF_P	D11	LA_N4	LA_N20	H25	FMC_LA_TX_P10	
	FMC_SYSREF_N	D12	LA_P5	LA_P21	H26	FMC_LA_TX_N10	
	FMC_LA_RX_P1	C10	LA_N5	LA_N21	G24	FMC_LA_RX_P9	
	FMC_LA_RX_N1	C11	LA_P6	LA_P22	G25	FMC_LA_RX_N9	
	FMC_LA_TX_P3	H13	LA_N6	LA_N22	D23	FMC_LA_RX_P11	
	FMC_LA_TX_N3	H14	LA_P7	LA_P23	D24	FMC_LA_RX_N11	
			LA_N7	LA_N23			
SYNC (C->M)	FMC_LA_TX_P16	G12			H28	FMC_LA_TX_P12	
	FMC_LA_TX_N16	G13	LA_P8	LA_P24	H29	FMC_LA_TX_N12	
	FMC_LA_TX_P4	D14	LA_N8	LA_N24	G27	FMC_LA_RX_P10	
	FMC_LA_TX_N4	D15	LA_P9	LA_N25	G28	FMC_LA_RX_N10	
	FMC_LA_RX_P3	C14	LA_N9	LA_P25	D26	FMC_LA_TX_P13	
	FMC_LA_RX_N3	C15	LA_P10	LA_N25	D27	FMC_LA_TX_N13	
	FMC_LA_TX_P5	H16	LA_N10	LA_P26	C26		
	FMC_LA_TX_N5	H17	LA_P11	LA_N26	C27		
			LA_N11	LA_P27			
	FMC_LA_RX_P4	G15		LA_N27	H31	FMC_LA_TX_P17	
	FMC_LA_RX_N4	G16	LA_P12	LA_P28	H32	FMC_LA_TX_N17	
	FMC_LA_TX_P6	D17	LA_N12	LA_N28	G30	FMC_LA_TX_P12	
	FMC_LA_TX_N6	D18	LA_P13	LA_P29	G31	FMC_LA_RX_N12	
	FMC_LA_RX_P5	C18	LA_N13	LA_N29	H34	FMC_LA_TX_P14	
	FMC_LA_RX_N5	C19	LA_P14	LA_P30	H35	FMC_LA_TX_N14	
	FMC_LA_TX_P7	H19	LA_N14	LA_N30	G33	FMC_LA_RX_P13	
	FMC_LA_TX_N7	H20	LA_P15	LA_P31	G34	FMC_LA_RX_N13	
			LA_N15	LA_N31	H37	FMC_LA_TX_P15	
				LA_P32	H38	FMC_LA_TX_N15	
				LA_N32	G36	FMC_LA_RX_P14	
				LA_P33	G37	FMC_LA_RX_N14	
				LA_N33			

ASP-134486-01

Alt. DEVCLKB

Alt. DEVCLK

Alt. SYSREF (M->C)

Alt. SYSREF (C->M)

Alt. SYNC (C->M)

FMC INTERFACE

FMC_LA_RX_CLK_P 10
FMC_LA_RX_CLK_N 10
FMC_LA_TX_CLK_P 8
FMC_LA_TX_CLK_N 8
FMC_LA_RX_P[15:0] 8,10
FMC_LA_RX_N[15:0] 8,10
FMC_LA_TX_P[17:0] 8
FMC_LA_TX_N[17:0] 8
FMC_CLK_M2C_P[1:0] 10
FMC_CLK_M2C_N[1:0] 10
FMC_DP_C2M_P[7:0] 9
FMC_DP_C2M_N[7:0] 9
FMC_DP_M2C_P[7:0] 9
FMC_DP_M2C_N[7:0] 9
FMC_GA[1:0] 8
FMC_C2M_PG 19
FMC_GPIO[7:0] 8

J26C

K25	HB_P0_CC	HB_P11	J30
K26	HB_N0_CC	HB_N11	J31
J24	HB_P1	HB_P12	F31
J25	HB_N1	HB_N12	F32
F22	HB_P2	HB_P13	E30
F23	HB_N2	HB_N13	E31
E21	HB_P3	HB_P14	K34
E22	HB_N3	HB_N14	K35
F25			J33
F26	HB_P4	HB_P15	J34
E24	HB_N4	HB_N15	F34
E25	HB_P5	HB_P16	F35
K28	HB_N5	HB_N16	K37
K29	HB_P6_CC	HB_P17_CC	K38
J27	HB_N6_CC	HB_N17_CC	J36
J28	HB_P7	HB_P18	J37
	HB_N7	HB_N18	
F28			E33
F29	HB_P8	HB_P19	E34
E27	HB_N8	HB_N19	F37
E28	HB_P9	HB_P20	F38
K31	HB_N9	HB_N20	E36
K32	HB_P10	HB_P21	E37
	HB_N10	HB_N21	

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J26B

F4	HA_P0_CC	HA_P12	F13
F5	HA_N0_CC	HA_N12	F14
E2	HA_P1_CC	HA_P13	E12
E3	HA_N1_CC	HA_N13	E13
K7	HA_P2	HA_P14	J15
K8	HA_N2	HA_N14	J16
J6	HA_P3	HA_P15	F16
J7	HA_N3	HA_N15	F17
F7			E15
F8	HA_P4	HA_P16	E16
E6	HA_N4	HA_N16	K16
E7	HA_P5	HA_P17_CC	K17
K10	HA_N5	HA_N17_CC	J18
K11	HA_P6	HA_P18	J19
J9	HA_N6	HA_N18	F19
J10	HA_P7	HA_P19	F20
	HA_N7	HA_N19	
F10			E18
F11	HA_P8	HA_P20	E19
E9	HA_N8	HA_N20	K19
E10	HA_P9	HA_P21	K20
K13	HA_N9	HA_N21	J21
K14	HA_P10	HA_P22	J22
J12	HA_N10	HA_N22	K22
J13	HA_P11	HA_P23	K23
	HA_N11	HA_N23	

ASP-134486-01

Alt. SYNC (M->C)

SYNC (M->C)

FMC_LA_RX_P15
FMC_LA_RX_N15
FMC_LA_RX_P2
FMC_LA_RX_N2
FMC_GPIO0
FMC_GPIO1
FMC_GPIO2
FMC_GPIO3
FMC_GPIO4
FMC_GPIO5
FMC_GPIO6
FMC_GPIO7

TRANSLATOR

J26F

E20	GND		
E23	GND	GND	E17
E26	GND	GND	E14
E29	GND	GND	E11
E38	GND	GND	E8
E32	GND	GND	E5
E35	GND	GND	E4
E40	GND	GND	E1
K2	GND	GND	F39
K3	GND	GND	F36
K6	GND	GND	F33
K9	GND	GND	F30
K12	GND	GND	F27
K15	GND	GND	F24
K18	GND	GND	F21
K21	GND	GND	F18
K24	GND	GND	F15
K27	GND	GND	F12
K30	GND	GND	F9
K33	GND	GND	F6
K36	GND	GND	F3
K39	GND	GND	F2
J1	GND	GND	G40
J4	GND	GND	G38
J5	GND	GND	G35
J8	GND	GND	G32
J11	GND	GND	G29
J14	GND	GND	G26
J17	GND	GND	G23
J20	GND	GND	G20
J23	GND	GND	G17
J26	GND	GND	G14
J29	GND	GND	G11
J32	GND	GND	G8
J35	GND	GND	G5
J38	GND	GND	G4
J40	GND	GND	G1
H3	GND	GND	A40
H6	GND	GND	A37
H9	GND	GND	A36
H12	GND	GND	A33
H15	GND	GND	A32
H18	GND	GND	A29
H21	GND	GND	A28
H24	GND	GND	A25
H27	GND	GND	A24
H30	GND	GND	A21
H33	GND	GND	A20
H36	GND	GND	A17
H39	GND	GND	A16
D2	GND	GND	A13
D3	GND	GND	A12
D6	GND	GND	A9
D7	GND	GND	A8
D10	GND	GND	A5
D13	GND	GND	A4
D16	GND	GND	A1
D19	GND	GND	B39
D22	GND	GND	B38
D25	GND	GND	B35
D28	GND	GND	B34
D37	GND	GND	B31
D39	GND	GND	B30
C1	GND	GND	B27
C4	GND	GND	B26
C5	GND	GND	B23
C8	GND	GND	B22
C9	GND	GND	B19
C12	GND	GND	B18
C13	GND	GND	B15
C16	GND	GND	B14
C17	GND	GND	B11
C20	GND	GND	B10
C21	GND	GND	B7
C24	GND	GND	B6
C25	GND	GND	B3
C28	GND	GND	B2
C29	GND	GND	C40
C32	GND	GND	C38
C33	GND	GND	C36

ASP-134486-01

FMC_SYSREF_N
FMC_SYSREF_P
0 R4007
0 R4009
FMC_LA_TX_N2
FMC_LA_TX_P2
DNI R4008
DNI R4010
LMK_SYSREF_FMC_P
LMK_SYSREF_FMC_N
12
12

FMC_DEVCLK_N
FMC_DEVCLK_P
0 R4003
0 R4004
FMC_LA_TX_CLK_N
FMC_LA_TX_CLK_P
DNI R4005
DNI R4006
LMK_CLK_FMC_P
LMK_CLK_FMC_N
12
12

J26D

FMC_DP_C2M_P0	C2	DP0_C2M_P	DP0_M2C_P	C6	FMC_DP_M2C_P0		
FMC_DP_C2M_N0	C3	DP0_C2M_N	DP0_M2C_N	C7	FMC_DP_M2C_N0		
FMC_DP_C2M_P1	A22	DP1_C2M_P	DP1_M2C_P	A2	FMC_DP_M2C_P1		
FMC_DP_C2M_N1	A23	DP1_C2M_N	DP1_M2C_N	A3	FMC_DP_M2C_N1		
FMC_DP_C2M_P2	A26	DP2_C2M_P	DP2_M2C_P	A6	FMC_DP_M2C_P2		
FMC_DP_C2M_N2	A27	DP2_C2M_N	DP2_M2C_N	A7	FMC_DP_M2C_N2		
FMC_DP_C2M_P3	A30	DP3_C2M_P	DP3_M2C_P	A10	FMC_DP_M2C_P3		
FMC_DP_C2M_N3	A31	DP3_C2M_N	DP3_M2C_N	A11	FMC_DP_M2C_N3		
FMC_DP_C2M_P4	A34	DP4_C2M_P	DP4_M2C_P	A14	FMC_DP_M2C_P4		
FMC_DP_C2M_N4	A35	DP4_C2M_N	DP4_M2C_N	A15	FMC_DP_M2C_N4		
FMC_DP_C2M_P5	A38	DP5_C2M_P	DP5_M2C_P	A18	FMC_DP_M2C_P5		
FMC_DP_C2M_N5	A39	DP5_C2M_N	DP5_M2C_N	A19	FMC_DP_M2C_N5		
FMC_DP_C2M_P6	B36	DP6_C2M_P	DP6_M2C_P	B16	FMC_DP_M2C_P6		
FMC_DP_C2M_N6	B37	DP6_C2M_N	DP6_M2C_N	B17	FMC_DP_M2C_N6		
FMC_DP_C2M_P7	B32	DP7_C2M_P	DP7_M2C_P	B12	FMC_DP_M2C_P7		
FMC_DP_C2M_N7	B33	DP7_C2M_N	DP7_M2C_N	B13	FMC_DP_M2C_N7		
	B28	DP8_C2M_P	DP8_M2C_P	B8			
	B29	DP8_C2M_N	DP8_M2C_N	B9			
	B24	DP9_C2M_P	DP9_M2C_P	B4			
	B25	DP9_C2M_N	DP9_M2C_N	B5			
			GBTCLK0_M2C_P	D4	FMC_GBTCLK_M2C_P0	9	
			GBTCLK0_M2C_N	D5	FMC_GBTCLK_M2C_N0	9	
			GBTCLK1_M2C_P	B20	FMC_GBTCLK_M2C_P1	9	
			GBTCLK1_M2C_N	B21	FMC_GBTCLK_M2C_N1	9	

ASP-134486-01

J26E

3.3V	D32	3P3VAUX	VADJ	E39	VAR_VCCIOP
			VADJ	F40	
	D40	3P3V	VADJ	G39	
	C39	3P3V	VADJ	H40	
	D36	3P3V			
	D38	3P3V	VIO_B_M2C	K40	
			VIO_B_M2C	J39	
12V	C35	12P0V	VREF_B_M2C	K1	VREF_FMC
	C37	12P0V	VREF_A_M2C	H1	
					PG_M2C only on High Pincount versions.
3.3V R90 10.0K	FMC_C2M_PG D1	PG_C2M	PG_M2C	F1	FMC_M2C_PG R89 10.0K 3.3V
8,28	FMC_PRSNTn H2	PRSNT_M2C_L			
			TRST	D34	FMC_JTAG_RST R184 10.0K
8	FMC_SDA C31	SDA	TMS	D33	FMC_JTAG_TMS 14
8	FMC_SCL C30	SCL	TDO	D31	FMC_JTAG_TDO 14
			TDI	D30	FMC_JTAG_TDI 14
			TCK	D29	JTAG_MUX_TCK 13,14,19,25
CLK2_BIDIR, CLK3_BIDIR, and CLK_DIR only on High Pincount versions.	K4	CLK2_BIDIR_P			
	K5	CLK2_BIDIR_N			
	J2	CLK3_BIDIR_P	CLK0_M2C_P	H4	FMC_CLK_M2C_P0
	J3	CLK3_BIDIR_N	CLK0_M2C_N	H5	FMC_CLK_M2C_N0
			CLK1_M2C_P	G2	FMC_CLK_M2C_P1
	B1	CLK_DIR	CLK1_M2C_N	G3	FMC_CLK_M2C_N1
FMC_GA0	C34	GA0	RES0	B40	
FMC_GA1	D35	GA1			

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VAR_VCCIOP
R88 DNI
VREF_FMC
C67 0.1uF
C66 0.1uF
R87 DNI

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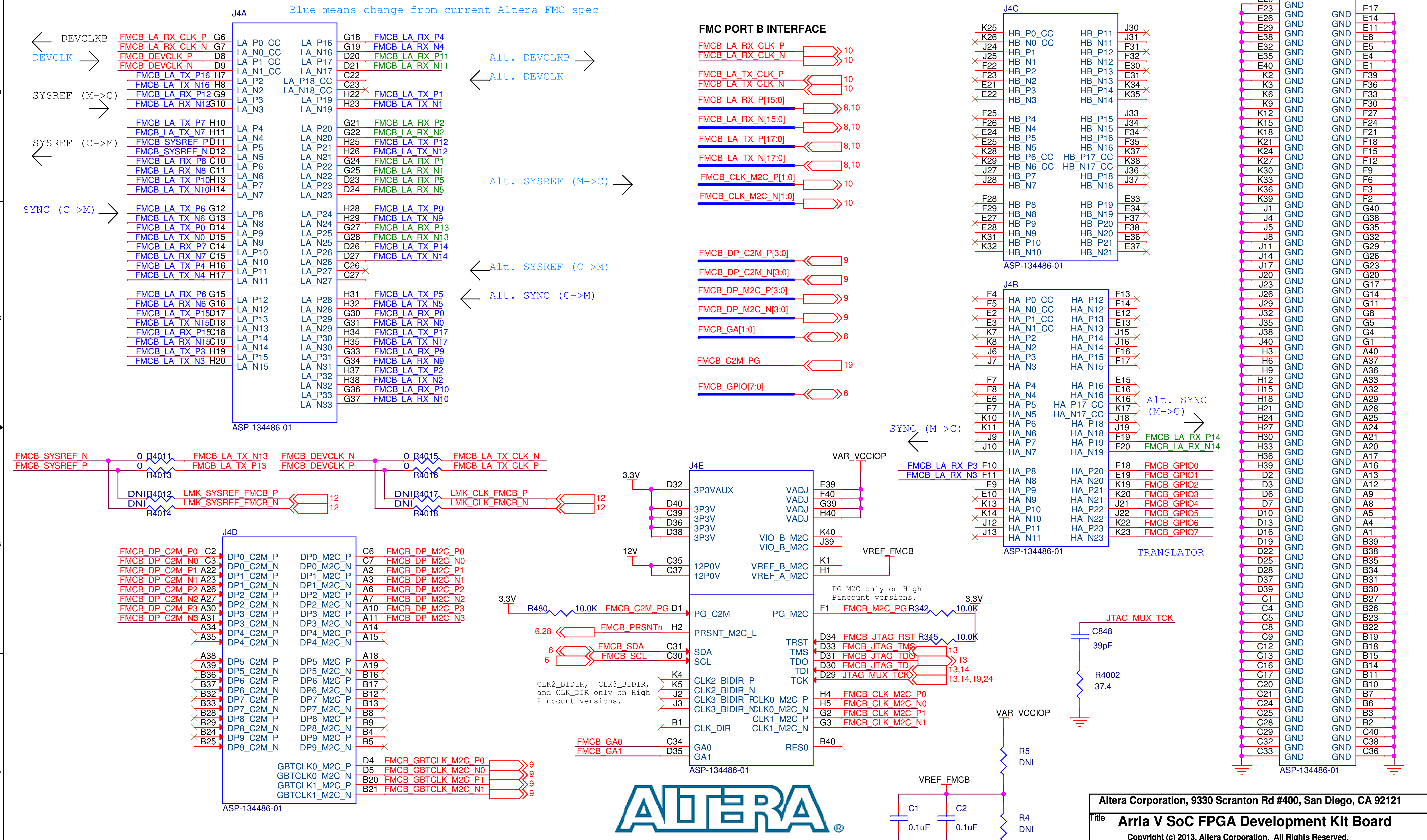
Date: Thursday, December 12, 2013	Sheet 24 of 45		

FMC PORT B



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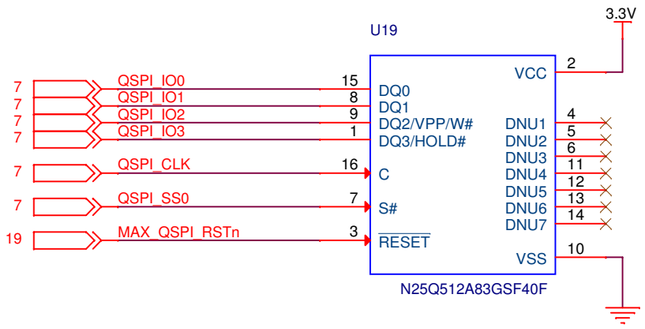
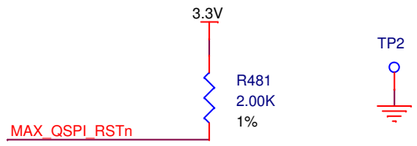
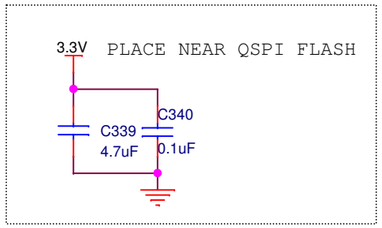
QSPI Flash & Reset Circuit

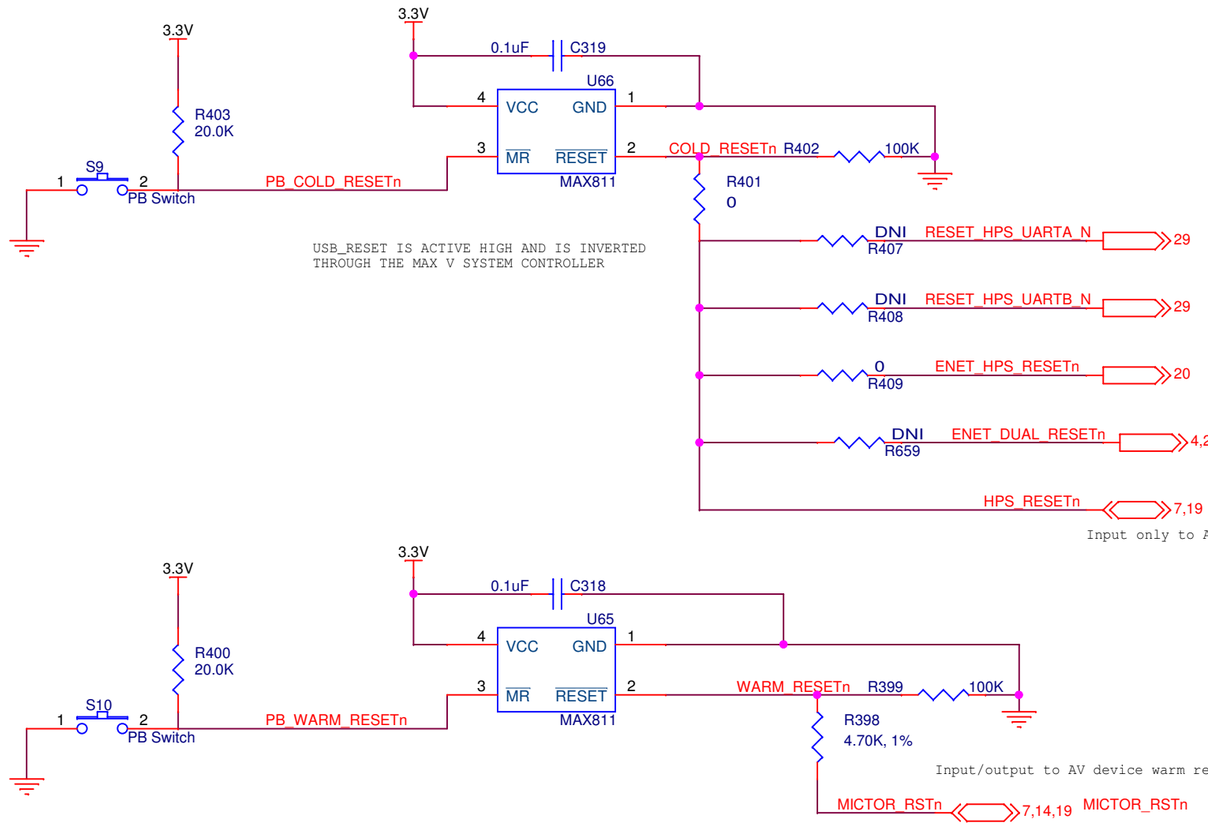
QSPI FLASH







RESET CIRUIT



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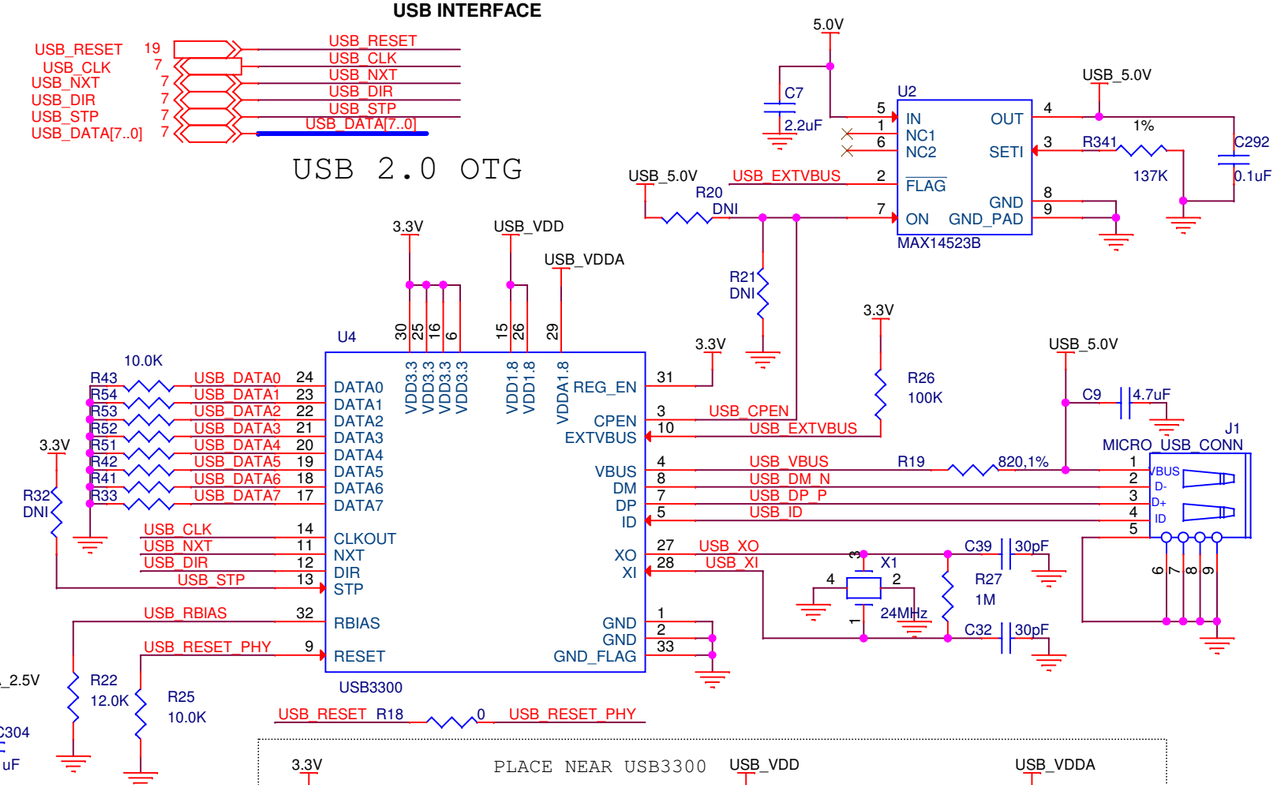
USB 2.0 OTG , Micro SD Card

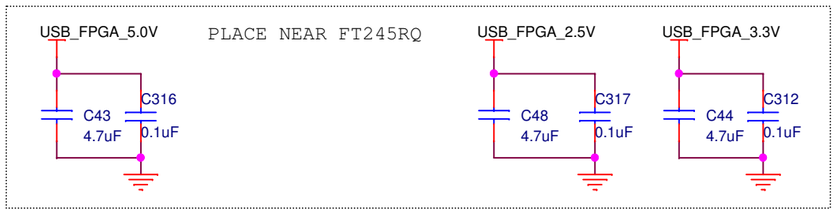
Current limit for Rseti of 137k is 1.013A

USB INTERFACE

USB_RESET 19 → USB_RESET
USB_CLK 7 → USB_CLK
USB_NXT 7 → USB_NXT
USB_DIR 7 → USB_DIR
USB_STP 7 → USB_STP
USB_DATA[7..0] 7 → USB_DATA[7..0]

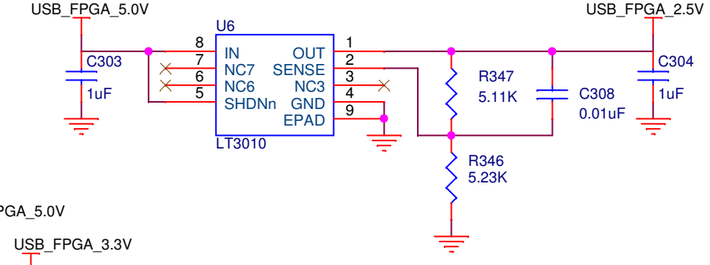
USB 2.0 OTG



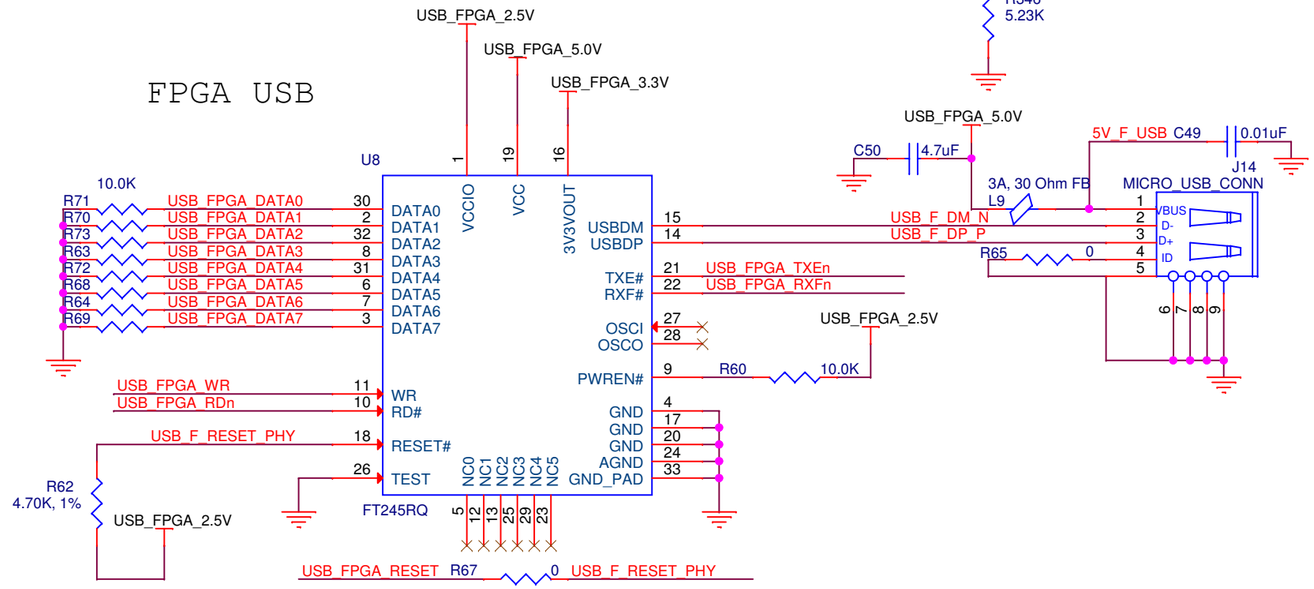


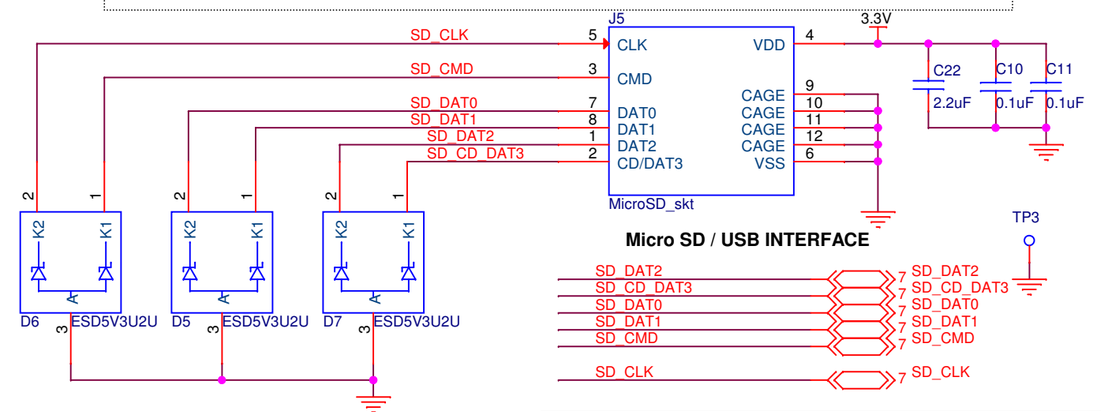
USB FPGA INTERFACE

USB_FPGA_RESET 19 → USB_FPGA_RESET
USB_FPGA_WR 8 → USB_FPGA_WR
USB_FPGA_RDn 8 → USB_FPGA_RDn
USB_FPGA_TXEn 8 → USB_FPGA_TXEn
USB_FPGA_RXFn 13 → USB_FPGA_RXFn
USB_FPGA_DATA[7..0] 8,10 → USB_FPGA_DATA[7..0]



FPGA USB





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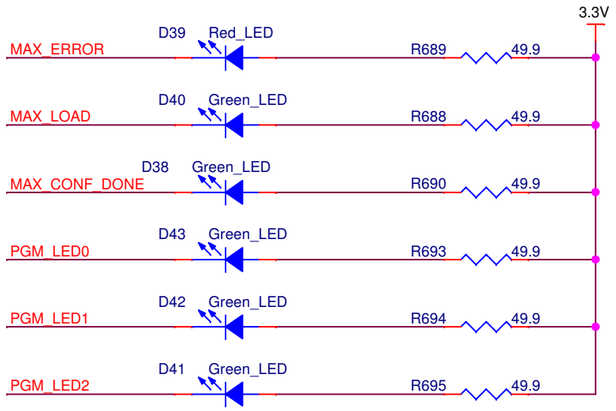
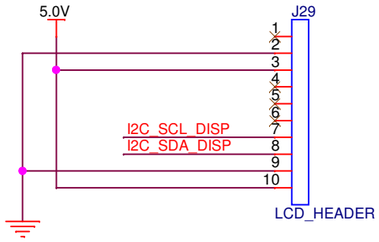
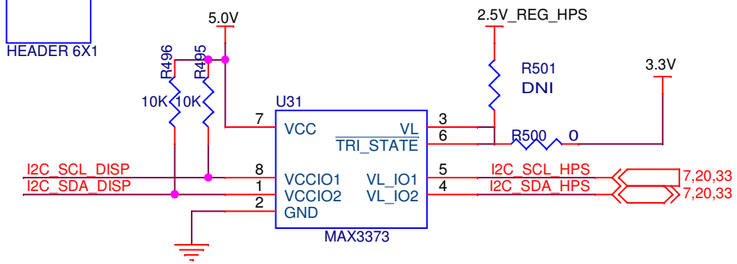
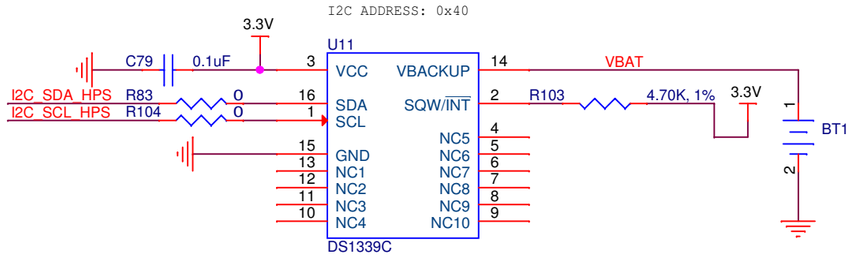
User I/O, RTC

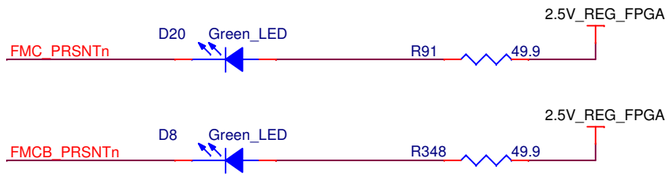


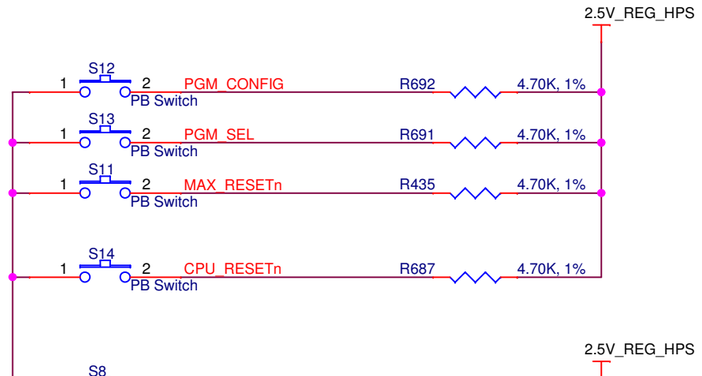
Note to assembler: Use this resistor to attach to LCD Header (follow assembly instructions).

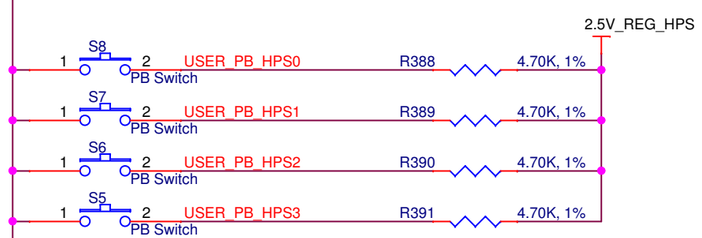


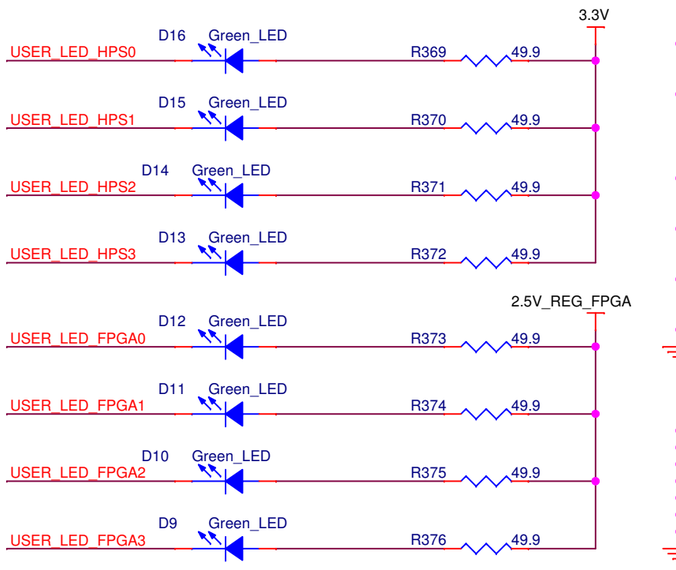


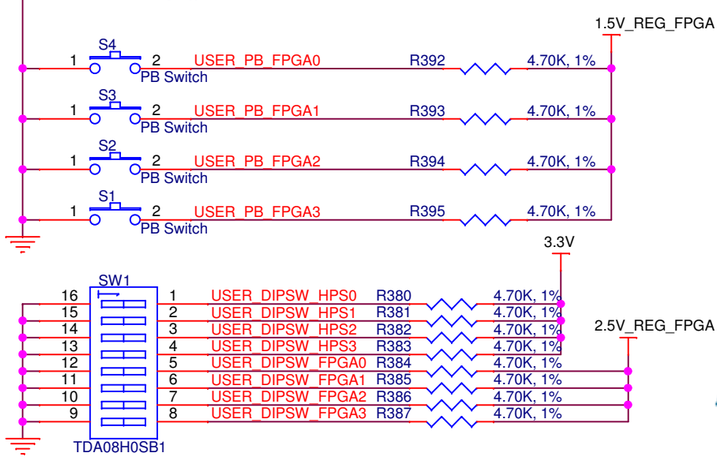


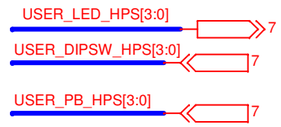


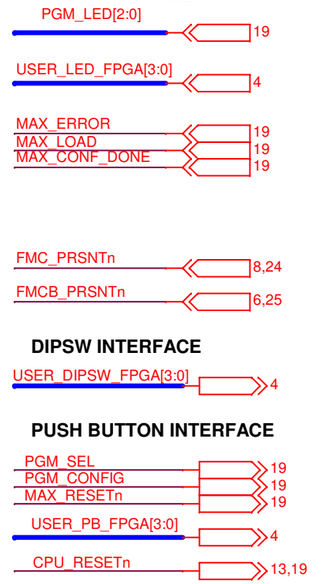












ALTERA®

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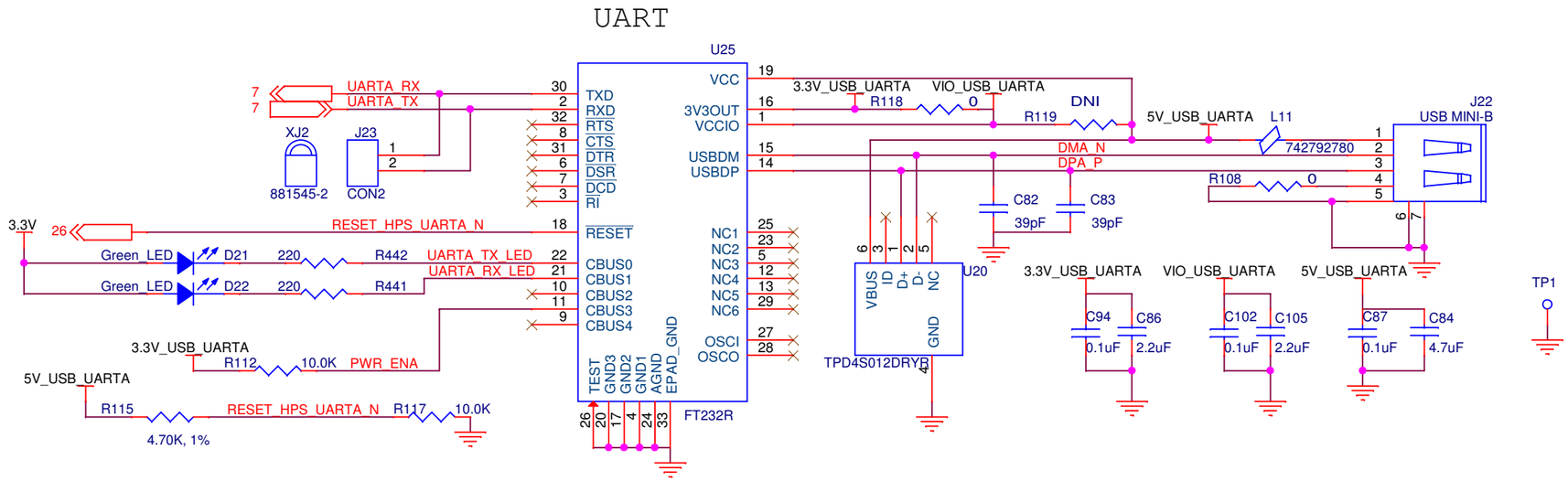
UARTS PORT A and PORT B



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On-Board USB Blaster II

J50
USB MINI-B
1 VBUS_5V
2 FX2_D_N
3 FX2_D_P
4 R315 DNI
5
7 6

U63
TPD2EUSB30
3 GND D+ 1
D- 2
1M R334
4.7nF C287

Y7
24.00MHz
C266 12pF
C267 12pF

FX2_SDA R662 0 MAX_SDA
3.3V
C246 0.1uF
U57
MAX811
GND VCC
RESET MR
100K R264 FX2_RESETn

U61
CY7C68013A_VFBGA
3.3V
AVCC RESET B8 FX2_RESETn
AVCC SCL F3 FX2_SCL
SDA G3 FX2_SDA
R679 2.00K
R677 2.00K
3.3V
VCC WAKEUP B7 FX2_WAKEUP
CTL0 H7 FX2_FLAGA
CTL1 G7 FX2_FLAGB
CTL2 H8 FX2_FLAGC
DMINUS RDY0 A1 FX2_SLRDn
DPLUS RDY1 B1 FX2_SLWRn
USB_B2_CLK IFCLK CLKOUT B2
24M_XTALIN XTALIN
24M_XTALOUT XTALOUT
PA0 PB0 H3 FX2_PB0
FX2_PA1 PA1 PB1 F4 FX2_PB1
FX2_PA2 PA2 PB2 H4 FX2_PB2
FX2_PA3 PA3 PB3 G4 FX2_PB3
FX2_PA4 PA4 PB4 H5 FX2_PB4
FX2_PA5 PA5 PB5 G5 FX2_PB5
FX2_PA6 PA6 PB6 F5 FX2_PB6
FX2_PA7 PA7 PB7 H6 FX2_PB7
RESERVED PD0 A8 FX2_PD0
PD1 A7 FX2_PD1
AGND PD2 B6 FX2_PD2
AGND PD3 A6 FX2_PD3
PD4 B3 FX2_PD4
PD5 A3 FX2_PD5
PD6 C3 FX2_PD6
PD7 A2 FX2_PD7
GND

VBUS_5V R685 10.0K FX2_WAKEUP
R686 20.0K C842 0.1uF

PLACE NEAR CY7C68013A
3.3V
C837 C835 C833 C843 C831 C832 C836 C841
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

1V8
JTAG_RX D35 RESn_JTAG_RX R651 56.2
Green_LED
JTAG_TX D36 RESn_JTAG_TX R650 56.2
Green_LED
SC_RX D34 RESn_SC_RX R652 56.2
Green_LED
SC_TX D33 RESn_SC_TX R653 56.2
Green_LED

1.5V_REG_HPS
R672 1.00K USB_SCL
R670 1.00K USB_SDA
R673 1.00K USB_FULL
R671 1.00K USB_EMPTY
R669 1.00K FACTORY_REQUEST

3.3V
J51
DNI
R362 1.00K C_USB_MAX_TCK 1 2
C_USB_MAX_TDO 3 4
R377 1.00K C_USB_MAX_TMS 5 6
7 8
C_USB_MAX_TDI 9 10
3.3V

U56B
MAX II BANK 1
EPM570GF100
FX2_PA2 B1 IO_B1_B1 IO_B1_H8 H8 FX2_PB1
FX2_FLAGC C1 IO_B1_C1 IO_B1_J3 J3 FX2_PB3
FX2_PA7 C2 IO_B1_C2 IO_B1_J4 J4 FX2_SCL
FX2_FLAGA D1 IO_B1_D1 IO_B1_J5 J5 FX2_PD6
FX2_PA3 D2 IO_B1_D2 IO_B1_J6 J6 FX2_PD4
FX2_PA4 D3 IO_B1_D3 IO_B1_J8 J8
EXTRA_SIG0 E3 IO_B1_E3 IO_B1_J9 J9 FX2_SLWRn
FX2_PB4 F1 IO_B1_F1 IO_B1_K1 K1 FX2_SLRDn
FX2_PA6 F2 IO_B1_F2 IO_B1_K2 K2 FX2_PD7
FX2_PB2 F3 IO_B1_F3 IO_B1_K3 K3 FX2_PD5
FX2_FLAGB G1 IO_B1_G1 IO_B1_K4 K4 FX2_PA5
FX2_PB0 G2 IO_B1_G2 IO_B1_K5 K5 C_JTAG_TDO
FX2_PA1 G3 IO_B1_G3 IO_B1_K6 K6 C_JTAG_TMS
FX2_PB5 H1 IO_B1_H1 IO_B1_K7 K7 C_JTAG_TDI
USB_DISABLEn H4 IO_B1_H4 IO_B1_K8 K8 C_JTAG_TCK
FX2_PB6 H7 IO_B1_H7 IO_B1_K10 K10

U56D
MAX II CONFIGURATION
EPM570GF100
MAX_SDA J7 IO1/DEV_OE IO1/DEV_CLRn K9 FX2_RESETn
C_USB_MAX_TDI H2 TDI IO1/GCLK0p E2 USB_B2_CLK
C_USB_MAX_TCK H3 TCK IO1/GCLK1p E1 FX2_PB7
C_USB_MAX_TMS J1 TMS IO2/GCLK2p F8 USB_CFG7
C_USB_MAX_TDO J2 TDO IO2/GCLK3p E10 M570_CLOCK

U56C
MAX II BANK 2
EPM570GF100
JTAG_TX A1 IO_B2_A1 IO_B2_C3 C3 USB_CFG3
JTAG_RX A2 IO_B2_A2 IO_B2_C4 C4 M570_PCIE_JTAG_EN
FACTORY_REQUEST A3 IO_B2_A3 IO_B2_A6 A6 USB_B2_DATA7
USB_CFG5 A4 IO_B2_A4 IO_B2_F10 F10 USB_B2_DATA5
USB_RESETn A7 IO_B2_A7 IO_B2_F9 F9 USB_B2_DATA6
USB_OEn B8 IO_B2_B8 IO_B2_B10 B10 RST
USB_RDn D10 IO_B2_D10 IO_B2_E8 E8 USB_CFG8
USB_WRn D9 IO_B2_D9 IO_B2_C10 C10 TRST
FACTORY_STATUS A9 IO_B2_A9 IO_B2_D8 D8 USB_FULL
SC_RX A10 IO_B2_A10 IO_B2_B6 B6 USB_EMPTY
SC_TX B2 IO_B2_B2 IO_B2_E9 E9 USB_CFG11
USB_CFG4 B3 IO_B2_B3 IO_B2_A8 A8 USB_SCL
EXTRA_SIG1 B4 IO_B2_B4 IO_B2_A5 A5 USB_SDA
USB_CFG6 B5 IO_B2_B5 IO_B2_G8 G8 EXTRA_SIG2
USB_B2_DATA0 B9 IO_B2_B9 IO_B2_G9 G9 USB_CFG10
USB_B2_DATA1 C9 IO_B2_C9 IO_B2_G10 G10 USB_CFG0 V77
USB_B2_DATA2 C8 IO_B2_C8 IO_B2_H9 H9 USB_CFG1 V81
USB_B2_DATA3 B7 IO_B2_B7 IO_B2_H10 H10 USB_CFG2 V80
USB_B2_DATA4 C7 IO_B2_C7 IO_B2_J10 J10 USB_CFG9

C_USB_MAX_TCK R684 0 FX2_PD0
C_USB_MAX_TDI R682 0 FX2_PD2
C_USB_MAX_TDO R666 0 FX2_PD3
C_USB_MAX_TMS R683 0 FX2_PD1

C_JTAG_TCK 0 R660 JTAG_TCK
C_JTAG_TMS 0 R661 JTAG_TMS
C_JTAG_TDI 0 R664 JTAG_BLASTER_TDI
C_JTAG_TDO 0 R665 JTAG_BLASTER_TDO

2.5V_REG_HPS
R645 DNI JTAG_BLASTER_TDI

TRST 19
RST 19

U56A
MAX II POWER
GNDINT VCCINT C6
C5 GNDINT VCCINT E7
E6 GNDINT VCCINT F4
F5 GNDINT VCCINT H6
H5 GNDINT VCCINT
D5 GNDIO VCCIO1 E4
D7 GNDIO VCCIO1 G4
E5 GNDIO VCCIO1 G6
F6 GNDIO
G5 GNDIO VCCIO2 D4
G7 GNDIO VCCIO2 D6
VCCIO2 F7
1V8
3.3V
1.5V_REG_HPS

PLACE NEAR MAX II (U14)
3.3V 1.5V_REG_HPS 1V8
C825 C826 C827 C829 C828 C830
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

FPGA USB INTERFACE

USB_B2_DATA[7:0] 4 USB_B2_DATA[7:0]
USB_FULL 4 USB_FULL
USB_EMPTY 4 USB_EMPTY
USB_SCL 4 USB_SCL
USB_SDA 4 USB_SDA
USB_B2_CLK 4,19 USB_B2_CLK
USB_RESETn 4 USB_RESETn
USB_OEn 4 USB_OEn
USB_RDn 4 USB_RDn
USB_WRn 4 USB_WRn
M570_PCIE_JTAG_EN 19 M570_PCIE_JTAG_EN

MAX V USB INTERFACE

USB_CFG[11:0] 19 USB_CFG[11:0]
EXTRA_SIG[2:0] 19 EXTRA_SIG[2:0]
USB_DISABLEn 14 USB_DISABLEn
M570_CLOCK 19 M570_CLOCK
FACTORY_STATUS 19 FACTORY_STATUS
FACTORY_REQUEST 19 FACTORY_REQUEST

JTAG INTERFACE

JTAG_TCK 14 JTAG_TCK
JTAG_TMS 14 JTAG_TMS
JTAG_BLASTER_TDI 14 JTAG_BLASTER_TDI
JTAG_BLASTER_TDO 14 JTAG_BLASTER_TDO

ALTERA

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Title: Arria V SoC FPGA Development Kit Board

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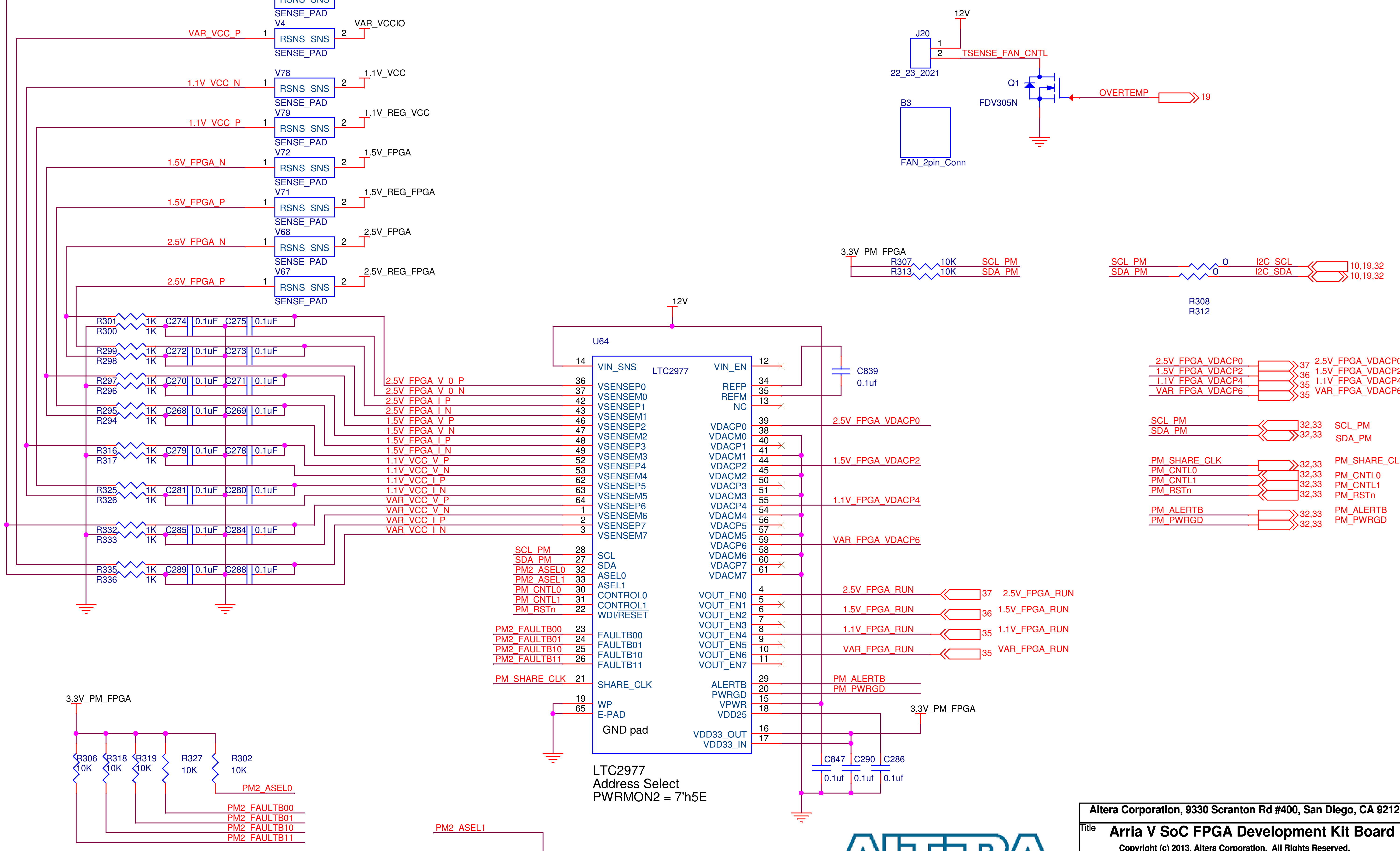
FPGA Power Monitor 1



V1
VAR_VCC_N
VAR_VCCIOP
V4
VAR_VCC_P
VAR_VCCIO
V78
1.1V_VCC_N
1.1V_VCC
V79
1.1V_VCC_P
1.1V_REG_VCC
V72
1.5V_FPGA_N
1.5V_FPGA
V71
1.5V_FPGA_P
1.5V_REG_FPGA
V68
2.5V_FPGA_N
2.5V_FPGA
V67
2.5V_FPGA_P
2.5V_REG_FPGA
RSNS SNS
SENSE_PAD
R301 R300 R299 R298 R297 R296 R295 R294 R316 R317 R325 R326 R332 R333 R335 R336
1K
C274 C275 C272 C273 C270 C271 C268 C269 C279 C278 C281 C280 C285 C284 C289 C288
0.1uF
2.5V_FPGA_V_0_P
2.5V_FPGA_V_0_N
2.5V_FPGA_I_P
2.5V_FPGA_I_N
1.5V_FPGA_V_P
1.5V_FPGA_V_N
1.5V_FPGA_I_P
1.5V_FPGA_I_N
1.1V_VCC_V_P
1.1V_VCC_V_N
1.1V_VCC_I_P
1.1V_VCC_I_N
VAR_VCC_V_P
VAR_VCC_V_N
VAR_VCC_I_P
VAR_VCC_I_N
12V
U64
LTC2977
VIN_SNS
VSENSEP0 VSENSEM0 VSENSEP1 VSENSEM1 VSENSEP2 VSENSEM2 VSENSEP3 VSENSEM3 VSENSEP4 VSENSEM4 VSENSEP5 VSENSEM5 VSENSEP6 VSENSEM6 VSENSEP7 VSENSEM7
SCL SDA ASEL0 ASEL1 CONTROL0 CONTROL1 WDI/RESET
FAULTB00 FAULTB01 FAULTB10 FAULTB11
SHARE_CLK
WP
E-PAD
GND pad
VIN_EN REFP REFM NC
VDACP0 VDACM0 VDACP1 VDACM1 VDACP2 VDACM2 VDACP3 VDACM3 VDACP4 VDACM4 VDACP5 VDACM5 VDACP6 VDACM6 VDACP7 VDACM7
VOUT_EN0 VOUT_EN1 VOUT_EN2 VOUT_EN3 VOUT_EN4 VOUT_EN5 VOUT_EN6 VOUT_EN7
ALERTB PWRGD VPWR VDD25 VDD33_OUT VDD33_IN
C839 0.1uf
SCL_PM
SDA_PM
PM2_ASEL0
PM2_ASEL1
PM_CNTL0
PM_CNTL1
PM_RSTn
PM2_FAULTB00
PM2_FAULTB01
PM2_FAULTB10
PM2_FAULTB11
PM_SHARE_CLK
2.5V_FPGA_VDACP0
1.5V_FPGA_VDACP2
1.1V_FPGA_VDACP4
VAR_FPGA_VDACP6
2.5V_FPGA_RUN 37
1.5V_FPGA_RUN 36
1.1V_FPGA_RUN 35
VAR_FPGA_RUN 35
PM_ALERTB
PM_PWRGD
3.3V_PM_FPGA
C847 C290 C286 0.1uf
LTC2977
Address Select
PWRMON2 = 7'h5E
R306 R318 R319 R327 R302
10K
J20
22_23_2021
TSENSE_FAN_CNTL
Q1
FDV305N
OVERTEMP 19
B3
FAN_2pin_Conn
R307 R313 10K
R308 R312 0
I2C_SCL 10,19,32
I2C_SDA 10,19,32
2.5V_FPGA_VDACP0 37
1.5V_FPGA_VDACP2 36
1.1V_FPGA_VDACP4 35
VAR_FPGA_VDACP6 35
SCL_PM 32,33
SDA_PM 32,33
PM_SHARE_CLK 32,33
PM_CNTL0 32,33
PM_CNTL1 32,33
PM_RSTn 32,33
PM_ALERTB 32,33
PM_PWRGD 32,33

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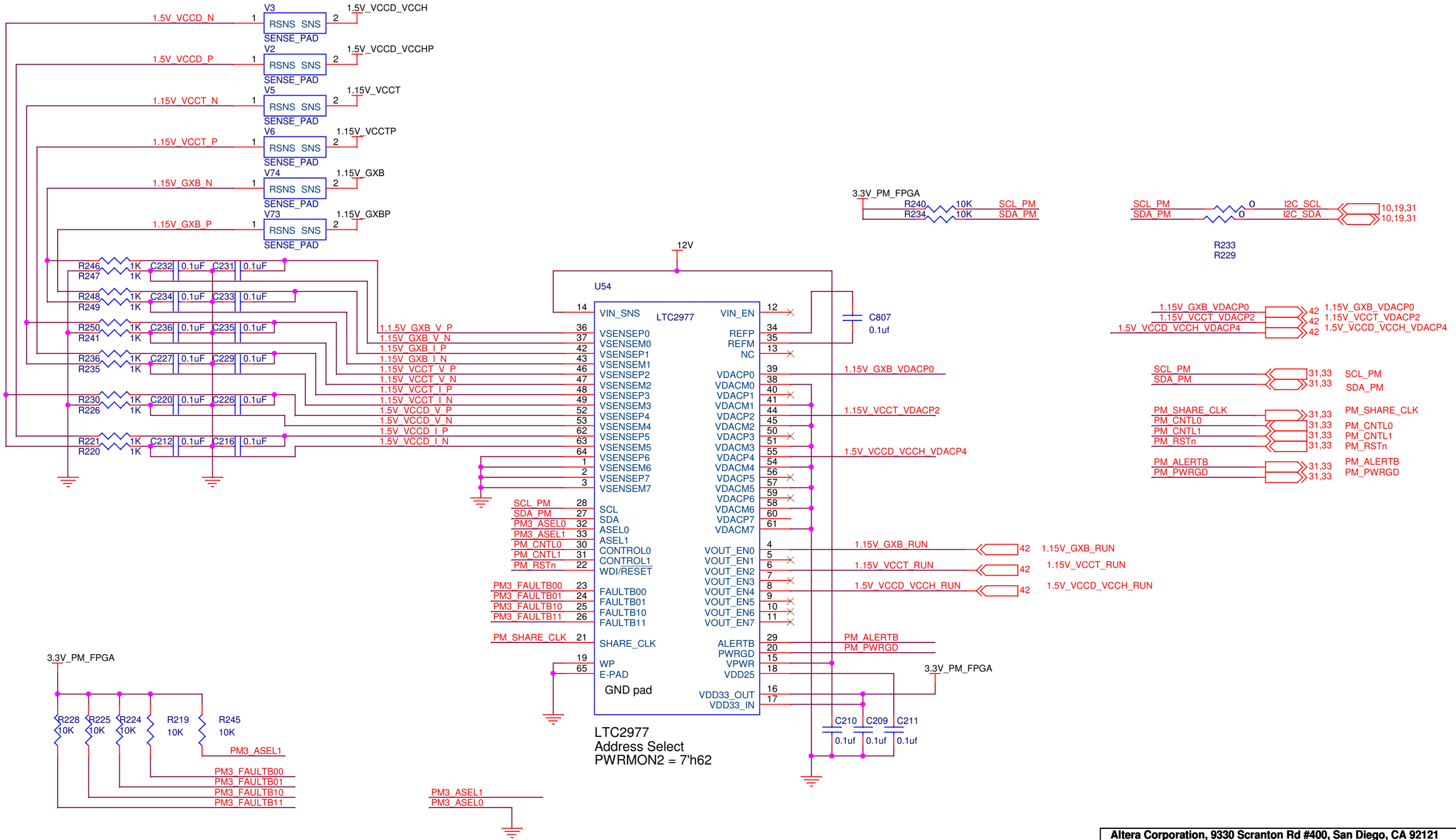
FPGA Power Monitor 2



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HPS Power Monitor

3.3V_HPS_N → V33 RSNS SNS (1 → 2) → 3.3V_HPS; SENSE_PAD
3.3V_HPS_P → V32 RSNS SNS (1 → 2) → 3.3V_REG_HPS; SENSE_PAD
2.5V_HPS_N → V43 RSNS SNS (1 → 2) → 2.5V_HPS; SENSE_PAD
2.5V_HPS_P → V44 RSNS SNS (1 → 2) → 2.5V_REG_HPS; SENSE_PAD
1.5V_HPS_N → V35 RSNS SNS (1 → 2) → 1.5V_HPS; SENSE_PAD
1.5V_HPS_P → V34 RSNS SNS (1 → 2) → 1.5V_REG_HPS; SENSE_PAD
1.1V_HPS_N → V36 RSNS SNS (1 → 2) → 1.1V_HPS; SENSE_PAD
1.1V_HPS_P → V37 RSNS SNS (1 → 2) → 1.1V_REG_HPS; SENSE_PAD

R196 1K	C200 0.1uF	C201 0.1uF	R195 1K		
R194 1K	C192 0.1uF	C197 0.1uF	R191 1K		
R190 1K	C185 0.1uF	C191 0.1uF	R186 1K		
R177 1K	C181 0.1uF	C182 0.1uF	R176 1K		
R175 1K	C179 0.1uF	C180 0.1uF	R174 1K		
R173 1K	C177 0.1uF	C178 0.1uF	R172 1K		
R171 1K	C175 0.1uF	C176 0.1uF	R170 1K		
R185 1K	C190 0.1uF	C184 0.1uF	R189 1K		

these GND connections to each VSENSEMx pin needs to be placed close to a GND pin of the BGA!

12V

U50 LTC2977

14	VIN_SNS	VIN_EN	12
1.1V_HPS_V_P 36	VSENSEP0	REFP	34
1.1V_HPS_V_N 37	VSENSEM0	REFM	35
1.1V_HPS_I_P 42	VSENSEP1	NC	13
1.1V_HPS_I_N 43	VSENSEM1		
1.5V_HPS_V_P 46	VSENSEP2	VDACP0	39 → 1.1V_HPS_VDACP0
1.5V_HPS_V_N 47	VSENSEM2	VDACM0	38
1.5V_HPS_I_P 48	VSENSEP3	VDACP1	40
1.5V_HPS_I_N 49	VSENSEM3	VDACM1	41
2.5V_HPS_V_P 52	VSENSEP4	VDACP2	44 → 1.5V_HPS_VDACP2
2.5V_HPS_V_N 53	VSENSEM4	VDACM2	45
2.5V_HPS_I_P 62	VSENSEP5	VDACP3	50
2.5V_HPS_I_N 63	VSENSEM5	VDACM3	51
3.3V_HPS_V_P 64	VSENSEP6	VDACP4	55 → 2.5_HPS_VDACP4
3.3V_HPS_V_N 1	VSENSEM6	VDACM4	54
3.3V_HPS_I_P 2	VSENSEP7	VDACP5	56
3.3V_HPS_I_N 3	VSENSEM7	VDACM5	57
		VDACP6	59 → 3.3_HPS_VDACP6
SCL_PM 28	SCL	VDACM6	58
SDA_PM 27	SDA	VDACP7	60
PM1_ASEL0 32	ASEL0	VDACM7	61
PM1_ASEL1 33	ASEL1		
PM_CNTL0 30	CONTROL0	VOUT_EN0	4 → EN_1.1V_HPS
PM_CNTL1 31	CONTROL1	VOUT_EN1	5
PM_RSTn 22	WDI/RESET	VOUT_EN2	6 → EN_1.5V_HPS
		VOUT_EN3	7
PM1_FAULTB00 23	FAULTB00	VOUT_EN4	8 → EN_2.5V_HPS
PM1_FAULTB01 24	FAULTB01	VOUT_EN5	9
PM1_FAULTB10 25	FAULTB10	VOUT_EN6	10 → EN_3.3V_HPS
PM1_FAULTB11 26	FAULTB11	VOUT_EN7	11
PM_SHARE_CLK 21	SHARE_CLK	ALERTB	29 → PM_ALERTB
		PWRGD	20 → PM_PWRGD
19	WP	VPWR	15
65	E-PAD	VDD25	18 → 3.3V_PM_HPS
GND pad		VDD33_OUT	16
		VDD33_IN	17

C783 0.1uf

C196 0.1uf, C199 0.1uf, C204 0.1uf

LTC2977
Address Select
PWRMON1 = 7'h5C

PM1_ASEL0
PM1_ASEL1

I2C Interface

J36 2x6HDR

1	1 2	2	SDA_PM
3	3 4	4	SCL_PM
5	5 6	6	PM_ALERTB
PM_CNTL1 7	7 8	8	
9	9 10	10	
11	11 12	12	

3.3V_PM_HPS

R211 10K	R212 10K	R206 10K	R203 10K	R204 10K	R205 10K	R207 10K	R208 10K	R209 10K	R210 10K	R213 10K	R214 10K

SDA_PM
SCL_PM
PM_RSTn
PM_PWRGD
PM_SHARE_CLK
PM_ALERTB
PM1_FAULTB00
PM1_FAULTB01
PM1_FAULTB10
PM1_FAULTB11
PM_CNTL0
PM_CNTL1

PM_SHARE_CLK → 31,32 PM_SHARE_CLK
PM_CNTL0 → 31,32 PM_CNTL0
PM_CNTL1 → 31,32 PM_CNTL1
PM_RSTn → 31,32 PM_RSTn
PM_ALERTB → 31,32 PM_ALERTB
PM_PWRGD → 31,32 PM_PWRGD

EN_1.1V_HPS → 41 EN_1.1V_HPS
EN_1.5V_HPS → 39 EN_1.5V_HPS
EN_2.5V_HPS → 38 EN_2.5V_HPS
EN_3.3V_HPS → 40 EN_3.3V_HPS

1.1V_HPS_VDACP0 → 41 1.1V_HPS_VDACP0
1.5V_HPS_VDACP2 → 39 1.5V_HPS_VDACP2
2.5_HPS_VDACP4 → 38 2.5_HPS_VDACP4
3.3_HPS_VDACP6 → 40 3.3_HPS_VDACP6

SCL_PM → R624 0 → I2C_SCL_HPS → 7,20,28 SCL_PM
SDA_PM → R625 0 → I2C_SDA_HPS → 7,20,28 SDA_PM

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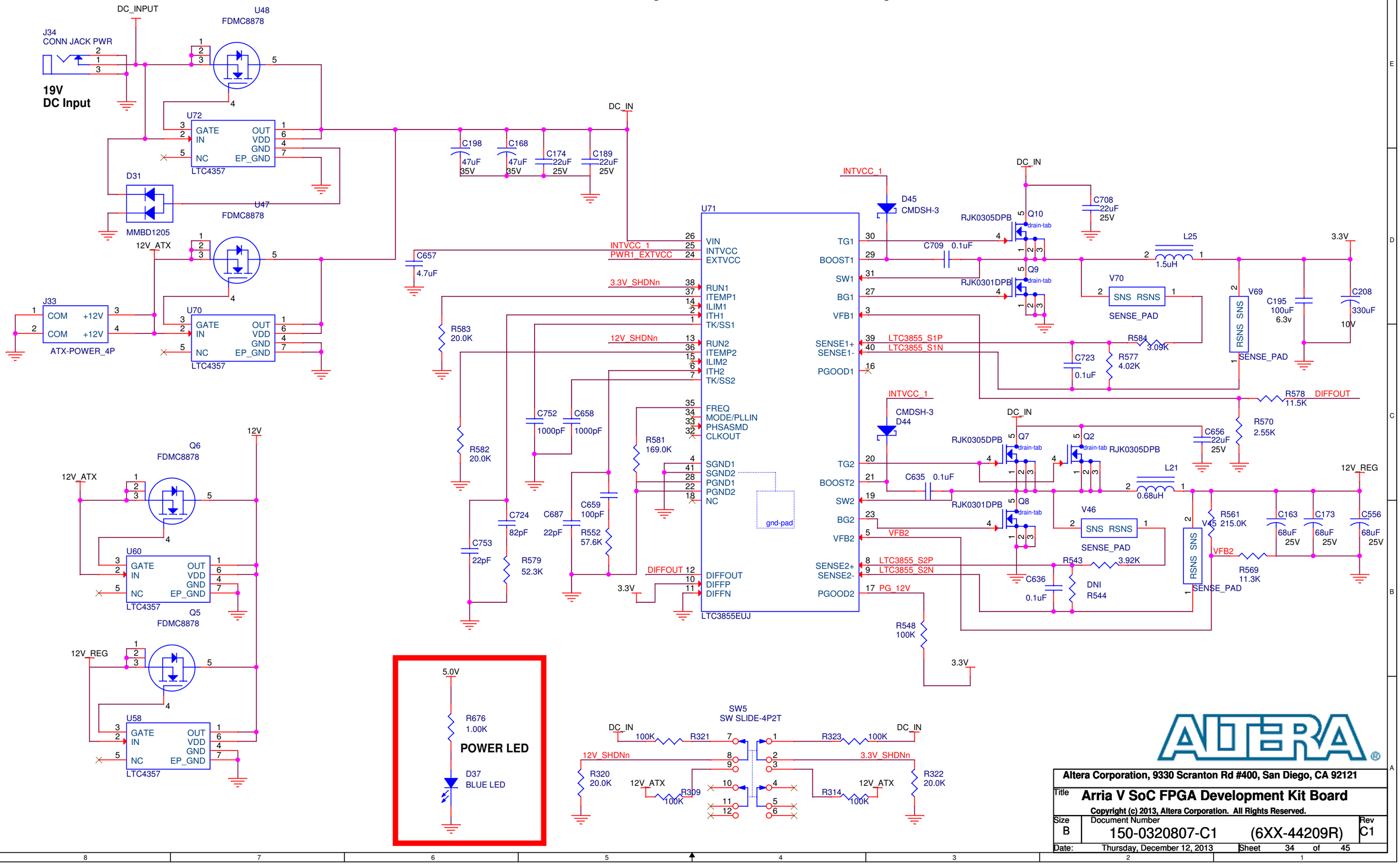
Power 1 - DC Input & 12V, 3.3V Output



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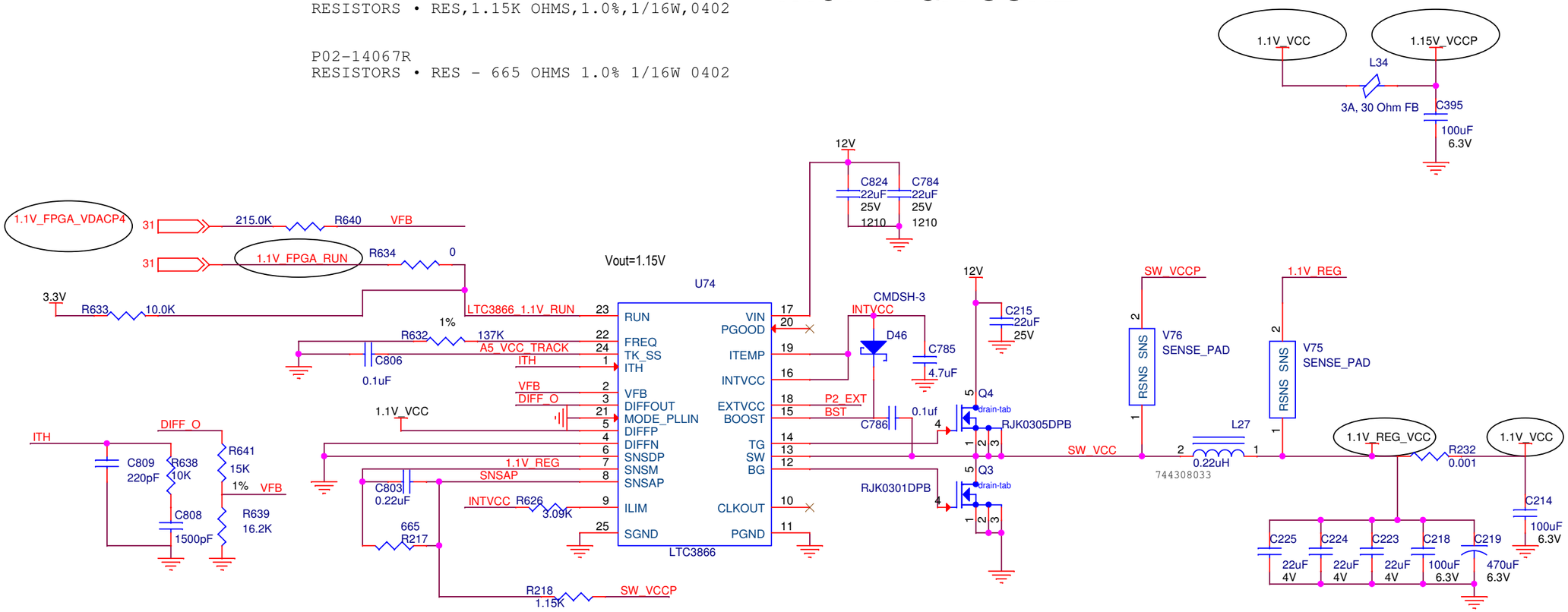
Power 2
1.15V FPGA CORE

P02-11401R
RESISTORS • RES,1.15K OHMS,1.0%,1/16W,0402

P02-14067R
RESISTORS • RES - 665 OHMS 1.0% 1/16W 0402



1.2V 953k P02-16417R
1.5V 549k P02-14713R (0603)
1.8V 383k P02-14133R + P02-15998R
2.5V 226k P02-14130R
3.3V 154k P02-15947R

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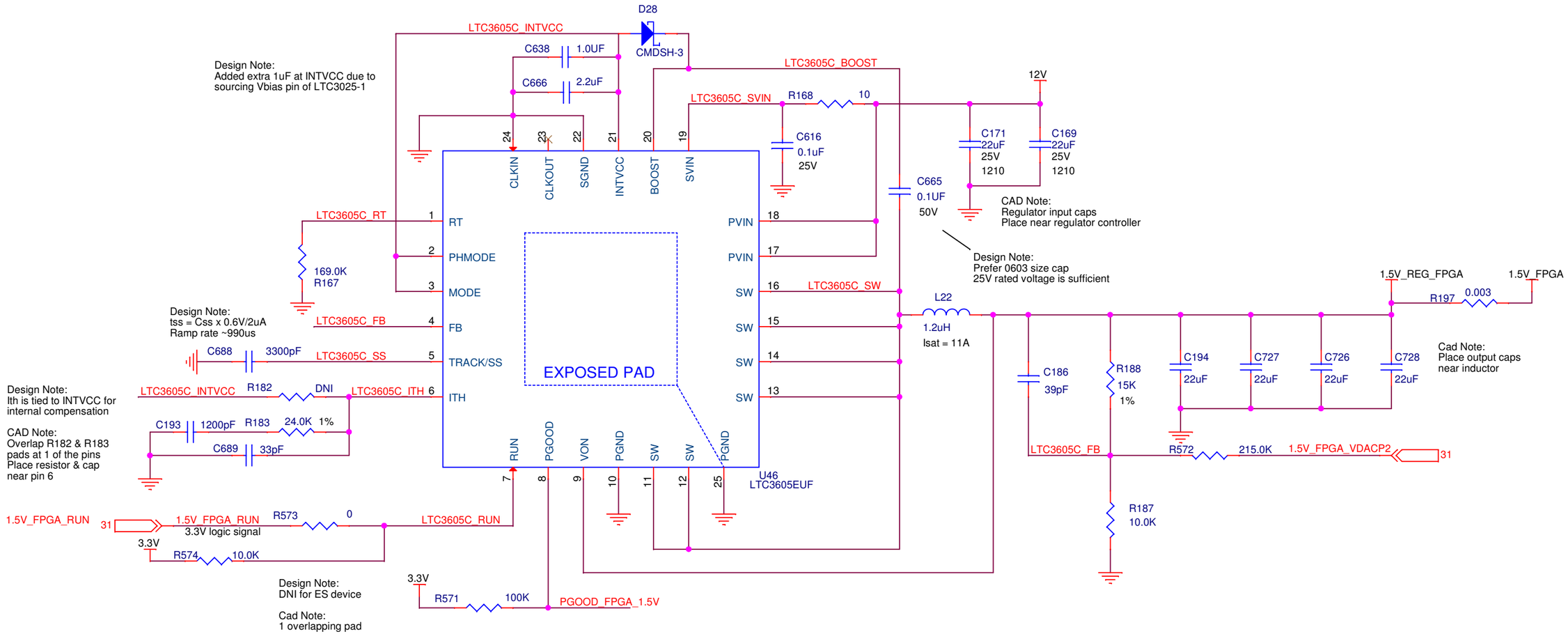
Power 3 - 1.5V FPGA



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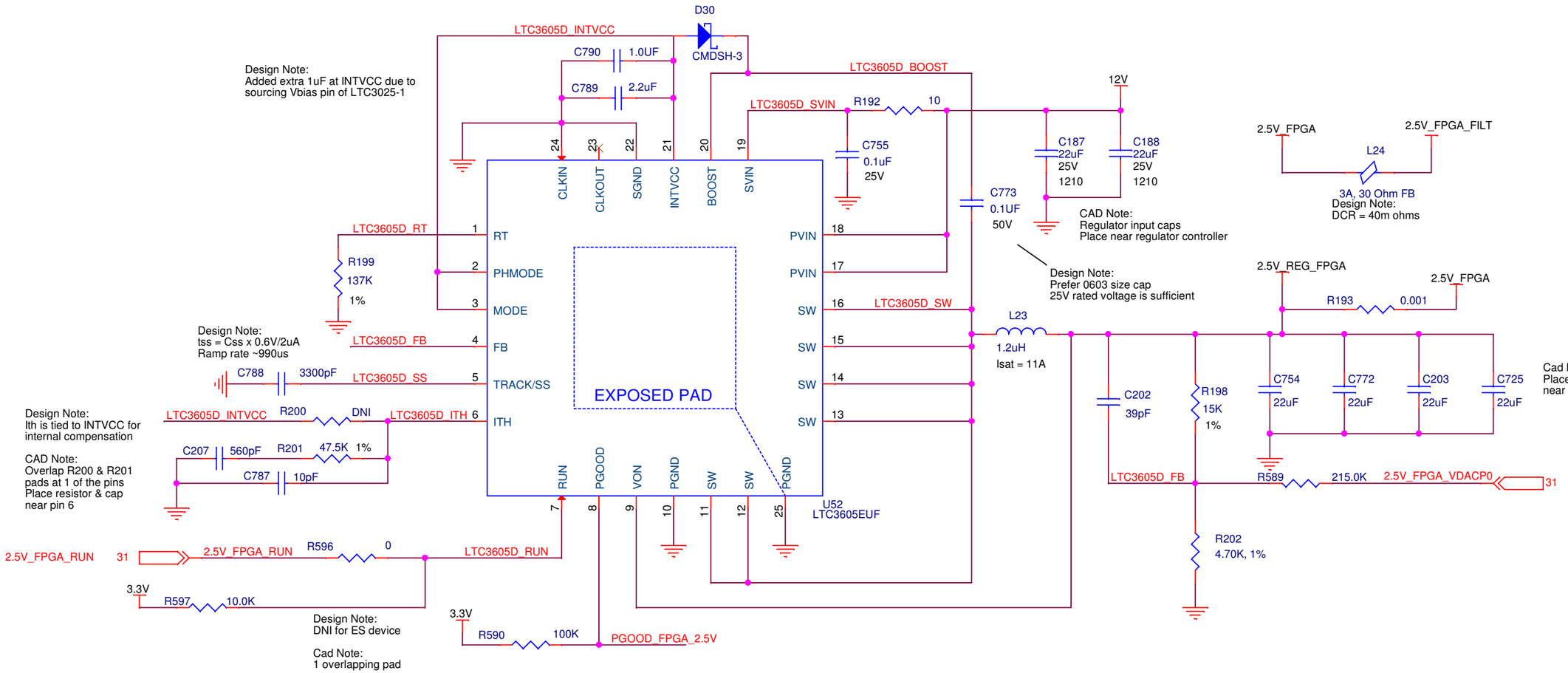
Power 3 - 2.5V FPGA



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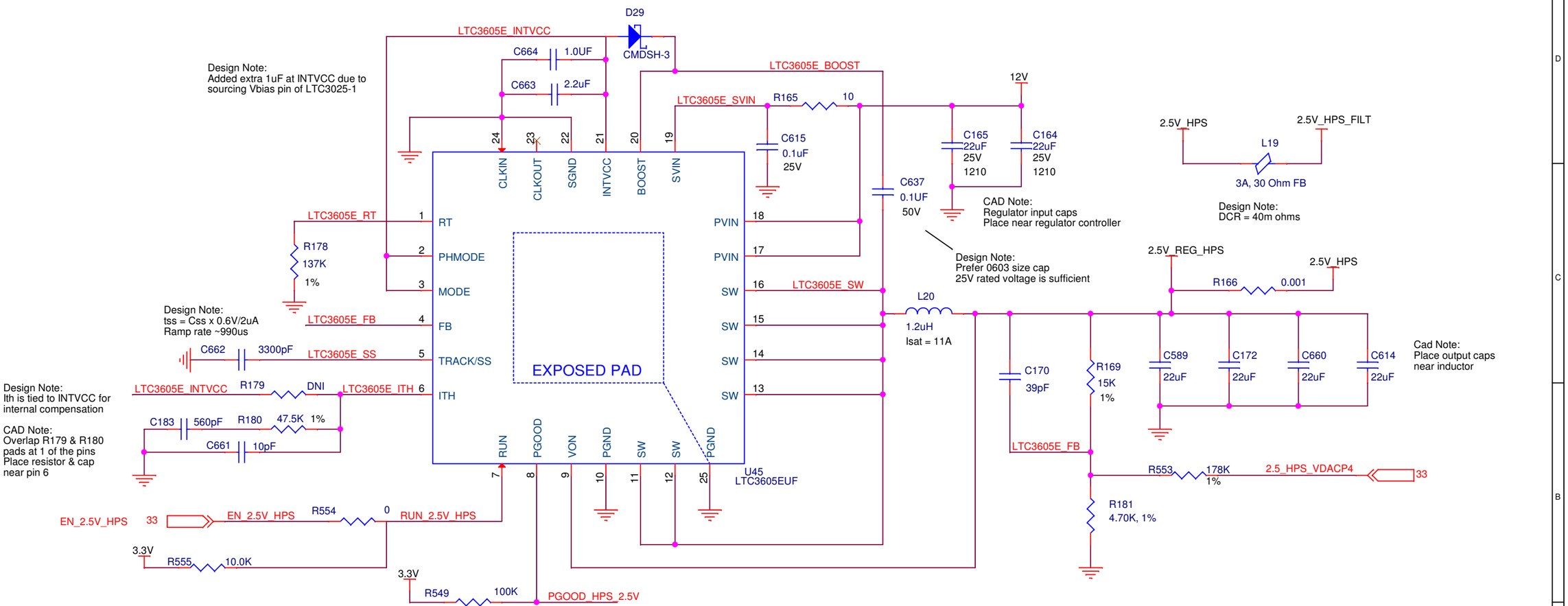
Power 3 - 2.5V HPS

Cad Note:
Place near INTVCC pin



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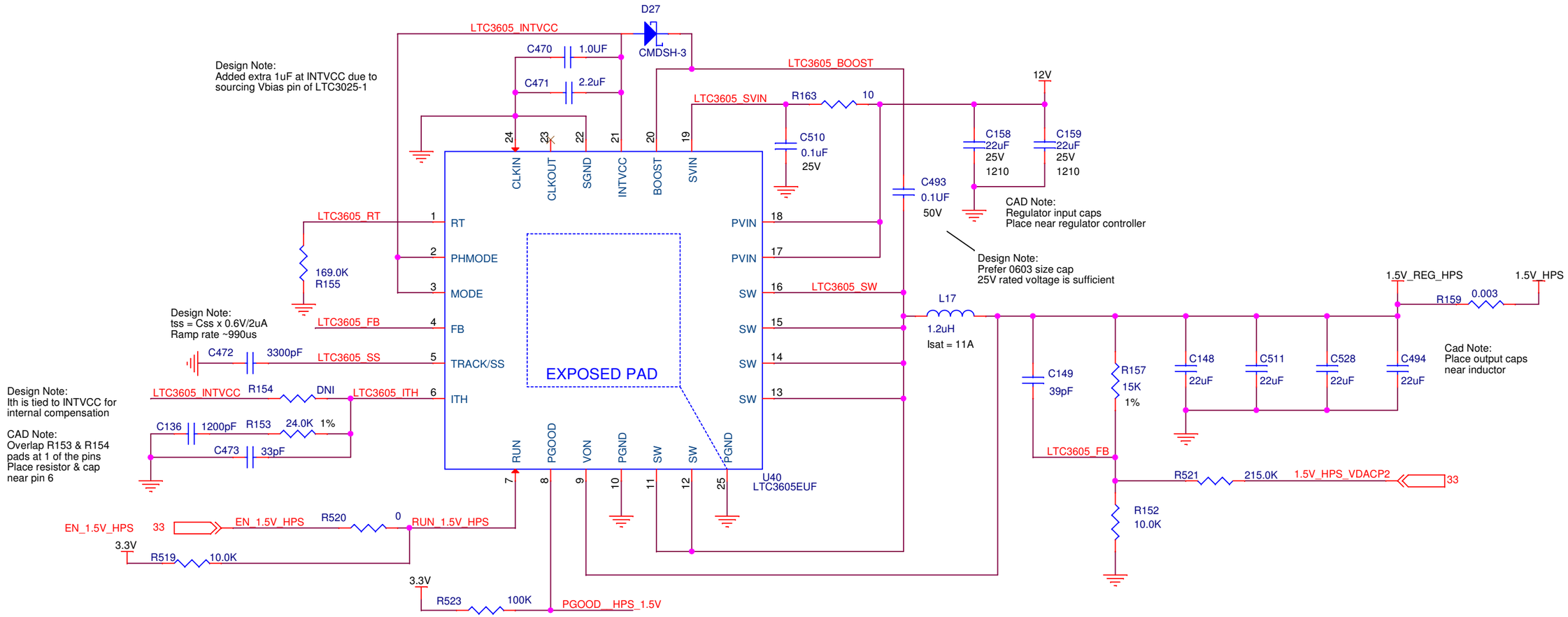
Power 3 - 1.5V & 1.5V FPGA



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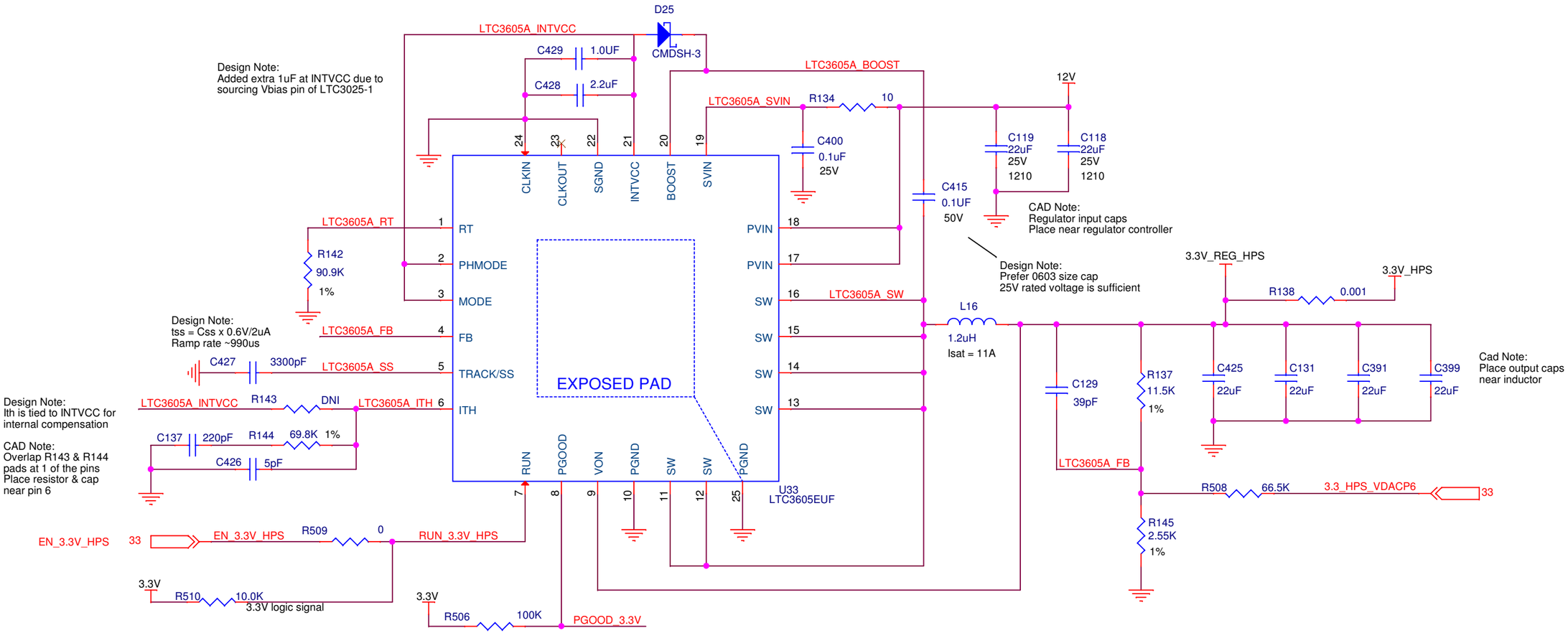
Power 3 - 3.3V HPS



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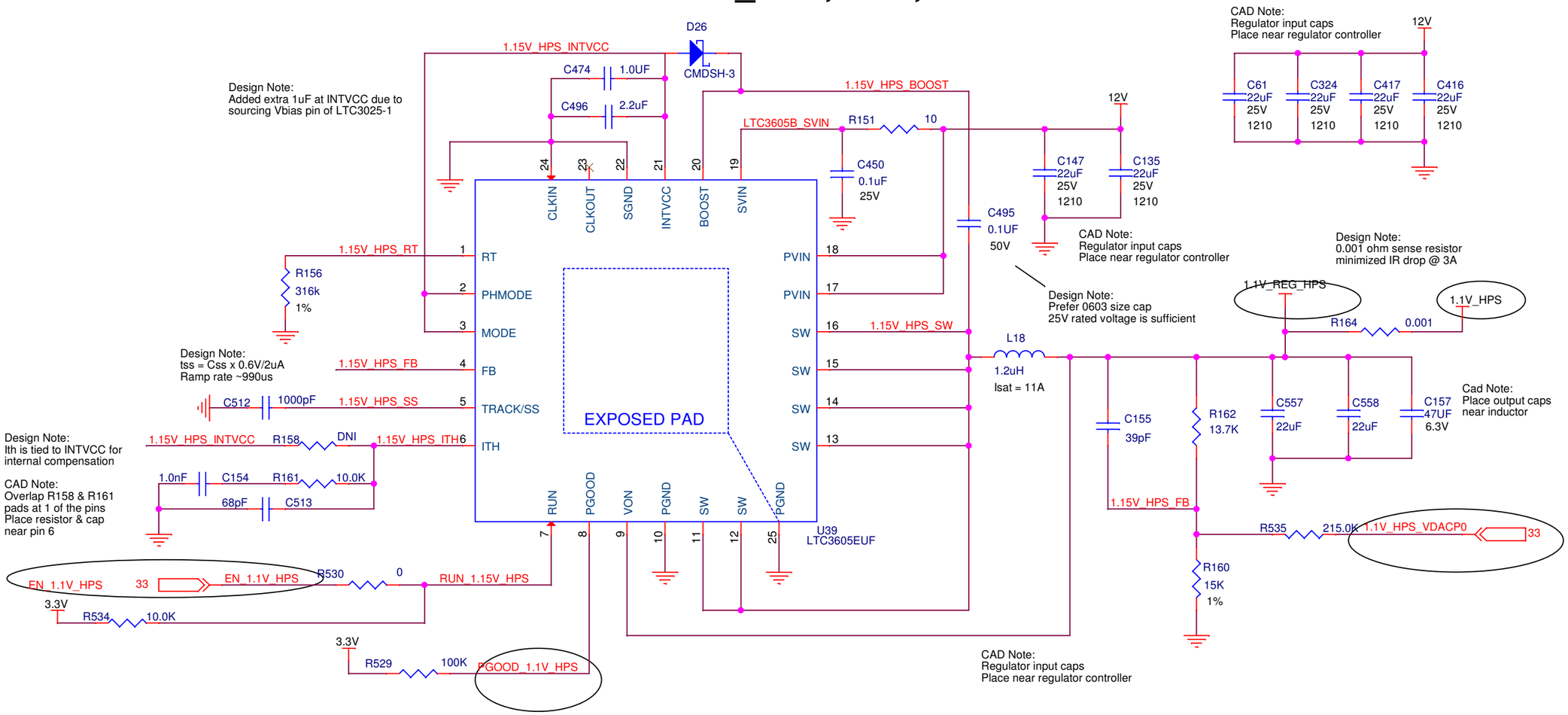
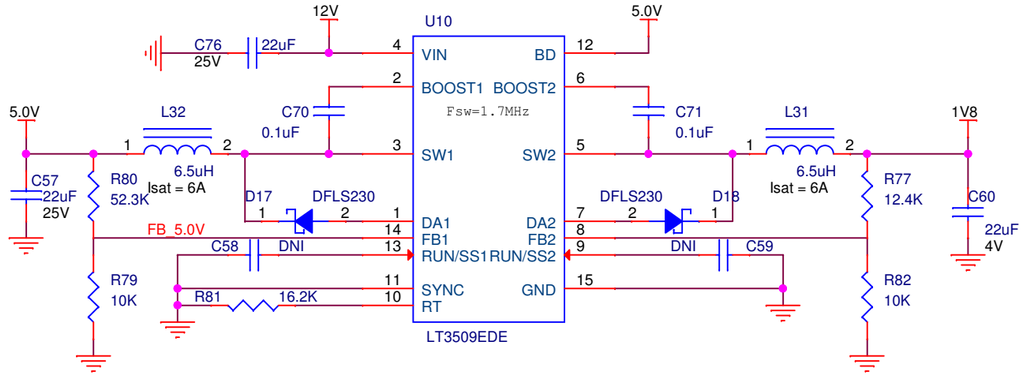
Power - 1.15V_HPS, 5.0V, 1.8V





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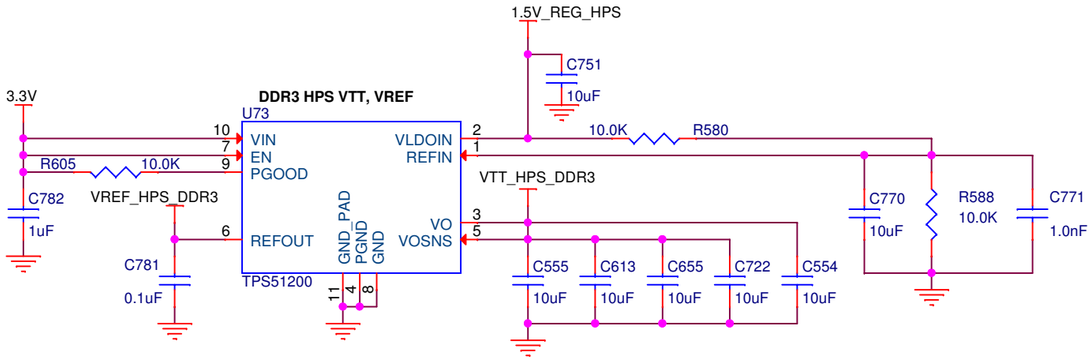
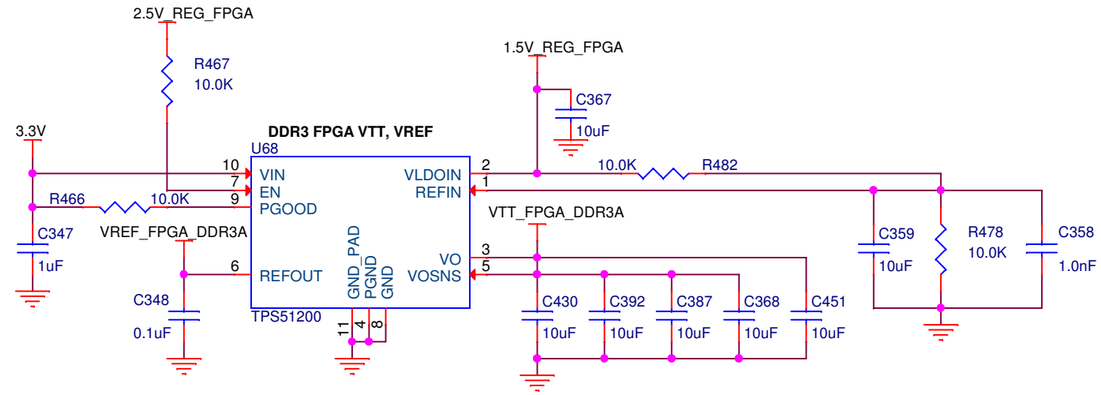
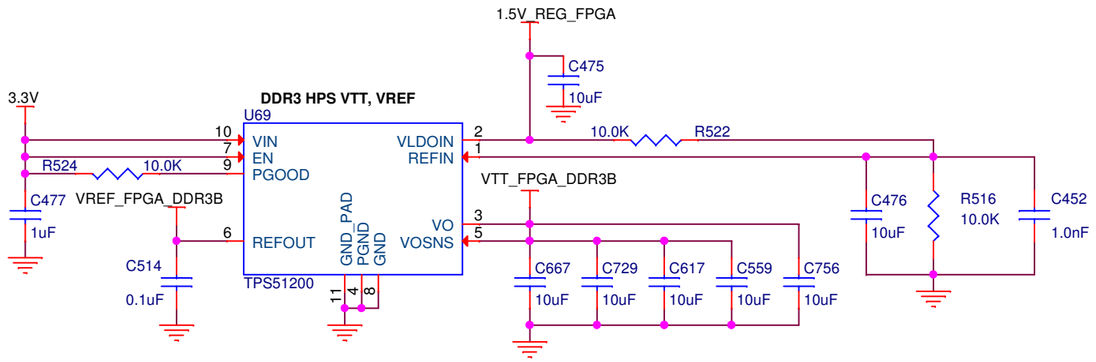
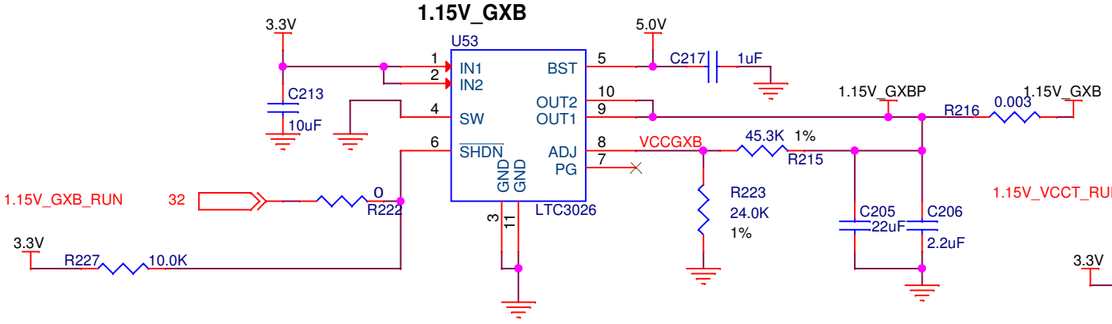
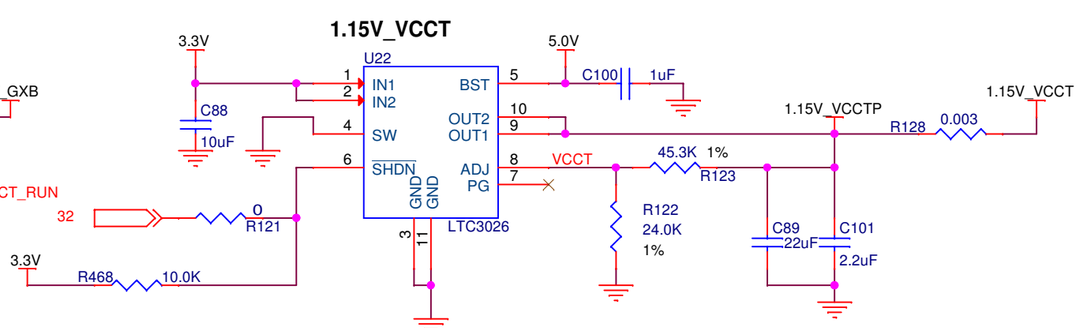
Power 4 - Linear Regulators

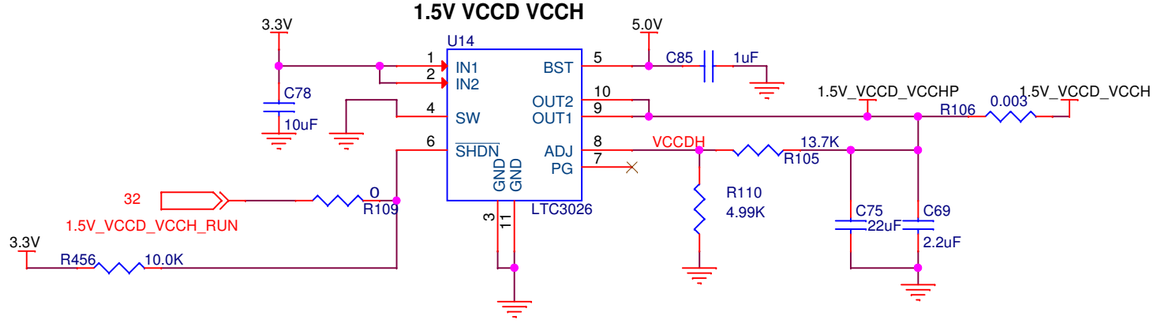


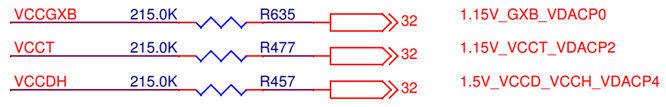












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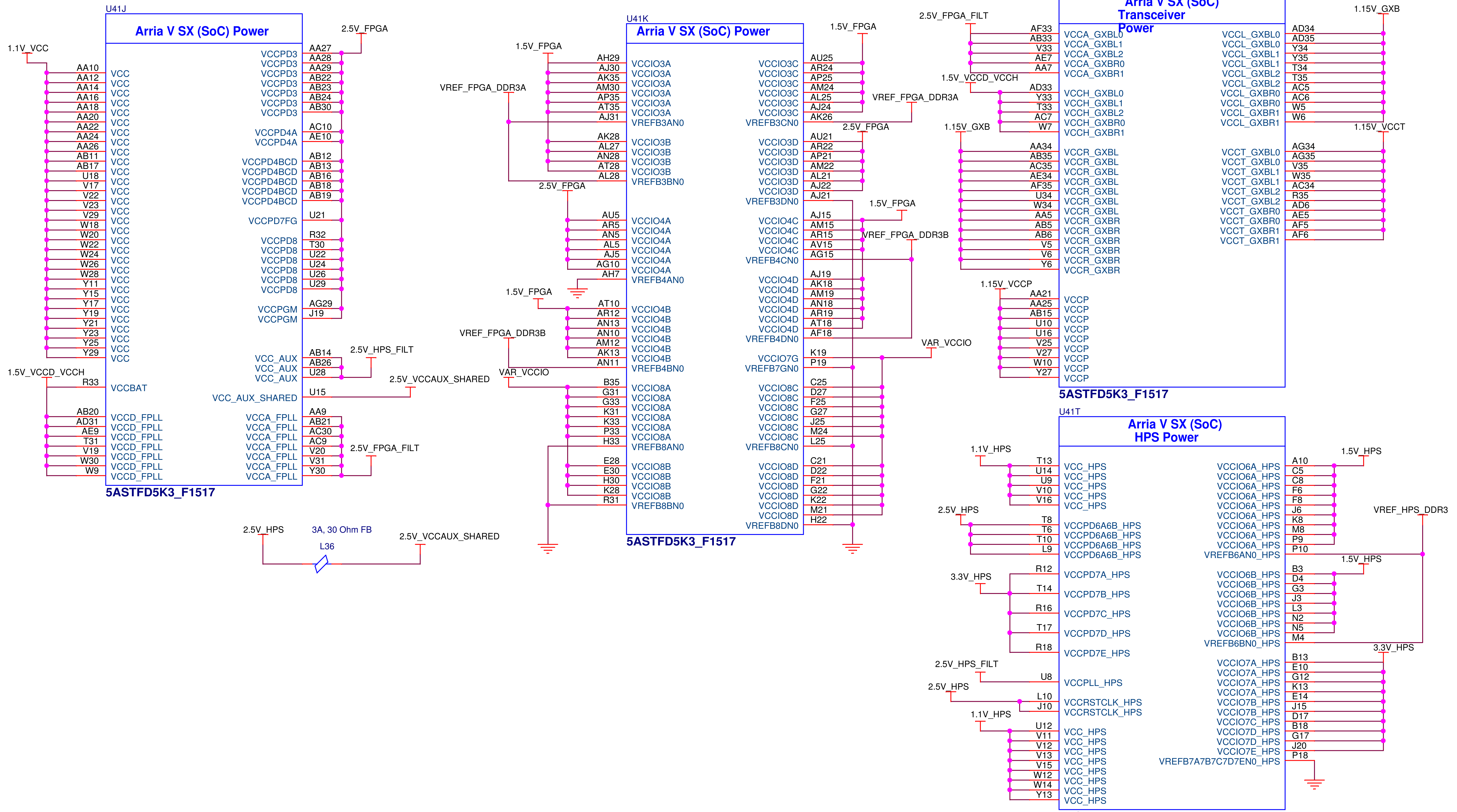
Power 7 - Arria V ST Power



U41J
Arria V SX (SoC) Power
1.1V_VCC
AA10 AA12 AA14 AA16 AA18 AA20 AA22 AA24 AA26 AB11 AB17 U18 V17 V22 V23 V29 W18 W20 W22 W24 W26 W28 Y11 Y15 Y17 Y19 Y21 Y23 Y25 Y29
VCC
1.5V_VCCD_VCCH
R33 VCCBAT
AB20 AD31 AE9 T31 V19 W30 W9
VCCD_FPLL
2.5V_FPGA
AA27 AA28 AA29 AB22 AB23 AB24 AB30 VCCPD3
AC10 AE10 VCCPD4A
AB12 AB13 AB16 AB18 AB19 VCCPD4BCD
U21 VCCPD7FG
R32 T30 U22 U24 U26 U29 VCCPD8
AG29 J19 VCCPGM
2.5V_HPS_FILT
AB14 AB26 U28 VCC_AUX
2.5V_VCCAUX_SHARED
U15 VCC_AUX_SHARED
2.5V_FPGA_FILT
AA9 AB21 AC30 AC9 V20 V31 Y30 VCCA_FPLL
5ASTFD5K3_F1517
2.5V_HPS
3A, 30 Ohm FB
L36
2.5V_VCCAUX_SHARED
U41K
Arria V SX (SoC) Power
1.5V_FPGA
AH29 AJ30 AK35 AM30 AP35 AT35 VCCIO3A
VREF_FPGA_DDR3A
AJ31 VREFB3AN0
AK28 AL27 AN28 AT28 VCCIO3B
AL28 VREFB3BN0
2.5V_FPGA
AU5 AR5 AN5 AL5 AJ5 AG10 VCCIO4A
AH7 VREFB4AN0
1.5V_FPGA
AT10 AR12 AN13 AN10 AM12 AK13 VCCIO4B
VREF_FPGA_DDR3B
AN11 VREFB4BN0
VAR_VCCIO
B35 G31 G33 K31 K33 P33 VCCIO8A
H33 VREFB8AN0
E28 E30 H30 K28 VCCIO8B
R31 VREFB8BN0
1.5V_FPGA
AU25 AR24 AP25 AM24 AL25 AJ24 VCCIO3C
VREF_FPGA_DDR3A
AK26 VREFB3CN0
2.5V_FPGA
AU21 AR22 AP21 AM22 AL21 AJ22 VCCIO3D
AJ21 VREFB3DN0
1.5V_FPGA
AJ15 AM15 AR15 AV15 VCCIO4C
VREF_FPGA_DDR3B
AG15 VREFB4CN0
AJ19 AK18 AM19 AN18 AR19 AT18 VCCIO4D
AF18 VREFB4DN0
VAR_VCCIO
K19 VCCIO7G
P19 VREFB7GN0
C25 D27 F25 G27 J25 M24 VCCIO8C
L25 VREFB8CN0
C21 D22 F21 G22 K22 M21 VCCIO8D
H22 VREFB8DN0
5ASTFD5K3_F1517
U41L
Arria V SX (SoC) Transceiver Power
2.5V_FPGA_FILT
AF33 VCCA_GXBL0
AB33 VCCA_GXBL1
V33 VCCA_GXBL2
AE7 VCCA_GXBR0
AA7 VCCA_GXBR1
1.5V_VCCD_VCCH
AD33 VCCH_GXBL0
Y33 VCCH_GXBL1
T33 VCCH_GXBL2
AC7 VCCH_GXBR0
W7 VCCH_GXBR1
1.15V_GXB
AA34 AB35 AC35 AE34 AF35 U34 W34 VCCR_GXBL
AA5 AB5 AB6 V5 V6 Y6 VCCR_GXBR
1.15V_VCCP
AA21 AA25 AB15 U10 U16 V25 V27 W10 Y27 VCCP
1.15V_GXB
AD34 AD35 VCCL_GXBL0
Y34 Y35 VCCL_GXBL1
T34 T35 VCCL_GXBL2
AC5 AC6 VCCL_GXBR0
W5 W6 VCCL_GXBR1
1.15V_VCCT
AG34 AG35 VCCT_GXBL0
V35 W35 VCCT_GXBL1
AC34 R35 VCCT_GXBL2
AD6 AE5 VCCT_GXBR0
AF5 AF6 VCCT_GXBR1
5ASTFD5K3_F1517
U41T
Arria V SX (SoC) HPS Power
1.1V_HPS
T13 U14 U9 V10 V16 VCC_HPS
2.5V_HPS
T8 T6 T10 L9 VCCPD6A6B_HPS
3.3V_HPS
R12 VCCPD7A_HPS
T14 VCCPD7B_HPS
R16 VCCPD7C_HPS
T17 VCCPD7D_HPS
R18 VCCPD7E_HPS
2.5V_HPS_FILT
U8 VCCPLL_HPS
2.5V_HPS
L10 J10 VCCRSTCLK_HPS
1.1V_HPS
U12 V11 V12 V13 V15 W12 W14 Y13 VCC_HPS
1.5V_HPS
A10 C5 C8 F6 F8 J6 K8 M8 P9 VCCIO6A_HPS
VREF_HPS_DDR3
P10 VREFB6AN0_HPS
1.5V_HPS
B3 D4 G3 J3 L3 N2 N5 VCCIO6B_HPS
M4 VREFB6BN0_HPS
3.3V_HPS
B13 E10 G12 K13 VCCIO7A_HPS
E14 J15 VCCIO7B_HPS
D17 VCCIO7C_HPS
B18 G17 VCCIO7D_HPS
J20 VCCIO7E_HPS
P18 VREFB7A7B7C7D7EN0_HPS
5ASTFD5K3_F1517

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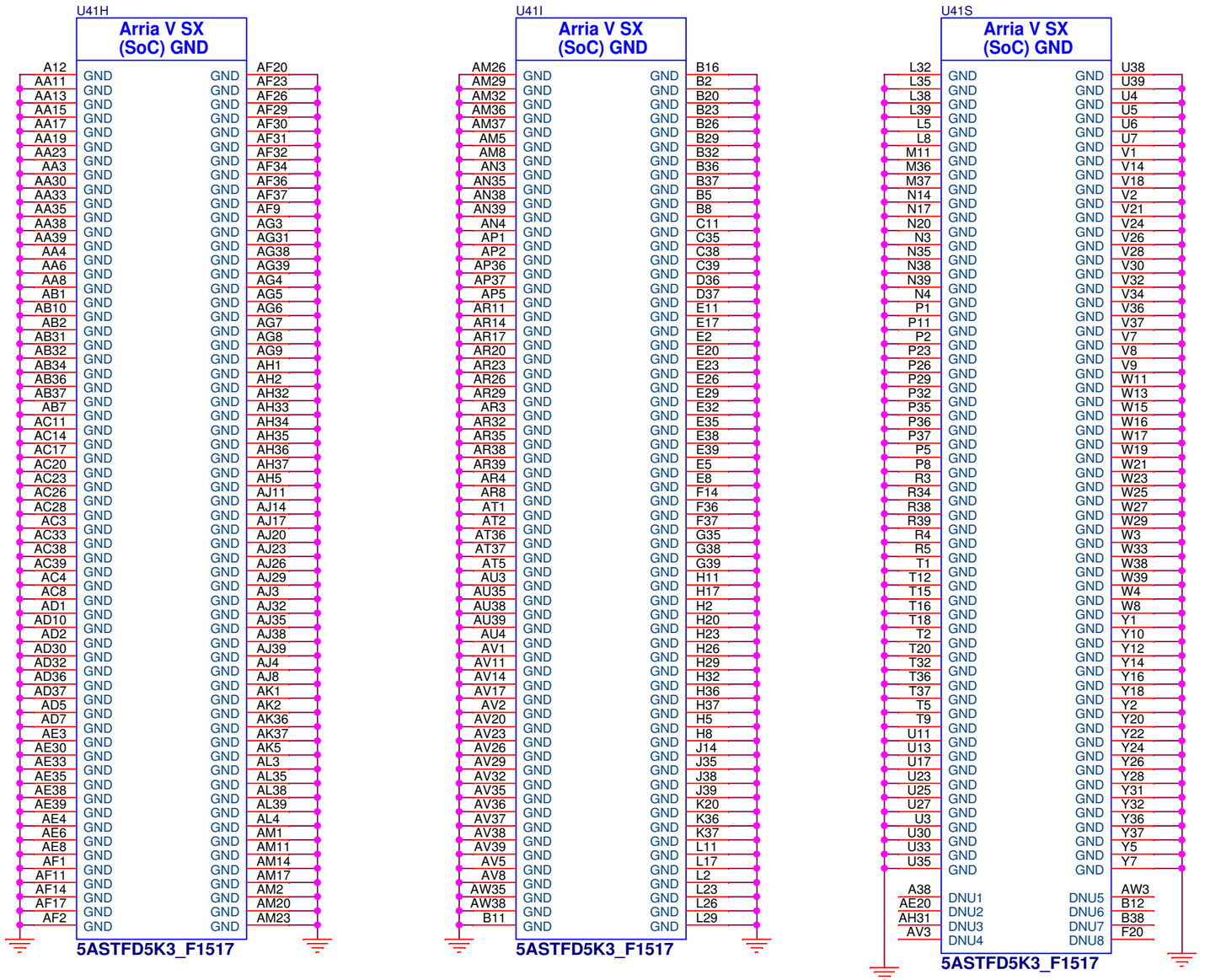
Power 8 - Arria V ST Ground



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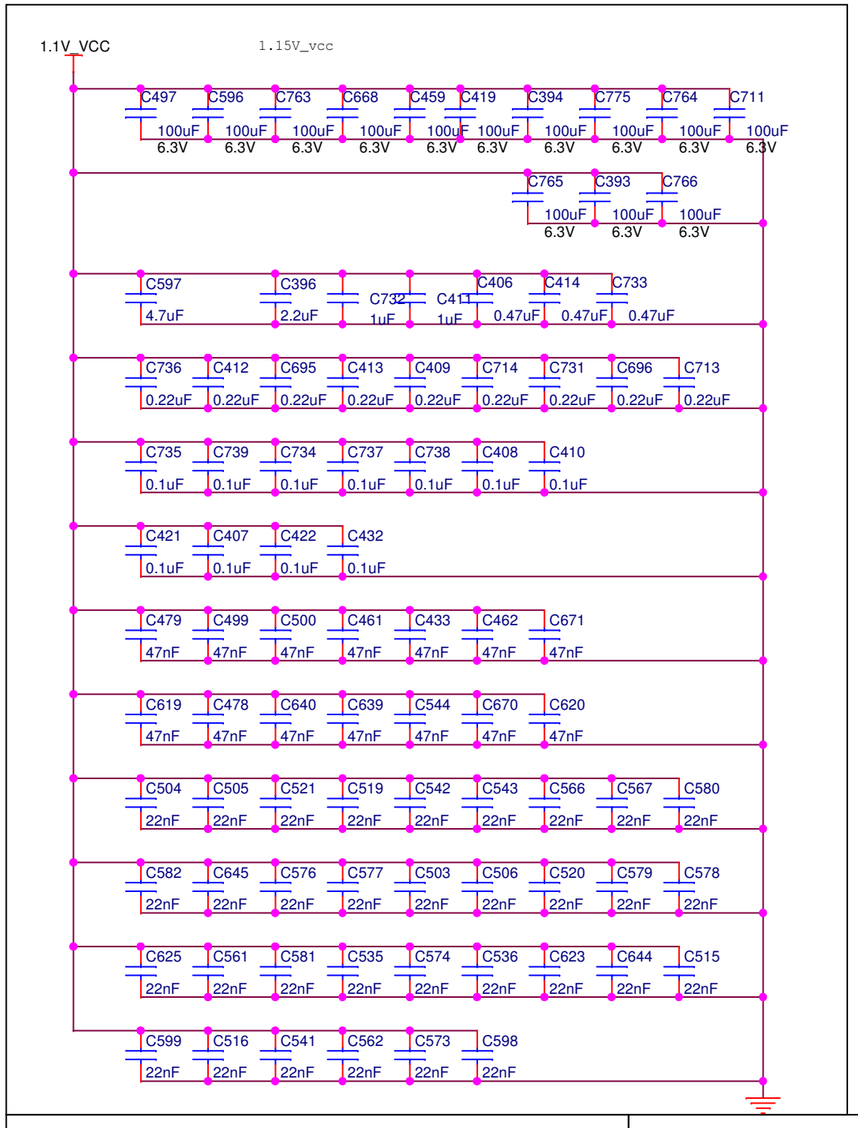
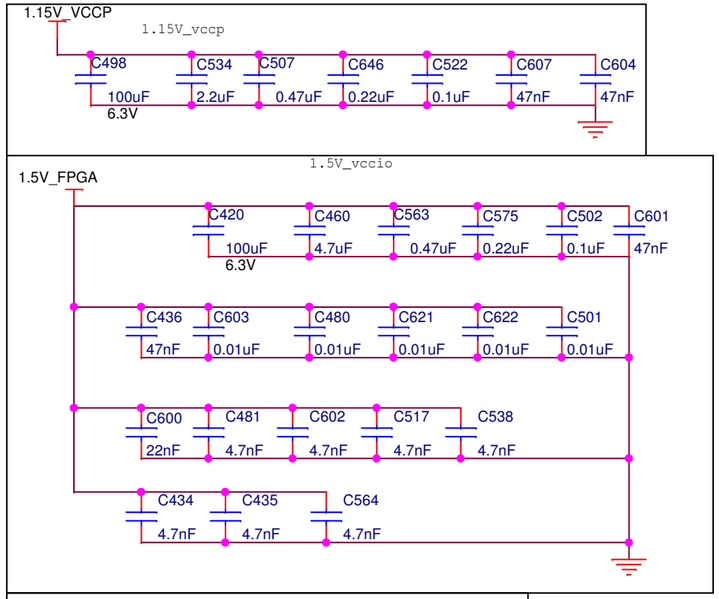
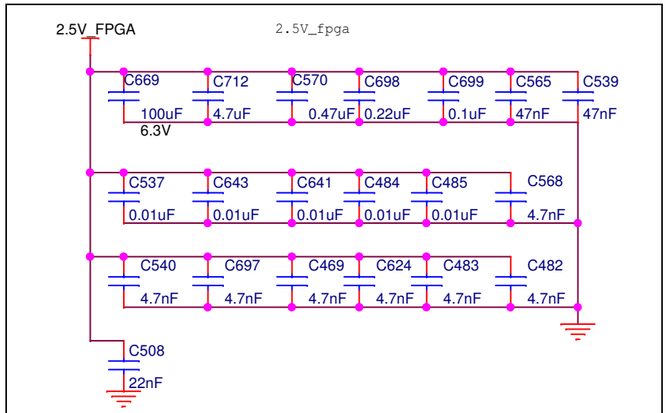
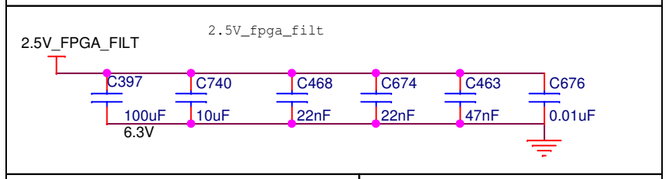
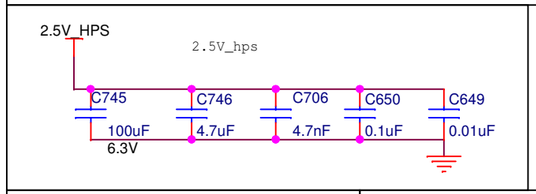
Decoupling

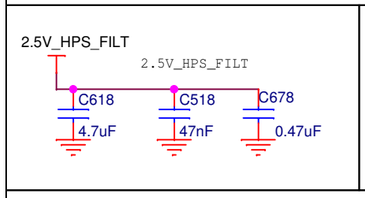


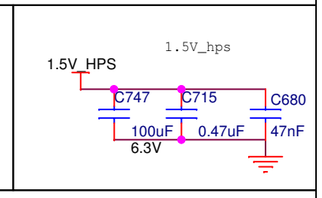


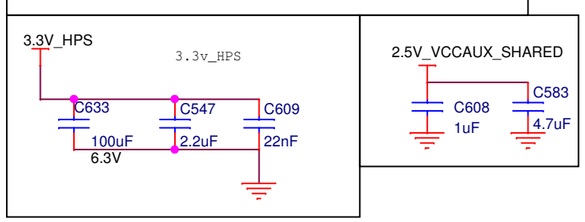


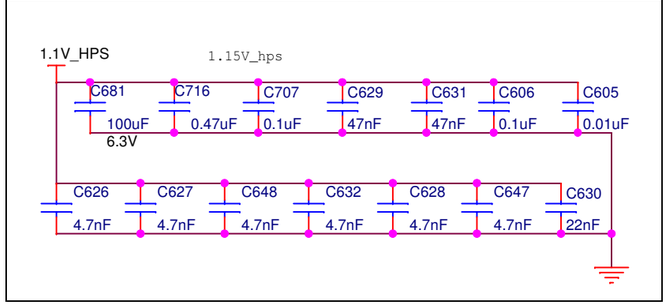


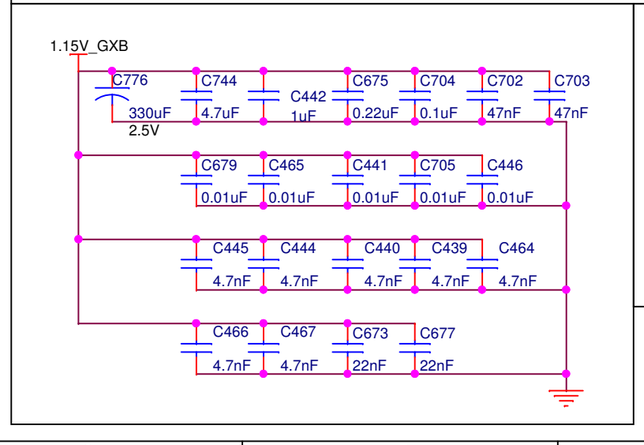


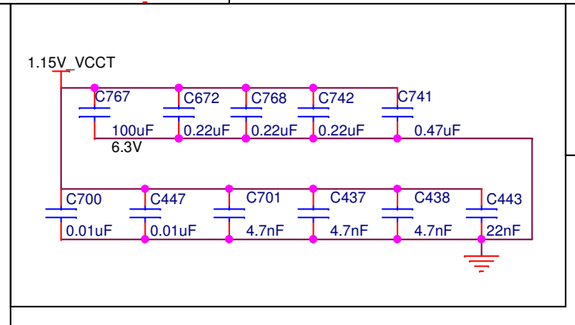


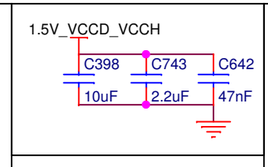


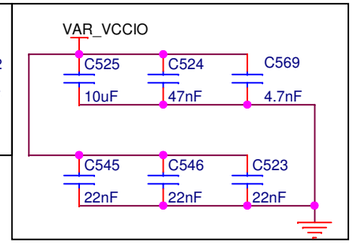


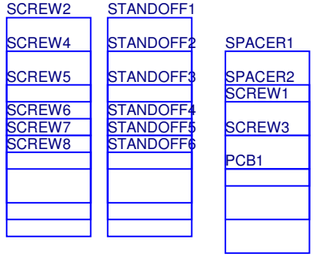












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