

Microwave Synthesizer Offers Multioctave Frequency Coverage and Excellent Phase Noise Performance

Marty Richardson, Senior Applications Engineer

Introduction

System frequency and modulation rate requirements continue to escalate with the need for more bandwidth and higher data rates. Low power consumption has become critical as applications once relegated to military and defense enter the commercial sector. These demands come with the caveat that there be no sacrifice of electrical performance or functionality. In order to meet these requirements, including an improved signal-to-noise ratio (SNR), bit error rate (BER), and the high quality of service (QoS) that users are accustomed to, the phase noise of the local oscillator (LO) must improve as well.

The newly released **ADF5610** is an integrated phase-locked loop (PLL) and voltage controlled oscillator (VCO) that highlights Analog Devices' efforts to provide a solution that addresses each of these concerns and more.

Frequency Coverage

A total of eight octaves are covered by the ADF5610 with the VCO fundamental frequency ranging from 3.65 GHz to 7.3 GHz, which is fed back to the PLL to minimize phase noise. A single-ended output (RFOUT) doubles the fundamental frequency range to provide 7.3 GHz to 14.6 GHz while the differential output simultaneously allows the full operating range of 57 MHz to 14.6 GHz through the use of divide by 1/2/4/8/16/32/64 and 128 settings.

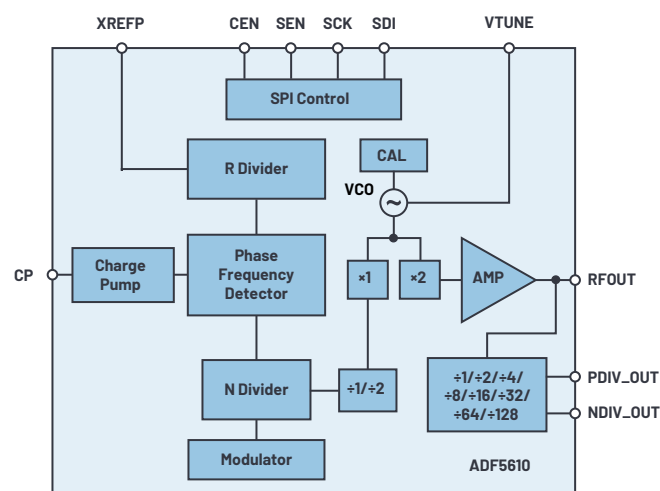


Figure 1. Block diagram of the ADF5610.

The architecture of the ADF5610 VCO allows wideband synthesizer performance while retaining industry-leading phase noise performance with a nominal open-loop phase noise at 10 GHz of -114 dBc/Hz at a 100 kHz offset. An internal state machine allows frequency settling times of under 40 μ s using just a passive loop filter; no need for additional circuitry or lookup tables (LUTs) unless faster settling times are required.

Leading PLL Performance for Converter Clocks

While the phased-locked loop (PLL) inside of the ADF5610 boasts a modest figure of merit (FOM) of -229 dBc/Hz (-232 dBc/Hz high current mode), when combined with exceptional $1/f$ noise (-129 dBc/Hz) and state-of-the-art VCO phase noise, rms jitter numbers less than 38 fs (1 kHz to 100 MHz integration limit) are possible. This makes the ADF5610 suitable for use in the most demanding converter clock applications. Loop filter resistor values should be kept at a minimum to reduce their thermal noise and a high frequency (100 MHz). An ultralow noise reference source is essential in order to achieve this level of performance.



Figure 2. RMS jitter: 8.0 GHz.



Figure 3. RMS jitter: 14.4 GHz.

Communications and Instrumentation LOs

In addition to its broad frequency coverage, industry-leading phase noise, and exceptionally fast lock times, the ADF5610 has additional features that make it attractive for wireless and instrumentation applications where it will most often serve as the local oscillator.

24 bits of fractional resolution are modest, but when paired with the ADF5610's exact frequency mode functionality, frequency generation with 0 Hz error is possible. Using the ADF5610 as the local oscillator allows the active mixer to be driven directly from the RFOUT port due to the nominal 5 dBm of output power, eliminating

the need for additional amplification and saving valuable board space. The output power on the differential divider (PDIVOUT/NDIVOUT) is nominally 2 dBm when used single ended, but it can be combined through a low loss balun or hybrid coupler for narrow-band applications to achieve an additional dB or two of output power.

Low power dissipation is essential today and the ADF5610 does its part by sipping less than 700 mW (low current mode with the output divider disabled) to just over a watt under worst-case conditions (high performance mode with the output divider set to divide-by-128). Even in low current mode, the ADF5610's phase noise performance leads in its class, increasing by just 2 dBc/Hz.

The ADF5610 has good spurious performance, with PFD spurious as low as -105 dBc, and in-band unfiltered integer boundary spurs nominally at -45 dBc.

Small Size

The ADF5610 PLL/VCO is available in a 7 mm × 7 mm, 48-lead land grid array (LGA) package. Minimal additional decoupling is required, meaning that exceptional performance exists in a small footprint solution. To achieve the best performance, the use of high quality low dropout (LDO) regulators such as the [ADM7150](#), [LT3045/LT3042](#), or [HMC1060](#) are recommended. The VCO requires a 5 V supply, while the remaining circuitry is powered from a 3.3 V rail. The ADF5610 can be simulated in ADIsimPLL™ to assist the user in designing the appropriate external component circuitry required to implement a complete PLL synthesizer.

Conclusion

Industry-leading frequency coverage and phase noise performance coupled with high output power and low power dissipation in a small form factor combine on the ADF5610 to address the stringent demands of new communication and instrumentation systems.

About the Author

Marty Richardson joined Analog Devices in 2014 as a senior applications engineer for the Microwave Frequency Generation Group. His RF/microwave career spans more than 35 years and includes previous roles in design and reliability. Currently he is focused on phase-locked loop (PLL), voltage controlled oscillator (VCO), and frequency multiplier products. He is an IEEE senior member and when not working or spending time with family, he enjoys home restoration projects, hunting, fishing, and mountain biking. He can be reached at marty.richardson@analog.com.

Engage with the ADI technology experts in our online support community. Ask your tough design questions, browse FAQs, or join a conversation.

ADI EngineerZone™
SUPPORT COMMUNITY

Visit ez.analog.com