LINEAR TECHNOLOGY

DESIGN NOTES

# I²C Fan Control Ensures Continuous System Cooling

Design Note 270

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## Introduction

Linear Technology's LTC®1840 is a dual fan speed controller for high availability servers and other rack-based network and telecom equipment. The LTC1840 offers advanced control and monitoring capabilities, accessed via an I²C and SMBus compatible 2-wire serial interface. In addition to two fan speed control channels, the LTC1840 also includes a fan tachometer and fault monitoring, nine slave addresses and four general-purpose programmable I/O pins in a 16-pin SSOP package. Adjusting fan speed to match instantaneous cooling requirements increases energy efficiency and reduces noise. By operating at reduced speeds, fan bearings are subjected to less wear, increasing fan life and reliability.

Figure 1 shows a block diagram for a fan speed control system using the LTC1840. The LTC1840 contains two current DACs used to gain full control over fan speed. The scaled currents individually adjust the fan-driving output voltage of a switching regulator. $V_O$ increases as the current $I_{DAC}$ is increased under command of the serial interface. The number of fans controlled by one DAC is limited only by the switching regulator output power.

The TACH of the LTC1840 monitors the speed of fans that include a tachometer output. Internal logic accumulates a maximum of 255 counts between the fan tachometer's rising edges. The rate of the counter is determined by a divisor (2, 4, 8 or 16 chosen via the serial interface) from the 50kHz internal oscillator. Fans slowing down due to worn bearings or halted from a jam will cause an overflow in the internal counter and a corresponding bit is set low in the fault register. The system controller can then take action, shutting down the faulty fan and summoning maintenance.

The chip contains four general purpose input/output (GPIO) pins that are configured independently. As open-drain outputs, they can be set high, low or to pulse at a 1.5Hz rate. The outputs are rated at 10mA sink current for compatibility with LEDs. Configured as inputs, the GPIO pins can monitor thermal switches, push buttons and switching regulator and Hot Swap™ controller fault or power good outputs. State changes are detected and flagged in a fault register.

Internal data registers are read and programmed via I²C by specifying device address and register address. DACA and DACB registers control the 100µA current outputs on a 255-step scale. The STATUS register allows the user to enable the TACHA and TACHB fault data and set the divisor for the internal counter frequency. The internal count, which is inversely proportional to tachometer speed, is stored in the TACHA and TACHB registers. Unmasked faults set the $\overline{FAULT}$ pin high as an instant hardware alert. The GPIO setup and GPIO data registers configure the GPIO pins, assign output and fault status and read input state.



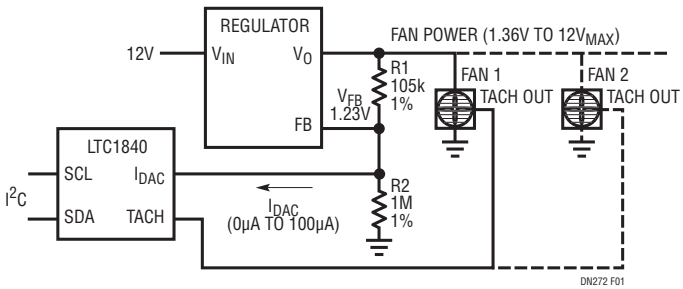


**Figure 1. LTC1840 Fan Speed Control Block Diagram**

## Continuous System Cooling and Tachometer Monitoring

The circuit in Figure 2 demonstrates the capabilities of the LTC1840. Power for up to four 12V, 420mA fans is supplied by each LTC1771 high efficiency step-down regulator. As shown, the upper LTC1771 drives a single fan backed up by an idle, redundant fan. In the event the primary fan fails, GPIO3 turns off the LTC1771 and simultaneously activates the backup fan which runs at full speed. These fans operate one at a time, so the tachometer outputs are wire ORed and only one input (TACHA) is required to monitor their speed.

Two fans are driven in parallel by the lower LTC1771 and alternately monitored by TACHB. These fans operate simultaneously, so their tachometer outputs are muxed by a quad NAND gate. GPIO2 operates in pulsing mode and serves to clock the mux.

## Additional Features

For applications requiring multiple fan controllers, the LTC1840's three-state (high, low, no connect) address programming inputs support nine user-selectable slave addresses. The $\overline{\text{FAULT}}$ output bypasses the serial interface and brings immediate attention to fault conditions detected by the LTC1840, including slow downs in the tachometer and changes in GPIO logic state.

If the $\overline{\text{BLAST}}$ pin is high at start-up or presented with a high to low transition at anytime, the DAC output currents are forced instantaneously to full scale and the chip awaits commands from the serial bus. In addition, when $\overline{\text{BLAST}}$ is set high the LTC1840 guards against system controller crashes with an internal watchdog timer. If the device is not accessed for a period of more than 1.5 minutes, both DAC outputs are set to full scale to guarantee adequate system cooling.

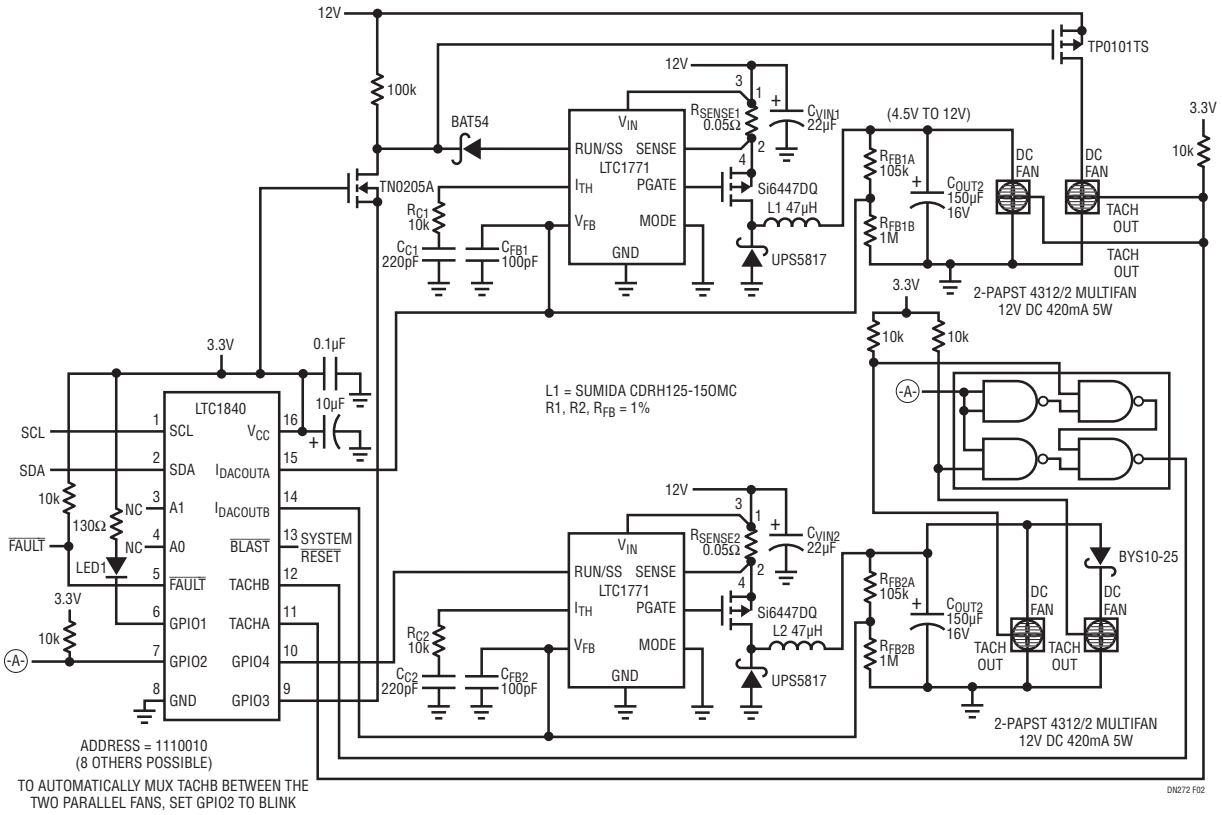


**Figure 2. Controlling Various Fan Operations with the LTC1840**

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