Keywords: Switching Regulator, BUCK Regulator, BUCK Converter, BUCK, Step-down, Multi-phase, Quad-phase, Phase Configuration, General Purpose Input, Enable Control, Voltage Selection, Low Power Mode

APPLICATION NOTE 6822

HOW TO USE MULTI-FUNCTION GPIS?

Abstract: The MAX77812 is a quad-phase, high-current, step-down (BUCK) converter for high-end gaming consoles, VR/AR headsets, DSLR cameras, drones, network switches and routers, and FPGA systems that use multicore processors. The MAX77812 has two user-programmable general-purpose inputs (GPIs) which can be configured as enable, output voltage selection, and low-power mode control input. This document provides information about using these GPIs.

Introduction

The MAX77812 has two general-purpose inputs (GPI0 and GPI1) which can be configured as the enable function of regulators, output voltage selection, low-power mode control, and 'no function'. The function of these two inputs is programmable through the I^2C/SPI (GPI_FUNC register) on the fly.

Enable Control

When GPIx are configured as the output-enable function, the enable logic of a specific regulator is an 'OR' logic of GPIx and the corresponding enable register bit (Mx_EN). For example, the default function of GPI0 is Master 3 Enable (GPI0_FUNC[3:0] = 0011b), so that Master 3 Enable is controlled by GPI0 and the M3_EN bit. If GPI0 is set high earlier than 'Global Enable (EN)' input, Master 3 is enabled earlier than other master phases, as shown in Figure 1. The two GPIs can be configured as the same enable function (e.g., M2_EN = GPI0_FUNC[3:0] = GPI1_FUNC[3:0] = 0010b). In this case, those inputs are ORed with the M2_EN bit. The GLB_EN function (GPIx_FUNC[3:0] = 0000b) allows the host processor to enable all the masters in sequence based on the STUP_DLYx registers. Note that M1 through M4 are defined by the PH_CFG0, PH_CFG1, and PH_CFG2 inputs.

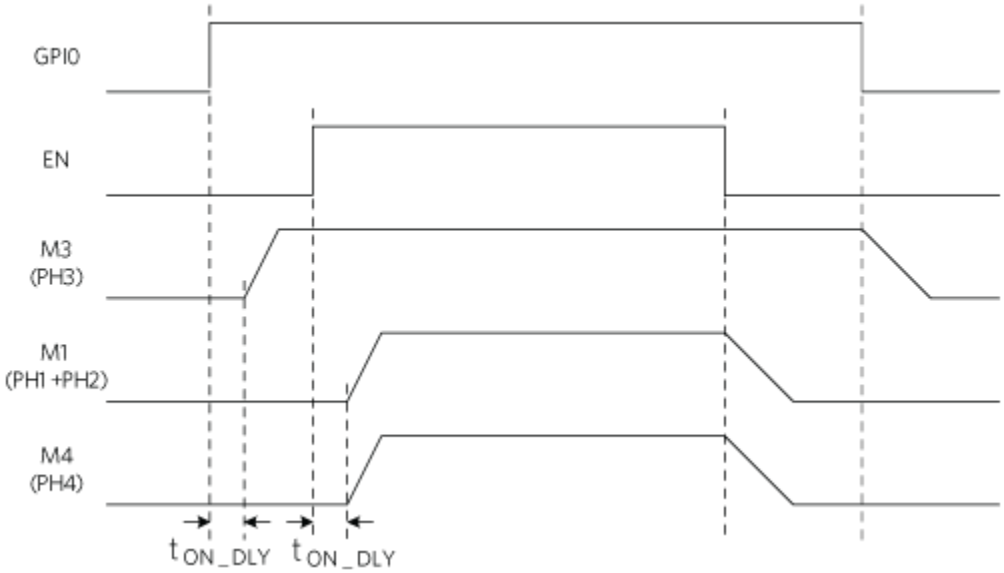

Figure 1. Timing diagram with GPI0 and EN in a 2+1+1 phase configuration.

Voltage Selection

The MAX77812 BUCK has two additional output voltage control registers (Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0]), besides Mx_VOUT[7:0]. Those two additional registers are for storing the default output voltage and the system sleep mode output voltage for a specific host processor.

When GPIx are configured as a voltage selection function, the output voltage of a specific regulator is set by Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0] registers based on the GPIx logic level. For example, if the function of GPI0 is programmed as Global Voltage Selection (GPIx_FUNC[3:0] = 0101b), the output voltages of all the master phases are toggled by GPI0 based on the preset values in Mx_VOUT_D[7:0] (GPI0 = HIGH) and Mx_VOUT_S[7:0] (GPI0 = LOW) registers. In case the two GPIs are configured as the same voltage selection function, those inputs are ORed. During the output voltage transition, the ramp-up/down slew rate is controlled by the B_RU_SR[2:0] and B_RD_SR[2:0] registers.

Low-Power Mode

When GPIx are configured as a Low-Power Mode (LPM) enable function, the Low-Power Mode enable logic of a specific master phase is an ‘OR’ logic of GPIx and the corresponding enable register bit (Mx_LPM). For example, if GPI0_FUNC[3:0] = 1011b, the LPM enable of Master 1 is controlled by GPI0 and M1_LPM bit. In case the two GPIs are configured as the same LPM enable function (i.e., GPI0_FUNC[3:0] = GPI1_FUNC[3:0] = 1100b), those inputs are ORed with the M2_LPM bit. The GLB_LPM function (GPIx_FUNC[3:0] = 1010b) allows the host processor to enable Low-Power Mode for all the masters at the same time.

Table 1. GPI Function Selection Register

Address 0x0F	Mode R/W	Type: O	Reset Value: 0x43
Bit	**Name**	**POR**	**Description**
7:4	GPI1_FUNC[3:0]	0100	GPI1 Function Selection
		0000b: GLB_EN	1000b: M3_VSEL
		0001b: M1_EN	1001b: M4_VSEL
		0010b: M2_EN	1010b: GLB_LPM
		0011b: M3_EN	1011b: M1_LPM
		0100b: M4_EN	1100b: M2_LPM
		0101b: GLB_VSEL	1101b: M3_LPM
		0110b: M1_VSEL	1110b: M4_LPM
		0111b: M2_VSEL	1111b: No Function
3:0	GPI0_FUNC[3:0]	0011	GPI0 Function Selection
		0000b: GLB_EN	1000b: M3_VSEL
		0001b: M1_EN	1001b: M4_VSEL
		0010b: M2_EN	1010b: GLB_LPM
		0011b: M3_EN	1011b: M1_LPM
		0100b: M4_EN	1100b: M2_LPM
		0101b: GLB_VSEL	1101b: M3_LPM
		0110b: M1_VSEL	1110b: M4_LPM
		0111b: M2_VSEL	1111b: No Function

Table 2. Multi-Function GPI Configurations

GPIx_FUNC[3:0]	Function	Remark
0000b	GLB_EN	Global Enable (Master 1 thru to Master 4)
0001b	M1_EN	Master 1 Enable
0010b	M2_EN	Master 2 Enable
0011b	M3_EN	Master 3 Enable
0100b	M4_EN	Master 4 Enable
0101b	GLB_VSEL	Global Voltage Selection (Master 1 thru Master 4)
0110b	M1_VSEL	Master 1 Voltage Selection
0111b	M2_VSEL	Master 2 Voltage Selection
1000b	M3_VSEL	Master 3 Voltage Selection
1001b	M4_VSEL	Master 4 Voltage Selection
1010b	GLB_LPM	Global Low Power Mode Select (Master 1 thru Master 4)
1011b	M1_LPM	Master 1 Low Power Mode Enable
1100b	M2_LPM	Master 2 Low Power Mode Enable
1101b	M3_LPM	Master 3 Low Power Mode Enable
1110b	M4_LPM	Master 4 Low Power Mode Enable
1111b	No Function	

Related Parts		
MAX77812	20A User-Configurable Quad-Phase Buck Converter	Samples

More Information
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