Keywords: trandceiver, E1, transmitter, receiver, transformer, serier resistance, receive circuit, transmit circuit, return loss

APPLICATION NOTE 352

General network interface design criteria for the DS2153 and DS2154

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Abstract: This application note presents a general form of the interface circuit for E1 transceiver chips and shows how to distribute resistance around the transformers. It explains why the transmitter and receiver pins require different protection techniques. It discusses the importance of return loss and shows how to calculate it. The DS2153/DS2154 E1 single-chip transceiver ICs are featured.

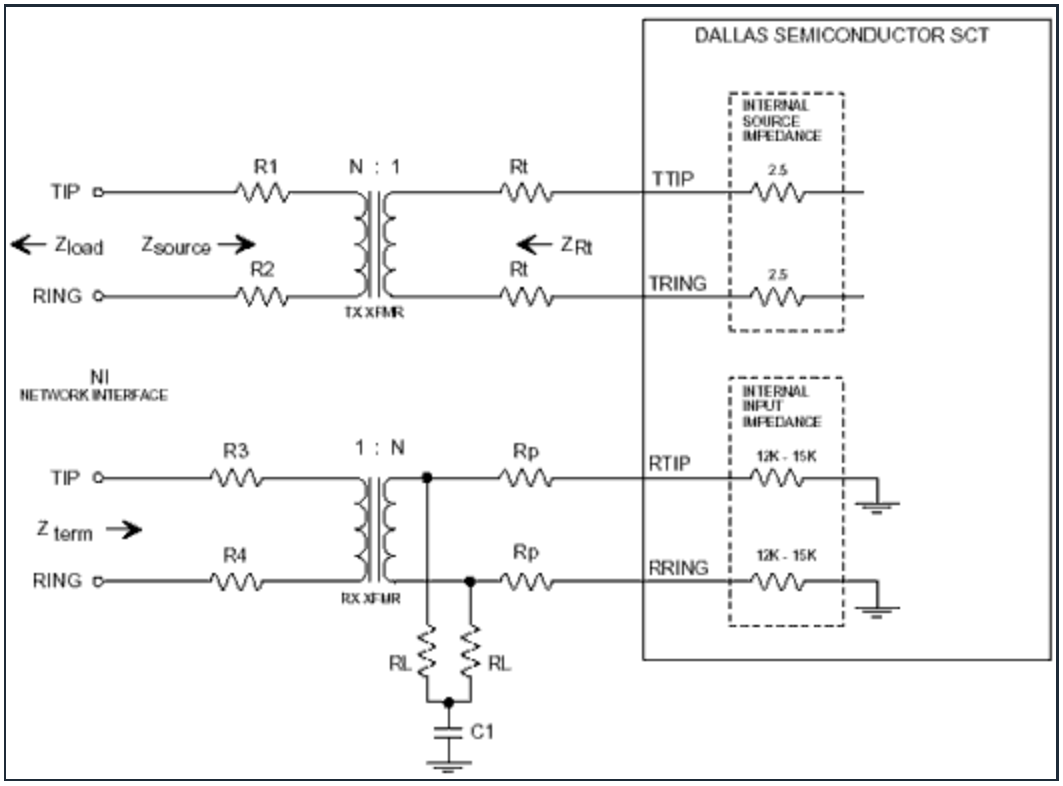

Figure 1. General network interface circuit.

Figure 1 illustrates a general form of the interface circuit for E1 transceiver chips. Not all of the components are necessary in all applications. This circuit is used to illustrate how to distribute resistance around the transformers. Application note 324, "T1/E1 network interface design" discusses over voltage protection in more detail.

The transmitter output drivers present a low impedance to inbound surges and must be able to drive sufficient current in the primary of the transmit transformer in order to produce the required output pulse at the network interface. The receiver inputs present a high impedance to inbound surges and require very little input current to operate. For these reasons, the transmitter and receiver pins require different protection techniques.

The receiver inputs are designed to recover a signal under these conditions:

- 1:1 transformer
- 0Ω series resistance
- Load resistance matched to cable impedance: 75Ω or 120Ω

The 5.0 volt transmitter output drivers are designed to fit a pulse into a template, measured under these conditions:

- 1:1.15 step up transformer
- 0Ω series resistance
- Specified load: 75Ω or 120Ω

The 3.3 volt transmitter output drivers are designed to fit a pulse into a template, measured under these conditions:

- 1:2 step up transformer
- 0Ω series resistance
- Specified load: 75Ω or 120Ω

Receive circuit

The receive circuit is the most straight forward. Generally a 1:1 transformer is used to interface to the receiver inputs. The primary consideration in the receive circuit is the accurate termination of the transmission line. E1 is carried on 75Ω unbalanced Coax or 120Ω balanced twisted pair. The components involved in the termination are R_3, R_4, and the two R_L resistors. R_3 and R_4 are added as part of the protection network. As these resistance values increase, R_L resistance decreases. This then becomes a voltage divider. If R_3 and R_4 are too large, then the signal is divided down and the receiver may be unable to recover weak signals. The two R_P resistors do not significantly affect the termination due to the relatively high input impedance of the receiver inputs. The following equation describes the termination:

Substitute $Z_{TERM} = R_3 + R_4 + 2R_L/N^2$

$Z_{TERM} = 75\Omega$ or $Z_{TERM} = 120\Omega$ and $N = 1$

Then solve for R_3, R_4, and $2R_L$

Capacitor C_1, along with resistors R_L, form a high frequency cutoff filter for improved noise immunity.

Transmit circuit

Several considerations must be made for the transmit interface circuit. Some applications require that the source impedance be closely matched to the characteristic impedance of the network. Along with this there may be a need to provide for protection of the circuit against power line cross (ul) and transient (FCC) conditions. All of these requirements must be considered simultaneously. Matching source impedance to the characteristic impedance of the line prevents reflection of stray signals by the transmitter, and is referred to as Return Loss which is calculated as

$$\text{Return Loss (dB)} = 20\log_{10} |Z_{SOURCE} - Z_{LOAD}|/|Z_{SOURCE} + Z_{LOAD}|$$

Where Z_{LOAD} = 120Ω or 75Ω

$$Z_{SOURCE} = R_1 + R_2 + N_2 (2R_t + 5)$$

When designing for high return loss without the need for circuit protection, R1 and R2 = 0. Resistors R_1, R_2 and R_t are added as part of a protection network. See application note 324. The E1 transceivers have programmable output levels which along with the transmit transformer turns ratio are used to compensate for resistive components between TTIP and TRING and the network interface so that signals arrive at the network interface with a peak voltage of 3.0V for 120Ω applications or 2.37V for 75Ω applications. Table 1 shows which Line Build Out (LBO) settings to choose based on transformer turns ratio and Z_{rt}. All resistance between the device and the network interface must be included in the Z_{rt} which is calculated as

$$Z_{rt} = 2R_t + ((R_1 + R_2/N^2)$$

Table 1. Line build out select in LICR for 5 volt devices

L2	L1	L0	Application	Transformer N	Return Loss[1]	Z_{Rt}[2]
0	0	0	75Ω normal	1.15		0
0	0	1	120Ω normal	1.15		0
0	1	0	75Ω normal with protection resistors	1.15		16.4
0	1	1	120Ω normal with protection resistors	1.15		16.4
1	0	0	75Ω high return loss	1.15	21dB	54
1	1	0	75Ω high return loss	1.36	21dB	36
1	0	0	120Ω high return loss	1.36	21dB	54

Table 2. Line build out select in LICR for 3.3 volt devices

L2	L1	L0	Application	Transformer N	Return Loss[1]	Z_{Rt}[2]
0	0	0	75Ω normal	1:2		0
0	0	1	120Ω normal	1:2		0
0	1	0	75Ω normal with protection resistors	1:2		5
0	1	1	120Ω normal with protection resistors	1:2		5
1	0	0	75Ω high return loss	1:2	21dB	12.4
1	0	1	120Ω high return loss	1:2	21dB	23.2

Note

1. The return loss in this table is a minimum value, the actual calculated value will exceed 21dB. Empty cells indicate that return loss is less than 21dB.
2. The above table differs from the data book in that it shows the total Z_{Rt}. The table in the data book shows the individual values of Rt and assumes R1 and R2 = 0.

Related Parts	
DS2154	Enhanced E1 Single Chip Transceiver

More Information
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