

MAXIM Engineering Journal

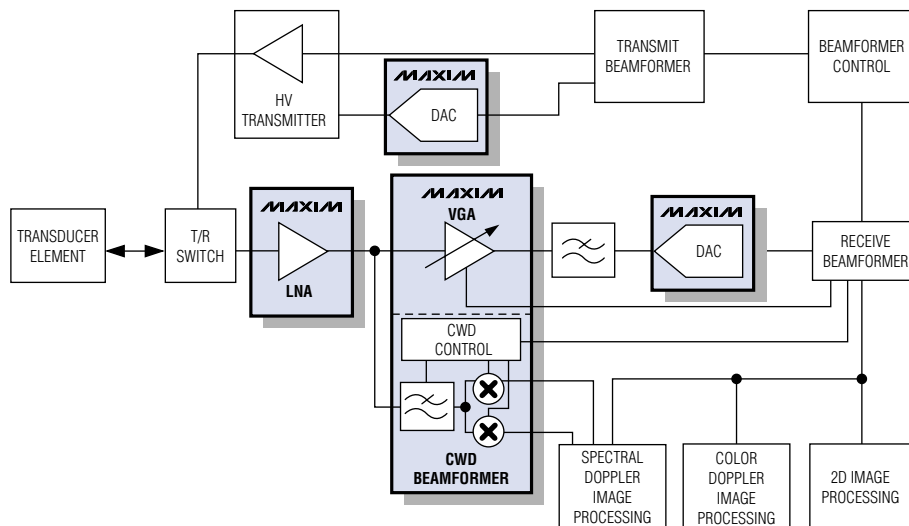
Volume Sixty

LETTER FROM THE CEO

2

IN-DEPTH ARTICLES

Three Is a Crowd for Instrumentation Amplifiers	3
Optimizing Ultrasound-Receiver VGA Output-Referred Noise and Gain	9
Robust Fail-Safe Biasing Circuit for AC-Coupled Multidrop LVDS Bus	14
Regain Location Information by Leveraging the 1-Wire Chain Function	16



A single transmit-and-receive channel is shown for a typical phased-array medical ultrasound imaging system. (See page 12.)

Letter from the CEO

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Maxim has introduced more than 5,000 products to date. Few, if any, other companies innovate at the rate that Maxim does. Our analog and mixed-signal IC products are constantly redefining what is possible, and enable next-generation advancements in numerous products and technologies over a broad array of end-equipment applications. Our success is largely due to our ability to continually define and invent products that add value to our customers' designs. We remain committed to developing cutting-edge products that take advantage of our world-class engineering talent and our large library of unique and proprietary process technologies.

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Equally important is the level of customer service that we provide. Maxim offers a wide variety of services to our customers, including new product updates, expert technical guidance from our Field Applications Engineers, complete and ready-to-go application-specific reference designs, and personalized assistance with orders, pricing, and delivery, just to name a few.

You, the engineer, have always been our most important customer. As a fellow engineer, I appreciate how important it is to have confidence in the consistent performance, quality, and availability of the components that you select for your projects. When you use a Maxim product in your design, know that it comes with our commitment to all of these important criteria.



Tunç Doluca
President and Chief Executive Officer

Three Is a Crowd for Instrumentation Amplifiers

Three-op-amp instrumentation amplifiers have long been the industry standard for precision applications that require high gains and/or high CMRR. However, these amplifiers have serious limitations when operating from the single-supply voltage rails required in many modern applications. This article explains the limitations of the conventional three-op-amp architecture for instrumentation amplifiers, and introduces Maxim's indirect current-feedback architecture that offers specific advantages for single-supply operation of instrumentation amplifiers. Detailed analysis is supported by laboratory waveforms.

Instrumentation Amplifier Applications

Instrumentation amplifiers amplify small differential voltages in the presence of large common-mode voltages, while offering a high input impedance. This characteristic has made them attractive to a variety of applications, such as strain-gauge bridge interfaces for pressure and temperature sensing, thermocouple temperature sensing, and a variety of low-side and high-side current-sensing applications.

Three-Op-Amp Instrumentation Amplifiers

The classic three-op-amp instrumentation amplifier (see **Figure 1**) offers excellent common-mode rejection and accurate differential gain programmable by a single resistor. The architecture is based on a two-stage configuration: the first stage provides unity common-mode gain and all (or most) of the differential gain, while the

second stage provides unity (or small) differential-mode gain and all of the common-mode rejection (see **Figure 2**).

Most low-voltage modern amplifiers have rail-to-rail output, but not necessarily rail-to-rail input. Still, let us consider an extremely high-gain, rail-to-rail input and output, three-op-amp instrumentation amplifier working from a single-supply (V_{CC}), similar to that shown in Figure 1.

Because $V_{OUT} = \text{gain} \times V_{DIFF} + V_{REF}$, it follows that:

$$\begin{aligned}(V_{OUT1}, V_{OUT2}) &= V_{CM} \pm (\text{gain} \times V_{DIFF}/2) \\ &= V_{CM} \pm (V_{OUT} - V_{REF}) / 2\end{aligned}$$

To prevent V_{OUT1} and V_{OUT2} from hitting the supply rails, it should be ensured that:

$$\begin{aligned}0 < (V_{OUT1}, V_{OUT2}) < V_{CC} \\ (\text{i.e., } 0 < V_{CM} \pm (V_{OUT} - V_{REF}) / 2 < V_{CC})\end{aligned}$$

noting that:

$$0 < V_{OUT} < V_{CC}$$

Applications often set $V_{REF} = 0$ (for unipolar input signals) or $V_{REF} = V_{CC}/2$ (for bipolar input signals).

With $V_{REF} = 0$, the inequality reduces to:

$$0 < V_{CM} \pm V_{OUT}/2 < V_{CC}$$

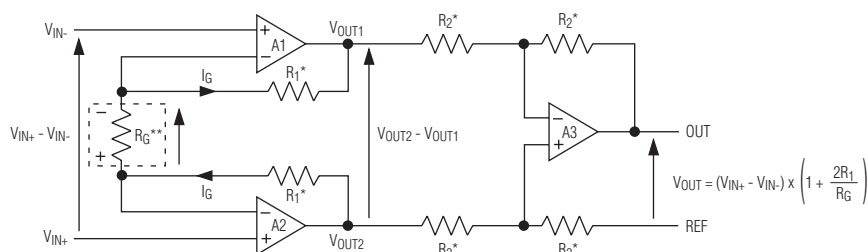
With $V_{REF} = V_{CC}/2$, the inequality reduces to:

$$0 < V_{CM} \pm V_{OUT}/2 \pm V_{CC}/4 < V_{CC}$$

These conditions are best understood graphically, as shown in **Figure 3**.

The grey areas in Figure 3 show the range of input common-mode voltages (in relation to input differential voltages), where the outputs of the Figure 1 amplifiers ($A1$, $A2$) will not saturate into the supply rails. This range depends on V_{OUT} and V_{REF} . Because $V_{OUT} - V_{REF}$ is really an amplified version of the input differential voltage, the allowed common-mode input range varies depending on the input differential voltage.

Practically, of course, it is best to make maximum use of the circuit's gain—to obtain the full output swing (V_{OUT})



* $R_1 = R_2 = 25k\Omega$

** R_G = INTERNAL TO MAX4195/MAX4196/MAX4197,

R_G = EXTERNAL TO MAX4194

Figure 1. Internal architecture is shown for the MAX4194–MAX4197 family of three-op-amp instrumentation amplifiers.

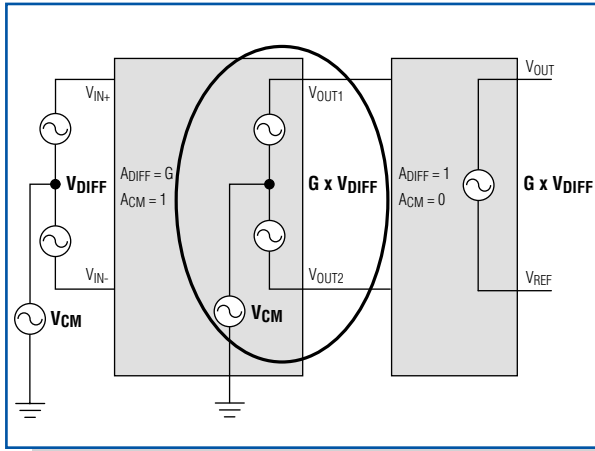


Figure 2. In this two-stage amplification of input signals, input common-mode voltage is carried through to the intermediate stage (circled).

when the maximum expected differential voltages are seen by the inputs. The black areas in **Figure 4** show the range of input common-mode voltages where the instrumentation amplifier amplifies the maximum input differential voltage so that $V_{OUT} = 0$ or $V_{OUT} = V_{CC}$.

As can be seen, the input common-mode voltage is severely restricted in both scenarios. In particular:

- If one wants to fully amplify a unipolar input-differential signal (setting $V_{REF} = 0$ and obtaining full output swing from 0 to V_{CC}), the signal must be present with a common-mode voltage of $\frac{1}{2}V_{CC}$. At any other common-mode voltage, the output voltage will not reach the full swing of V_{CC} (the maximum input differential voltage is reduced). For bipolar input differential signals (with $V_{REF} = \frac{1}{2}V_{CC}$), the corresponding range of input common-mode voltages, where one can achieve full output voltage swing of 0 to V_{CC} , is only between $\frac{1}{4}V_{CC}$ and $\frac{3}{4}V_{CC}$.
- In both cases, if the input common-mode voltage were to be at or close to ground (0V), then the amplifier loses all ability to amplify input differential voltages.

Therefore, assuming that the input differential (wanted) voltages are unrelated to the input common-mode (unwanted) voltages, the black areas represent design minima and maxima for V_{CM} that can be tolerated for the full range of V_{OUT} . Outside this area, certain combinations of V_{DIFF} and V_{CM} may not result in a permissible V_{CM} .

Note that, in the case of the Figure 4a, if full-scale V_{CM} variation is required, the input common-mode voltage tolerance is zero. Simply put, no common-mode variation of the input signal is allowed.

As a result, three-op-amp instrumentation amplifiers find only limited applications in single-supply systems. It is worthwhile to continue this discussion to answer two questions:

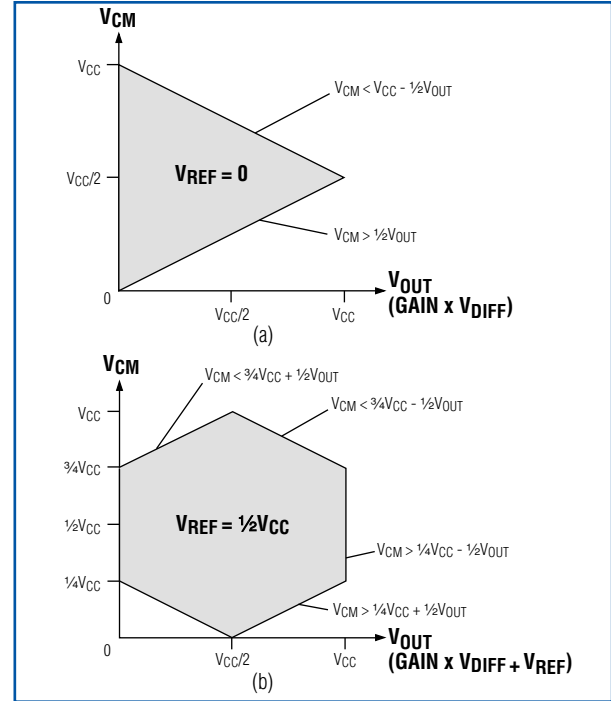


Figure 3. The usable V_{CM} at various input differential voltages for a single-supply, three-op-amp instrumentation amplifier is shown with (a) $V_{REF} = 0$ and (b) $V_{REF} = V_{CC}/2$. The horizontal axis is the amplified input differential voltage (V_{OUT}).

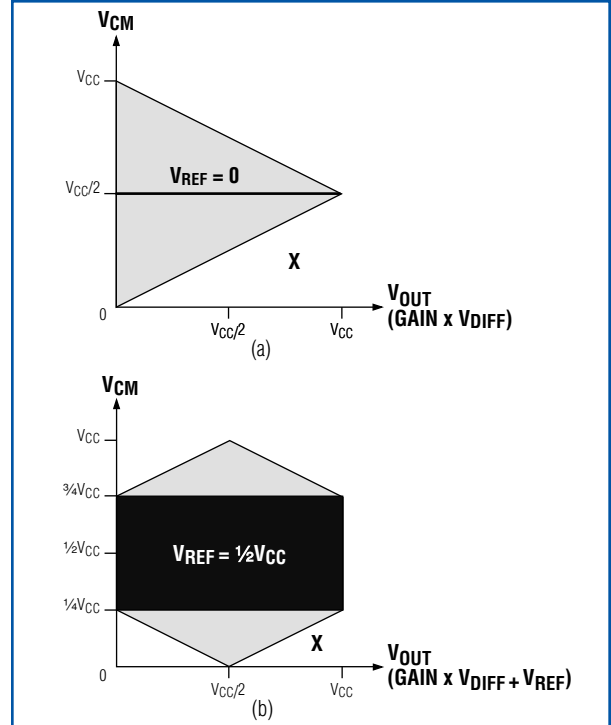


Figure 4. The black box shows the range of input common-mode voltages in which the conventional three-op-amp instrumentation amplifier uses its gain to give a maximum output voltage (i.e., at a maximum input differential voltage) with (a) $V_{REF} = 0$ and (b) $V_{REF} = V_{CC}/2$.

- (1) What happens if the internal amplifiers (A1 and A2) saturate into the rails?
- (2) What is the effect of non-rail-to-rail input architectures?

Effect of Input-Amplifier Saturation

Consider the case when the output of amplifier A1 has saturated into ground. In other words, $V_{IN+} > V_{IN-}$, and the common-mode voltage is in the area marked X in Figure 4. (V_{DIFF} is larger than allowed by the grey area.)

Because A1 is saturated ($V_{OUT1} = 0$), it transitions into a comparator (nonlinear) mode of operation, and the voltage at its inverting pin is no longer constrained to be the same as its noninverting pin (V_{IN-}). Amplifier A2 then acts as a noninverting amplifier with a gain of $1 + R1 / (R1 + R_G)$ for voltages at its noninverting pin (V_{IN+}). For a high-gain amplifier, $R_G \ll R1$ and, therefore, amplifier A2 simply acts as an amplifier with a noninverting gain of 2:

$$V_{OUT2} = 2 \times V_{IN+} = 2 \times (V_{CM} + V_{DIFF}/2) \\ = 2 \times V_{CM} + V_{DIFF}$$

The second-stage differential amplifier, A3, simply examines its inputs V_{OUT1} and V_{OUT2} , and presents the difference at its output:

$$V_{OUT} = (2 \times V_{CM} + V_{DIFF}) + V_{REF}$$

Similarly, if A2 saturates to ground:

$$V_{OUT} = -(2 \times V_{CM} - V_{DIFF}) + V_{REF}$$

This is a potentially hazardous mode of operation for the three-op-amp instrumentation amplifier. Not only has it stopped amplifying the input differential voltage, but instead of “gracefully degrading” in some fashion, the three-op-amp instrumentation amplifier transitions into a mode that amplifies the input common-mode voltage relative to the input differential voltage. This problem is exacerbated by the fact that common-mode voltages are generally uncontrolled and probably are unwanted noise that corrupts signals of interest. This is a serious issue, as the primary reason for using the instrumentation amplifier is to eliminate such noise.

Effect of Non-Rail-to-Rail Input Architectures

As mentioned earlier, most amplifiers have rail-to-rail output, but not rail-to-rail input. Rail-to-rail input stages are especially difficult to design for precision applications, because the crossover between near- V_{CC} common-mode voltage operation and near-GND common-mode voltage operation can never be perfect—during this transition, offset voltages can arise between n-type and p-type pairs in the input differential stage. A low V_{OS} and a high CMRR are key specifications for a well-designed, precision instrumentation amplifier. Because $CMRR = \Delta V_{OS} / \Delta V_{CM}$, the change in V_{OS} when changing common-mode

voltage across the crossover region severely degrades the CMRR specification.

As a result, most precision instrumentation amplifiers tend to be non-rail-to-rail input type, though they still include the negative rail (0V) as part of the input common-mode voltage range. If we re-examine Figure 3, taking into account its input common-mode voltage limitations and redrawing the graphs, we can reason that the graphs will look like those in **Figure 5**.

The Indirect Current-Feedback Architecture

The indirect current-feedback architecture is a new approach to designing instrumentation amplifiers that has become extremely popular for its multiple benefits. **Figure 6** shows the indirect current-feedback architecture as used in the MAX4462 and MAX4209 instrumentation amplifiers.

This new architecture contains a high-gain amplifier (C) and two transconductance amplifiers (A and B). Each transconductance amplifier converts its input differential voltage into an output current and rejects all of its input common-mode voltage. At the stable operating point for the amplifier, the output current sourced from the g_M stage A matches the input current sunk by g_M stage B. This current matching is enabled by feedback action through high-gain amplifier C, which forces the differential voltage at the input of feedback amplifier B to be the same as the differential voltage at the inputs of amplifier A. This design

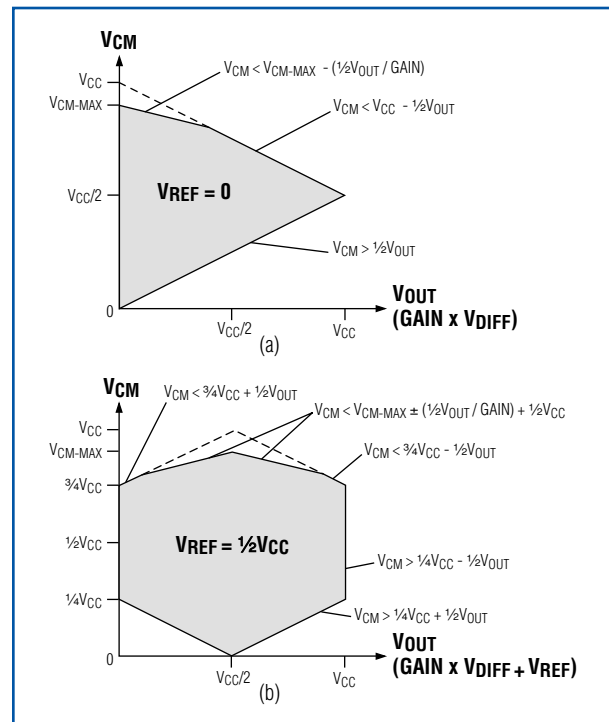


Figure 5. The usable input common-mode voltage at various input differential voltages for a single-supply, three-op-amp instrumentation amplifier accounts for a non-rail-to-rail input stage with (a) $V_{REF} = 0$ and (b) $V_{REF} = V_{CC}/2$.

then sets up a defined current in the output resistor chain (equal to $V_{DIFF} / R1$), which also flows through R2. Therefore, the output voltage at OUT is simply a gained-up version of the input differential voltage (gain = $1 + R2 / R1$). The output can be offset by feeding an arbitrary reference voltage at REF, much like a standard three-op-amp instrumentation amplifier.

By translating the part operation to a high-level block diagram, as in **Figure 7**, and by comparing it to Figure 2, a key advantage emerges. The intermediate signal in the three-op-amp instrumentation amplifier contains not only the gained-up differential voltage, but also the input common-mode voltage. However, the indirect current-feedback architecture contains only a recent representation of the input differential voltage. The first stage provides all the common-mode rejection. The second stage then offers all the differential gain and reinforces common-mode rejection, thereby allowing the output to be offset by a

reference voltage, if necessary. As a result, the input common-mode voltage limitations that are present in the three-op-amp instrumentation amplifier simply do not exist within the indirect current-feedback architecture.

Taking into account the input common-mode voltage limitations (i.e., a non-rail-to-rail input stage), the transfer characteristics then would behave similarly to that shown in **Figure 8**. The black areas show the design limit of input common-mode voltages in which the full output-voltage range is achievable. The grey areas illustrates the range of input common-mode voltages in which the instrumentation amplifier operates as expected—it outputs a voltage proportional to a gained-up version of the input differential voltage, and it rejects all input common-mode voltage.

Experimental Results

The following experimental results effectively support the indirect current-feedback discussion. Consider the

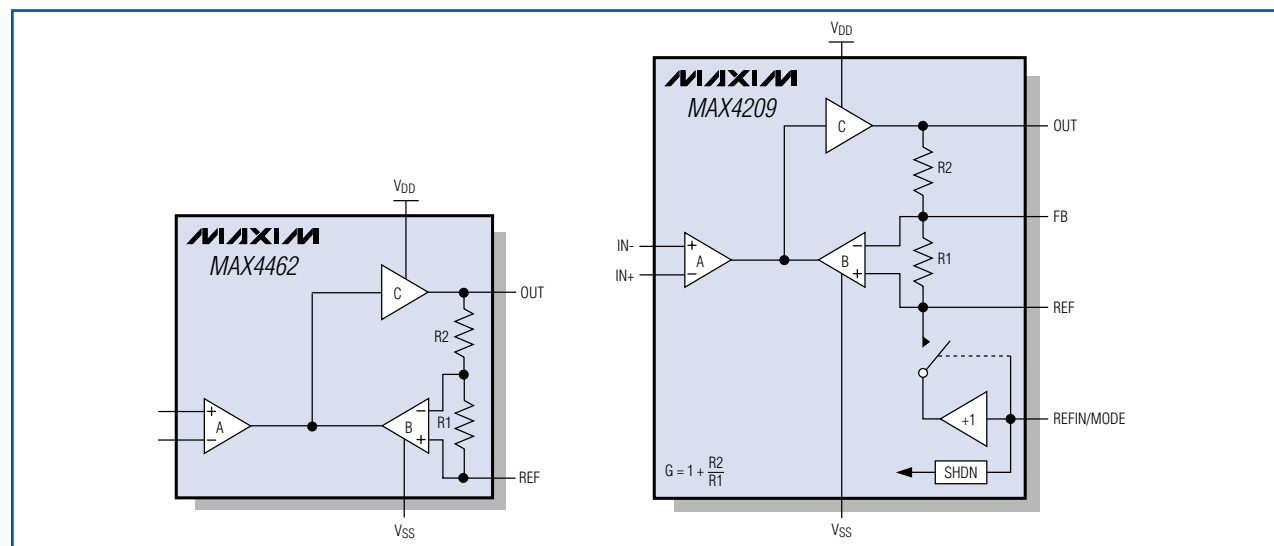


Figure 6. Indirect current-feedback architecture is used in the MAX4462 and MAX4209 instrumentation amplifiers.

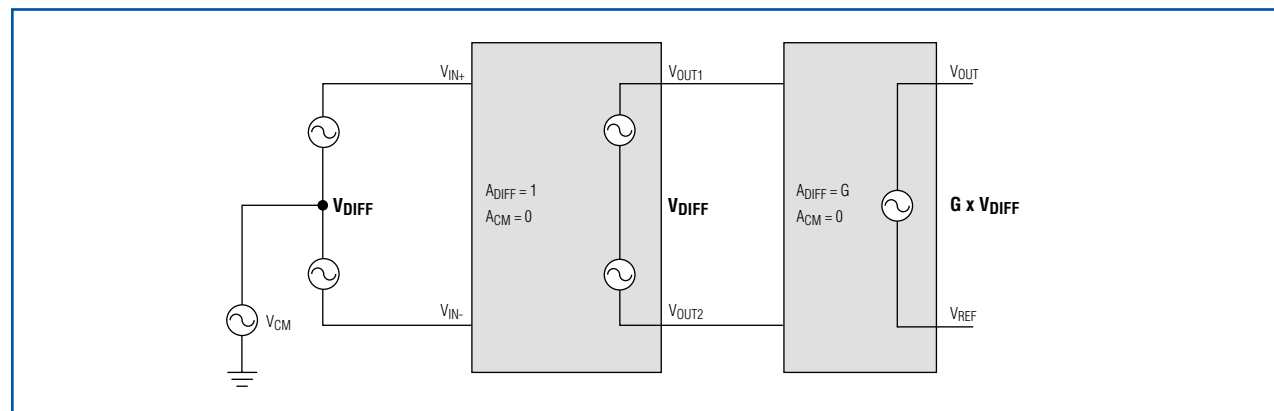


Figure 7. The operation of an indirect current-feedback instrumentation amplifier has no common-mode voltage in the output of the first stage.

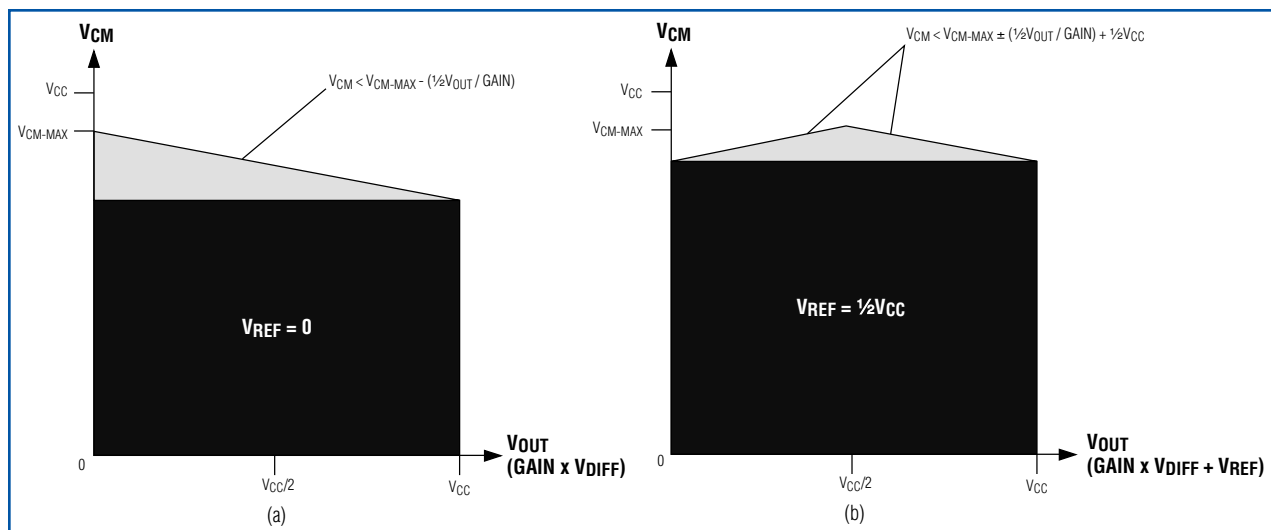


Figure 8. The usable range of input common-mode voltages for an indirect current-feedback instrumentation amplifier is shown in grey and black. In both (a) and (b), the black area, which is a subset of the grey area, shows where the full output voltage is achievable.

MAX4197 and the MAX4209H. Both are instrumentation amplifiers with a gain of 100. The MAX4197 has a three-op-amp architecture, while the MAX4209H is an indirect current-feedback instrumentation amplifier. Both parts are supplied with a $V_{CC} = 5V$ and a $V_{REF} = 2.5V$ to offset the zero output of the device.

In this experiment, two types of waveforms are input to the instrumentation amplifier.

Case 1 has a 1kHz differential voltage in the presence of a large 100Hz common-mode voltage. The output of the instrumentation amplifier is expected to contain only a 1kHz signal with no 100Hz components. The waveforms can be approximated as:

$$V_{IN+} = \text{sine-wave amplitude} = 2V_{P-P}, \\ \text{offset} = 1V, \text{ frequency} = 100\text{Hz}$$

$$(V_{IN+} - V_{IN-}) = \text{sine-wave amplitude} = 30mV_{P-P}, \\ \text{offset} = 0, \text{ frequency} = 1\text{kHz}$$

Case 2 has a 100Hz differential voltage in the presence of a large 1kHz common-mode voltage. The output of the instrumentation amplifier is expected to contain only a 100Hz signal with no 1kHz components. The input waveforms can be approximated as:

$$V_{IN+} = \text{sine-wave amplitude} = 2V_{P-P}, \\ \text{offset} = 1V, \text{ frequency} = 1\text{kHz}$$

$$(V_{IN+} - V_{IN-}) = \text{sine-wave amplitude} = 30mV_{P-P}, \\ \text{offset} = 0, \text{ frequency} = 100\text{Hz}$$

The results follow, where channel 1 is V_{IN+} , channel 2 is V_{IN-} , and channel 3 is the output of the instrumentation amplifier.

Case 1 Results

In **Figure 9a**, the MAX4209H shows the expected result. The MAX4197 gives the expected results only when the input common-mode voltage is well above ground (**Figure 9b**). The 100Hz component in the MAX4197's output voltage is obvious.

Case 2 Results

Again, the MAX4209H shows the expected results (**Figure 10a**). The MAX4197 amplifies the input differential signal only when the common-mode voltage is well above ground (**Figure 10b**). When the common-mode voltage is close to ground, the output voltage either inverts the common-mode voltage or simply buffers it, depending on whether A1 or A2 saturates (as explained earlier).

Conclusion

In the midst of an unprecedented era of high-performance electronic devices, today's consumers demand not only better performance, but also more intelligent power-management schemes to enable longer battery life and energy efficiency. A transition from dual-supply analog designs to single-supply architectures is already underway that is changing the way electronics are designed and used. New, innovative architectures, such as the indirect current-feedback architecture described in this article, are making the dreams of yesterday into realities of today.

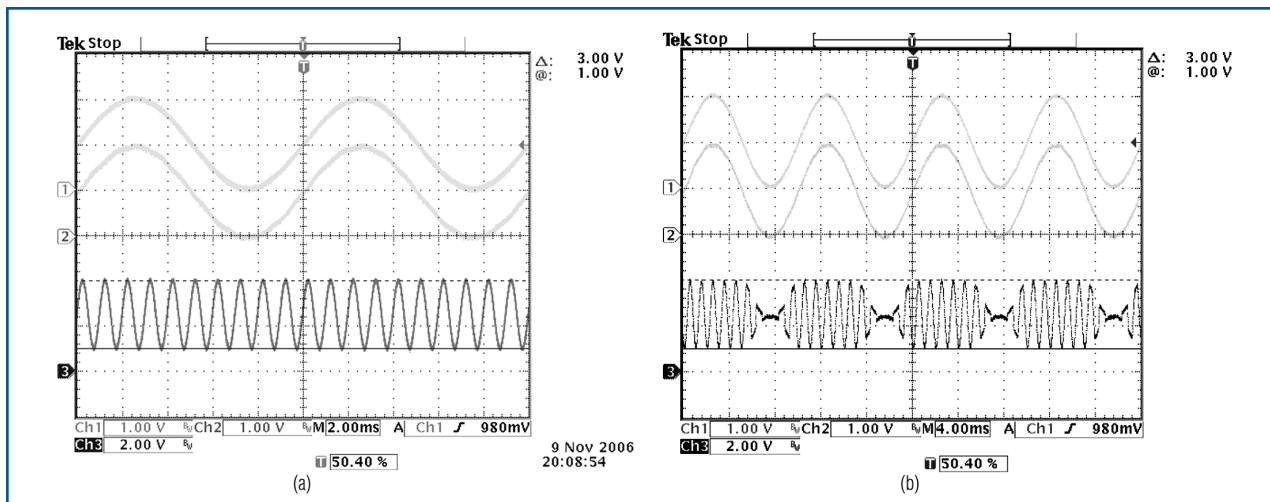


Figure 9. The results are shown for Case 1 with (a) the MAX4209H indirect current-feedback architecture and (b) the MAX4197 three-op-amp architecture. Note that the 1 kHz V_{DIFF} is too small to be visible on the input 1 and input 2 traces, whereas the 100 Hz V_{CM} dominates.

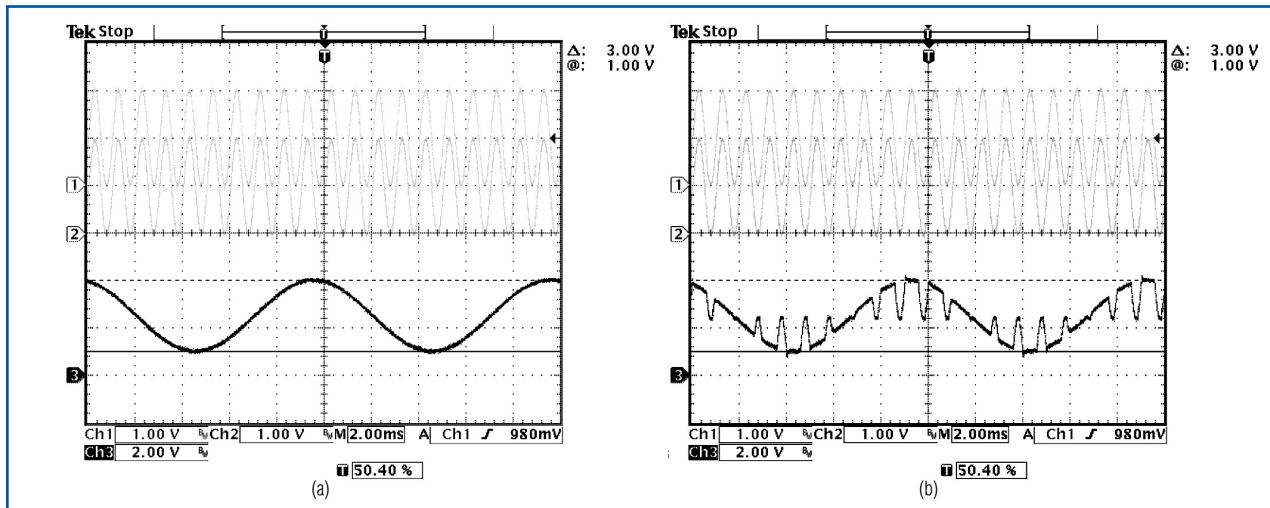


Figure 10. The results are shown for Case 2 with (a) the MAX4209H indirect current-feedback architecture and (b) the MAX4197 three-op-amp architecture. Note (as with Figure 9) the breakthrough of the 1 kHz V_{CM} over the desired output for the three-op-amp instrumentation amplifiers. The indirect current-feedback architecture maintains its excellent performance.

Optimizing Ultrasound-Receiver VGA Output-Referred Noise and Gain

Improves Doppler Dynamic Range and Sensitivity

A critical component in phased-array ultrasound receivers is the variable-gain amplifier (VGA), sometimes referred to as a time-gain control (TGC) amplifier. In this article, we examine how VGA output-referred noise and gain can have a pronounced affect on ultrasound pulsed Doppler dynamic range and sensitivity, and how the MAX2037 octal ultrasound VGA has optimized these parameters to yield the best overall system performance in a typical receiver lineup.

Phased-Array Receiver Overview

Before we examine how these critical VGA specifications affect Doppler performance, it is helpful to review the basic elements and operation of a typical phased-array ultrasound receive channel. For a high-level overview of phased-array ultrasound receivers, see *Appendix A—Phased-Array Ultrasound System Basics* (on page 12). A typical receiver lineup consists of an LNA, a VGA, an anti-alias filter, and an ADC (as shown in **Figure 1**). The LNA amplifies single-ended input signals between 1MHz and 15MHz

from a single transducer element. The LNA has approximately 19dB of gain and an active input impedance of between 50Ω and 1kΩ, optimized to match the transducer element and maintain an ultra-low noise figure.

At the beginning of a receive cycle immediately after a transmit burst, the signal at the LNA input can be as large as 0.5V_{P-P}. Over the receive interval, the signal strength attenuates and ultimately falls below the noise floor of the receiver. The rate of attenuation can be calculated knowing that acoustic energy attenuates in the human body at a rate of approximately 0.7dB/cm-MHz (1.4dB/cm-MHz, round trip) and that the propagation velocity of sound in the body is 1540m/s (13μs, round trip). The dynamic range required to process this signal over the full receive interval is approximately 110dB and is well beyond the range of a realistic ADC converter. As a result, the receiver gain is dynamically increased over the receive interval using a VGA (hence the term “time-gain control”) to map this signal into the available ADC input dynamic range. A VGA with approximately 40dB of gain range is required to map the received signal into a 12-bit ADC with 70dB of dynamic range. The three-pole anti-alias filter in the Figure 1 receive chain keeps the ADC from mapping high-frequency noise and extraneous signals beyond the normal maximum imaging frequencies of 15MHz. The ADC is typically a 12-bit ADC running at anywhere from 40MSPs to 60MSPs.

VGA Output-Referred Noise and Gain, and Its Affect on PW Doppler

Standard 2D, grayscale ultrasound imaging typically requires about 40dB of dynamic range per phased-array channel. However, pulsed Doppler imaging modalities, such as spectral PW Doppler and color-flow imaging, require as much as 70dB because the received signal

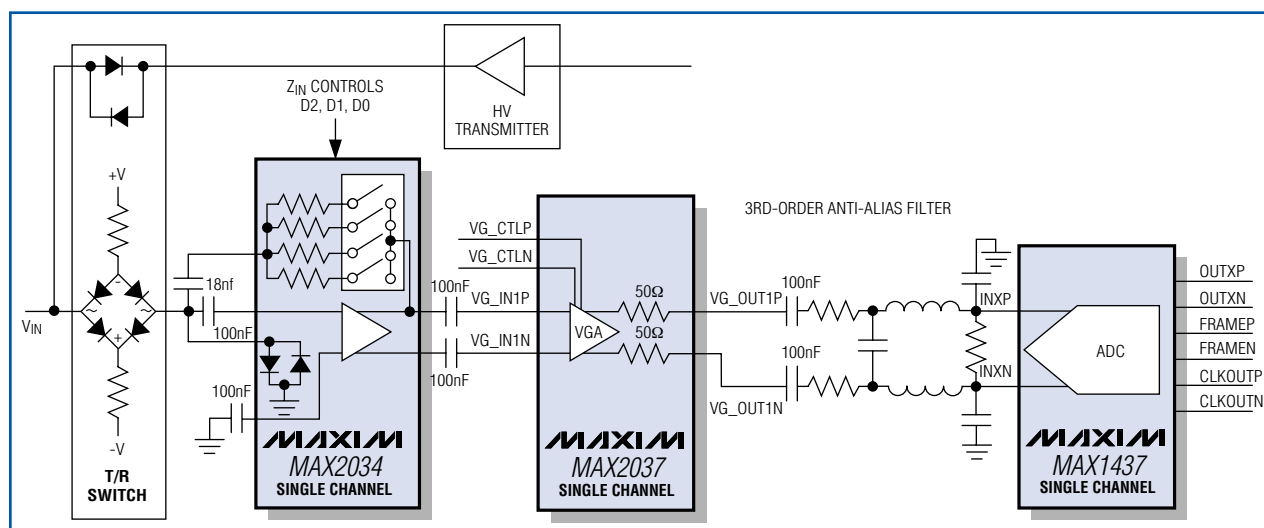


Figure 1. A typical phased-array ultrasound-receiver lineup consists of an LNA, a VGA, an anti-alias filter, and an ADC.

strength from blood can be substantially weaker than signals from surrounding tissue. For this reason, high-dynamic-range 12-bit ADCs are used to improve receiver Doppler performance.

Designing VGAs compatible with these ADCs in an ultrasound receiver lineup is a significant challenge. Specifically, it is difficult to maintain low output-referred noise to preserve receiver dynamic range while still providing enough gain to ensure that a low receiver noise figure is maintained at high-TGC levels. Low output-referred noise and high maximum gain generally are mutually exclusive benefits in practical VGA implementations. Designers of VGAs for this application must optimize and properly balance these VGA properties to ensure the best overall receiver performance.

To better understand how these VGA properties affect the performance of the receiver, let us consider two specific cases. One situation is when the TGCs are at medium and low gains and the received signal levels are relatively large. Under these conditions, it is important to optimize receiver dynamic range. The other case is when the TGCs are at maximum gain and the signal levels are small. In the latter case, preserving sensitivity by optimizing receiver noise figure is paramount.

Effect of VGA Output-Referred Noise on Receiver Dynamic Range (Medium- to Low-TGC Gain Condition)

At medium- and low-TGC levels, the VGA output noise is dominated by the output-referred noise of the VGA. This noise must be significantly below the ADC's noise floor, otherwise the ADC's dynamic range is sacrificed. Consider the ultrasound receiver lineup shown in Figure 1. The MAX2037 VGA has approximately $22\text{nV}/\sqrt{\text{Hz}}$ of output-referred noise. The MAX1437 12-bit, 50Msps ADC used to

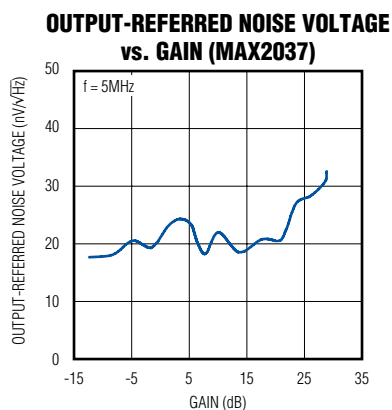


Figure 2. The MAX2037 features half the noise of competitive devices, while providing much higher gain.

digitize the VGA's output has a $31.7\text{nV}/\sqrt{\text{Hz}}$ noise floor, given that the ADC's maximum input voltage is $1.4\text{V}_{\text{P-P}}$ and its specified SNR is 70dB. If the passive anti-alias filter between the VGA and ADC in this example has 0dB attenuation in the passband, then the 70dB SNR of the ADC would effectively be reduced by 1.7dB to 68.3dB as a result of the VGA's contributed output-referred noise. In practice, however, most anti-alias filters used in this application have some passband attenuation.

For stability reasons, many VGAs require some form of real output impedance driving the filter. These impedances must be large enough so the capacitor values in the filter are not unrealistically small. Such constraints usually result in a practical anti-alias filter with between 3dB to 6dB of attenuation in the passband. Attenuation in the anti-alias filter passband further reduces the output-referred noise seen at the input of the ADC and improves dynamic range. With 6dB of passband attenuation, there is only a 0.49dB reduction in the ADC's SNR due to the MAX2037's output-referred noise.

It is easy to see that VGAs with significantly more output-referred noise than the MAX2037 can be problematic. For example, VGAs with just $40\text{nV}/\sqrt{\text{Hz}}$ of output-referred noise, which is nearly twice the level of the MAX2037, result in a 1.5dB reduction in the ADC's SNR when using a 6dB attenuation anti-alias filter. This is a significant reduction, especially in difficult-to-image pulsed Doppler applications. It is important to note that the reduction in receiver gain caused by attenuation in the anti-alias filter can have significant negative effects on receiver noise figure, as we shall examine in more detail in the next section of this article.

The MAX2037 provides approximately half of the output-referred noise of competitive devices. It also has a significantly higher maximum gain to optimize dynamic range and preserve receiver noise figure when used with 12-bit ADCs and realistic passive anti-alias filters. **Figure 2** shows a plot of the MAX2037 output-referred noise as a function of gain.

Effect of VGA Maximum Gain on Receiver Noise Figure (High-TGC Gain Condition)

At high-TGC levels, where the receiver is optimized for small-signal sensitivity, the VGA's combined output-referred noise and the ADC's noise floor should be much less than the amplified transducer noise floor seen at the ADC's input.

The **Figure 3** simplified, ultrasound-receiver block diagram shows how receiver gain before the ADC affects noise-figure performance. The receiver lineup assumes the MAX2034 quad LNA with 19dB of gain, the MAX2037 VGA with a maximum gain of 29.5dB, and the MAX1437 octal 12-bit ADC. It also assumes an anti-alias filter with

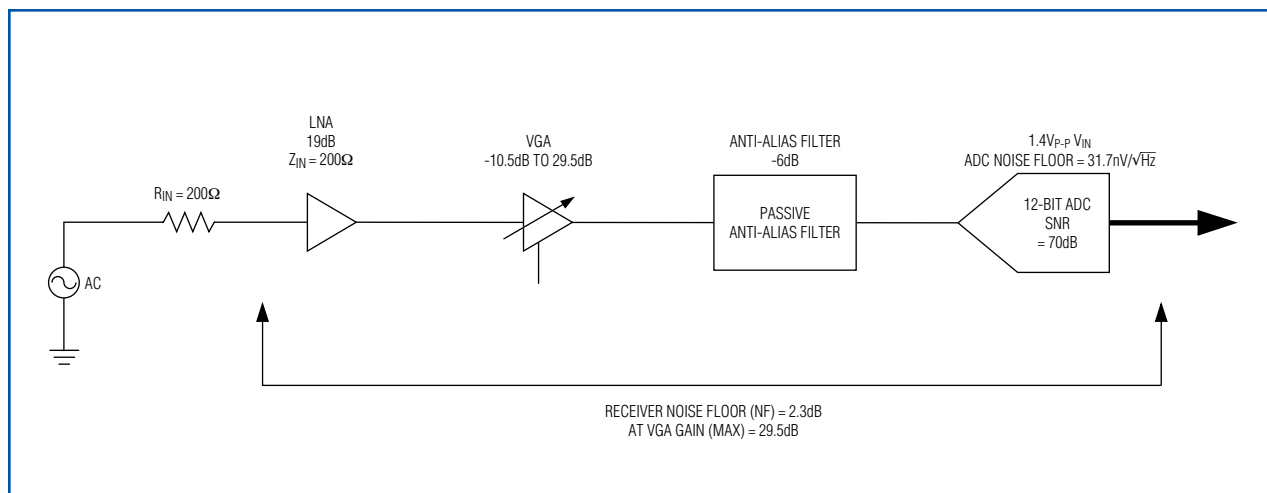


Figure 3. Gain before the ADC affects noise-figure performance in this simplified ultrasound-receiver block diagram.

6dB of attenuation in the passband. The assumed transducer impedance is 200Ω , which yields a thermal noise floor of $V_N = \sqrt{(4 \times K \times T \times R \times \Delta F)}$ or $1.8\text{nV}/\sqrt{\text{Hz}}$. The thermal noise floor at the LNA input, assuming an LNA Z_{IN} of 200Ω , is half of this value ($0.9\text{nV}/\sqrt{\text{Hz}}$). The full receiver lineup noise figure in this case is approximately 2.3dB when using typical noise specifications for the LNA, VGA, and ADC. The noise floor of the MAX1437 is $31.7\text{nV}/\sqrt{\text{Hz}}$. At maximum TGC levels, the gain of this lineup before the ADC, including the anti-alias filter, is 42.5dB. The ADC noise referred to the receiver input in this example is only $0.237\text{nV}/\sqrt{\text{Hz}}$ and, as a result, the ADC contributes only 0.18dB to the total receiver 2.3dB noise figure.

What happens if the VGA has less maximum gain or the ADC's noise floor is higher? **Figure 4** shows the effect that VGA gain has on the small-signal noise figure of the typical ultrasound receiver shown in Figure 3. We plotted the noise figure for two different ADC noise floors, assuming that a MAX2034 low-noise ultrasound LNA with 19dB of gain and an anti-alias filter with 6dB of attenuation are in the receiver lineup. The top curve in the graph represents the MAX1437 with 1.4V_{P-P} maximum input voltage, SNR of 70dB, and a noise floor of approximately $31.7\text{nV}/\sqrt{\text{Hz}}$. The other curve represents an ADC with 2V_{P-P} inputs, SNR of 70dB, and a resulting noise floor of approximately $45.2\text{nV}/\sqrt{\text{Hz}}$. The graph clearly shows the effect of receiver noise figure on these two different ADCs. It also illustrates how the high 29.5dB maximum gain of the MAX2037 results in improved receiver noise figure.

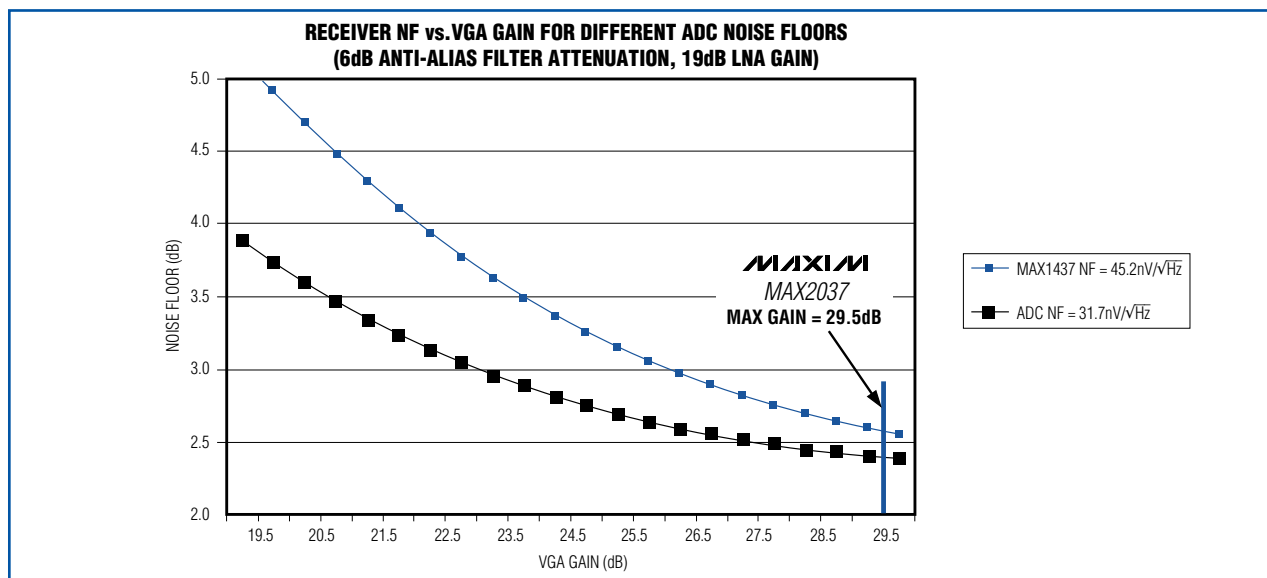


Figure 4. Receiver noise figure vs. VGA gain is shown for the Figure 3 ultrasound receiver.

VGAs with less maximum gain result in higher overall receiver noise figure at maximum TGC levels and reduced small-signal Doppler sensitivity. A significant improvement in noise figure can be achieved by proper use of low-noise-floor ADCs, like the MAX1437, and high maximum gain VGAs, like the MAX2037.

Conclusion

Proper attention to the affect of VGA output-referred noise, maximum VGA gain, anti-alias filter attenuation, and ADC

noise on receiver dynamic range and noise figure is important and needs to be considered for optimal ultrasound-receiver sensitivity. The MAX2037 VGA optimizes and properly balances output-referred noise and maximum gain to ensure compatibility with 12-bit ADCs like the MAX1437 in order to achieve the best possible ultrasound-receiver performance.

Appendix A—Phased-Array Ultrasound System Basics

High-Level Phased-Array Ultrasound System Block Diagram

Figure 5 shows a block diagram of a typical phased-array medical ultrasound imaging system. Systems using a phased-array approach like this require anywhere from 64 to 256 receive channels and a comparable number of transmit channels. In the **Figure 5** block diagram, a single transmit-and-receive channel is shown for simplicity.

Ultrasound Transmit Basics

To produce an ultrasound image, a phased-array ultrasound system must produce N (where N = number of transmit channels) properly delayed, high-voltage

transmit pulses. These pulses are used to excite the individual elements of a transducer array to produce a focused acoustic transmission (**Figure 6**).

Ultrasound Receiver Basics

Acoustic energy reflected from acoustic impedance discontinuities in the body are received by the transducer and routed to separate receive channels in the system. These receive channels amplify and then digitize the signals from each transducer element, as shown in **Figure 7**. Using a calculated delay profile, the digitized signals are delayed and summed in the ultrasound system's digital beamformer in order to generate a focused, receive beamformed signal. The resulting digital signal is used to generate 2D and PW/color-flow Doppler information.

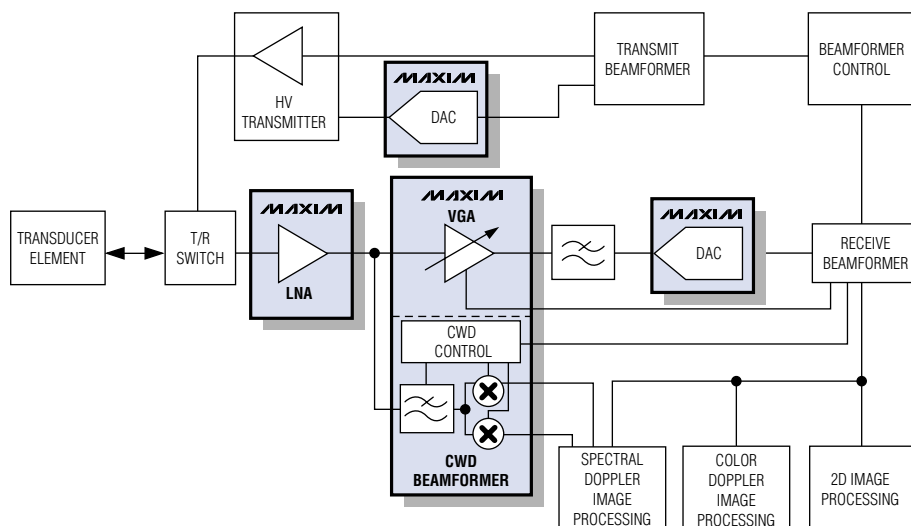


Figure 5. A single transmit-and-receive channel is shown for a typical phased-array medical ultrasound imaging system.

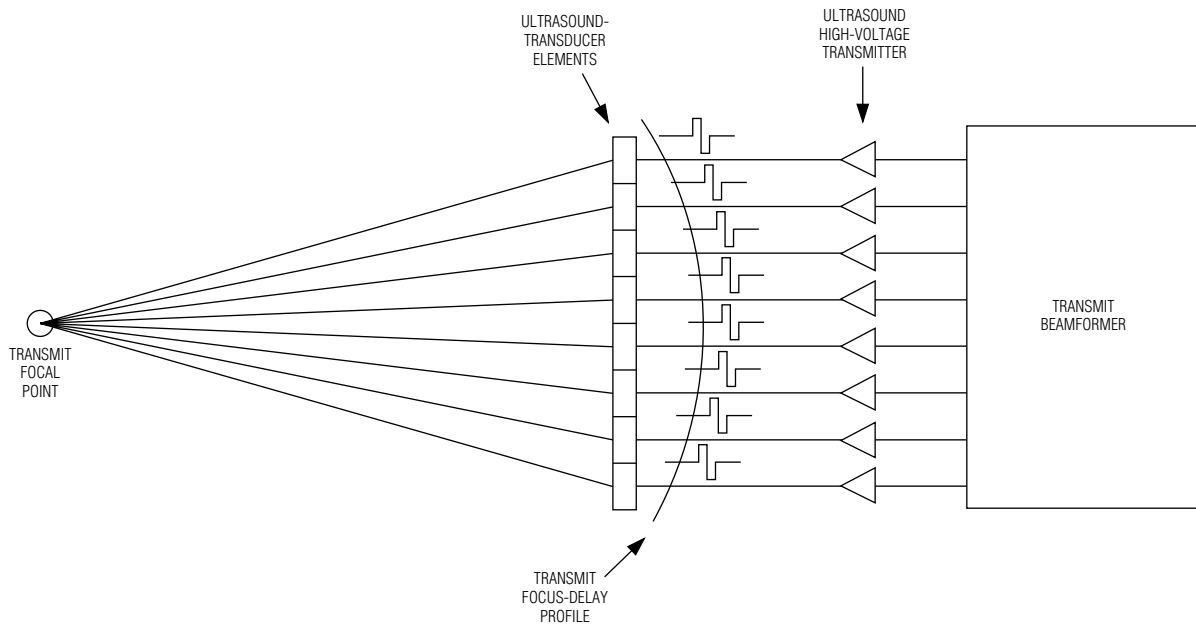


Figure 6. A focused acoustic transmission is produced by properly delayed, high-voltage transmit pulses.

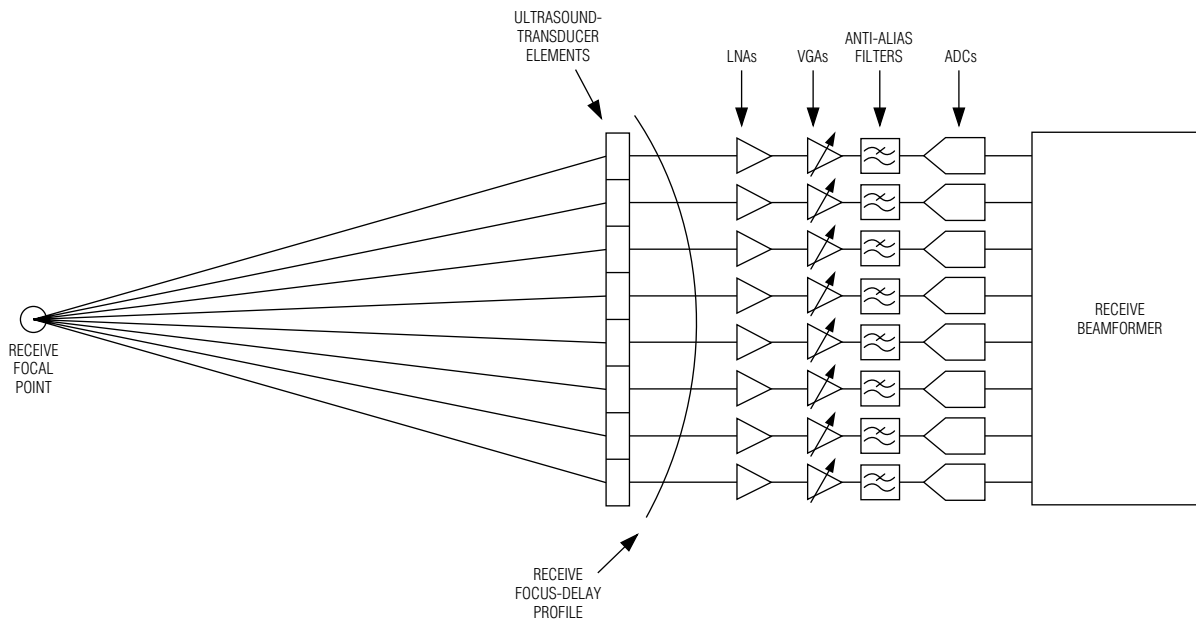


Figure 7. Signals from each transducer element are amplified and digitized by receive channels in the ultrasound-receiver system.

Robust, Fail-Safe Biasing Circuit for AC-Coupled Multidrop LVDS Bus

LVDS signaling is used widely in high-speed digital-signal interconnections, especially in digital video and camera signals. One of the popular bus topologies, the multidrop LVDS bus, connects multiple LVDS receivers to a 100Ω differential twisted pair driven by an LVDS transmitter. This bus structure is a convenient way to form a multiplex for LVDS signal routing. Additionally, more LVDS interconnections are using AC coupling to avoid ground-level shift and common-mode interference.

Figure 1 shows the block diagram of a typical multidrop LVDS bus. The connection length between the bus and the receiver inputs should be as short as possible. The fail-safe biasing circuit shown in Figure 1 provides a common-mode bias around 1.2V. When the bus is not driven by the Tx, or the bus has no state transition for a long time, the circuit also sets a small, 50mV to 100mV differential voltage to drive the LVDS receiver output to a determined logic state. For a general discussion of LVDS fail-safe circuits, refer to Application Note 3662, *Understanding LVDS Fail-Safe Circuits*, at www.maxim-ic.com/AN3662.

There is a significant difference in the biasing between the multidrop bus and a point-to-point connection: the receivers in a multidrop bus must be high impedance, as compared to the point-to-point connection in which the receiver's input

impedance must match the 100Ω impedance of the differential link. The variations of the resistor values are, therefore, a common weakness in the traditional fail-safe biasing circuit. This application note examines that traditional fail-safe circuit design, discusses the problem of component variations, and proposes a new robust biasing circuit.

Traditional Biasing Circuit and Its Weakness

The most common, traditional fail-safe biasing circuit consists of two resistor voltage-dividers at the two LVDS input pins. The implementation is depicted in **Figure 2a**. The resistor values are chosen so the voltages at both input pins are around 1.2V and the voltage difference of the two input pins is -50mV. The voltages at these two input pins are calculated under the nominal resistor values marked in Figure 2a. When the bus is not driven, this voltage difference will make the receiver output to be logic-low.

If, however, one considers resistor tolerance, the value of the differential voltage can change significantly. Assuming the use of all 1%-tolerant resistors, **Figure 2b** shows that the voltage difference can reach -90mV, a worst-case negative variation. Alternatively, at the opposite extreme, **Figure 2c** shows that the voltage difference can be as low as -16mV. Consequently, with a $\pm 1\%$ resistance change, the fail-safe differential input could change from -80% to +68%.

A large differential fail-safe voltage is a notable weakness of this traditional circuit design. The large voltage difference causes several reactions: the duty cycle for logic-high or low becomes unbalanced; the triggering threshold moves up at one side of the input and reduces the slow rate at the triggering point, thus causing the receiver's intrinsic jitter to increase. As Figure 2c illustrates, moreover, the low value of the voltage difference might not be enough to activate the fail-safe function.

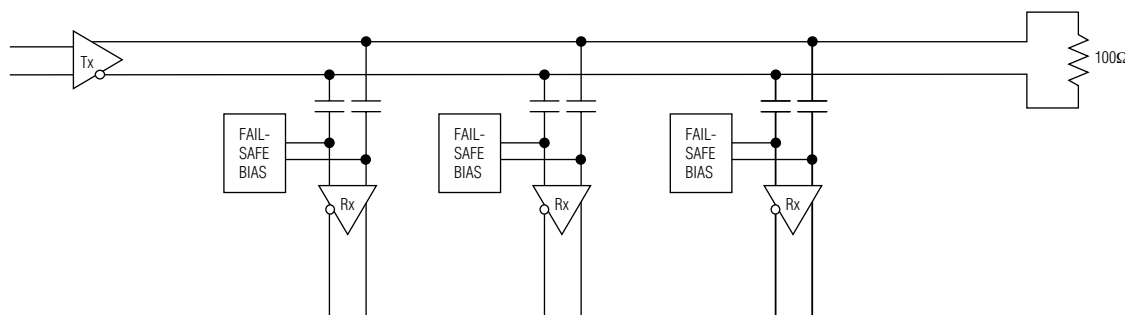


Figure 1. Short connections should be used between the bus and receiver inputs of an AC-coupled, LVDS multidrop bus.

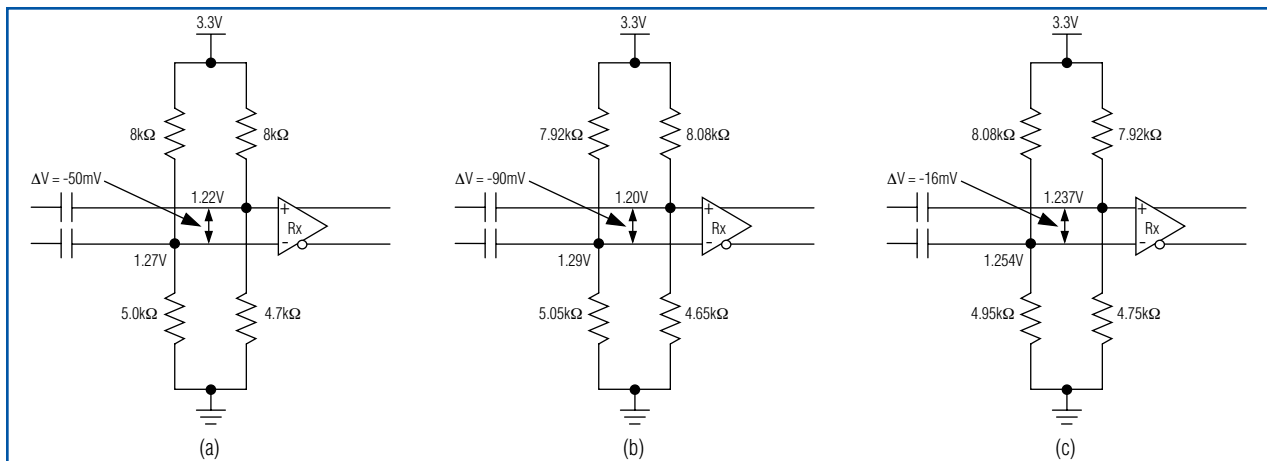


Figure 2. Commonly used fail-safe biasing circuit is shown (a) with nominal resistor values, (b) in a design that produces the greatest voltage differences at $\pm 1\%$ tolerance, and (c) in a design that produces the smallest voltage differences at $\pm 1\%$ tolerance.

To overcome the mentioned weaknesses in the traditional biasing circuit, consider the following new biasing circuit that is very robust against resistor variations.

New Fail-Safe Biasing Circuit

A new topology for a fail-safe biasing circuit generates a relatively constant differential voltage regardless of the resistor variation. **Figure 3** diagrams the new circuit.

In the new circuit, the common-mode voltage is supplied to the two input pins from a common source. The differential voltage is generated by a pulldown (or pullup) resistor on one input pin. From the values shown in Figure 3, we see that even with $\pm 5\%$ resistors, the fail-safe differential voltage only changes between -15% to $+15\%$, which is far more robust than the circuit shown in Figure 2. This new circuit can be used for LVDS products that have an internal common pullup fail-safe circuit, such as the MAX9169/MAX9170 and MAX9174/MAX9175, or

circuits that have a weak internal common-mode biasing, like the MAX9242/MAX9244/MAX9246/MAX9254, MAX9218, and MAX9248 deserializer products.

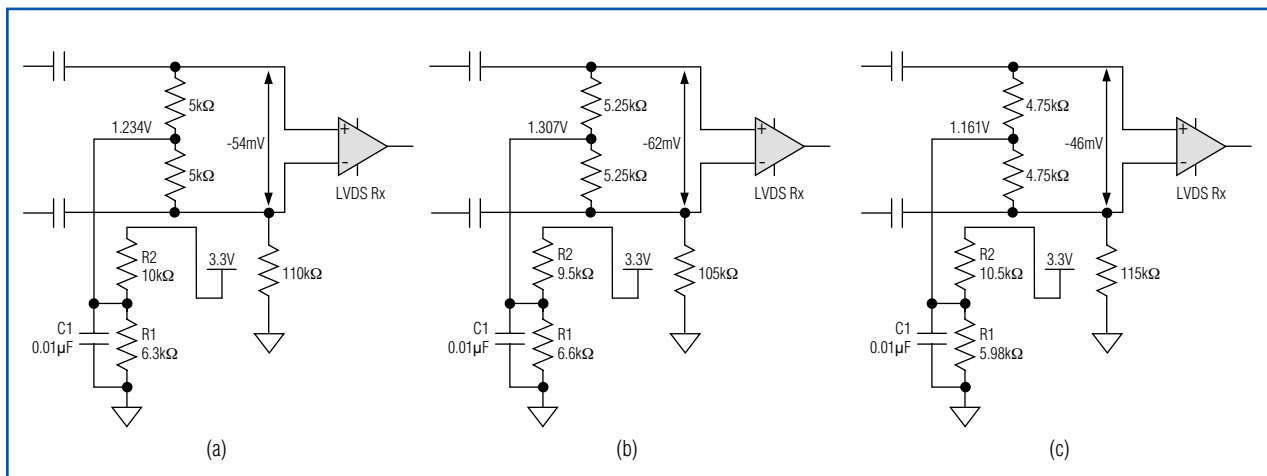


Figure 3. A robust fail-safe biasing circuit is shown (a) with nominal resistor values, (b) in a design that produces the greatest voltage differences at $\pm 5\%$ tolerance, and (c) in a design that produces the smallest voltage differences at $\pm 5\%$ tolerance.

Regain Location Information by Leveraging the 1-Wire Chain Function

A Simple Signaling and Protocol Method Determines Device Physical Location

A common characteristic of digital bus systems is sharing. Parallel bus systems, having become commonplace with the introduction of microprocessors, share data and address lines with all components connected to the bus. Chip-select signals are decoded from address lines and control signals. Through hardware design and wiring, the physical location of each component connected to the bus was always known. As technology evolved towards lower cost serial bus systems,¹ the address lines were sacrificed first. The chip-select function remained with SPI™ and MICROWIRE™ serial buses. More advanced serial bus systems introduced protocol-based addressing, in which address information is transmitted as a preamble to the data. A prominent example of such buses is the I²C/SMBus™, where the communication interface is reduced to a data and clock line. To achieve additional cost savings, the clocking information can be embedded in the data stream. Representatives of this category are 1-Wire®, LIN, and SensorPath buses.

As a consequence of protocol-based addressing, the knowledge of the physical location of a component is lost. This is a problem if the serial bus is used for instrumentation or control purposes (e.g., to measure temperature at multiple locations). Address pins that, in the case of the I²C bus, are tied to logic 1, logic 0, SCL, or SDA can mitigate the problem. This way, a single pin can define four different digital states, equivalent to two bits. Although simple and efficient, this approach has its limit as the original I²C protocol provides only seven address bits. The 1-Wire bus, with its 64-bit address, allows more flexibility in this respect. However, each address pin increases cost and, therefore, is not a welcome addition.

A simple, low-cost mechanism to regain the physical location information for a serial bus with multiple attached devices marks one location as the beginning of the network (location #1) and then identifies subsequent devices in the

SPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

SMBus is a trademark of Intel Corp.

1-Wire is a registered trademark of Dallas Semiconductor Corp. Dallas Semiconductor is a wholly owned subsidiary of Maxim Integrated Products, Inc.

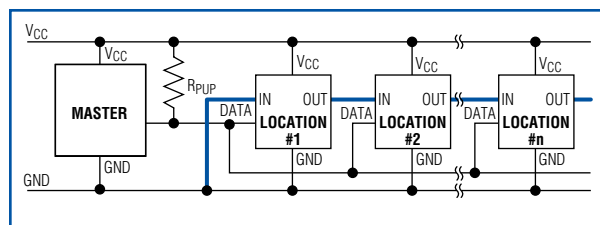


Figure 1. A serial network is enhanced for location detection.

connection, as in **Figure 1**. The connections that constitute this mechanism are shown as thick, blue lines. At the first location, the line is simply tied to ground.

Aside from the two pins labeled IN and OUT in Figure 1, on-chip logic is required to read the IN pin and to write to the OUT pin. With the help of these resources, the master can identify the first device, then the next device, and so on until all devices and their locations relative to each other are identified, provided that the protocol supports a network inventory function. A serial bus system that meets this requirement is the 1-Wire bus.

The 1-Wire bus is a simple signaling scheme that performs half-duplex bidirectional communications between a host/master controller and one or more slaves sharing a common data line (**Figure 2**). Both power and data communication for slave devices are transmitted over this single 1-Wire line. For power delivery, slaves capture charge on an internal capacitor when the line is in a high state, and then use this charge for device operation when the line is low during data transmission. A typical 1-Wire master consists of an open-drain I/O port pin with a resistor pullup to a 3V to 5V supply. This clever communication scheme also allows you to add memory, authentication, and mixed-signal functions at any time, easily and efficiently.

An important, fundamental feature in every 1-Wire system is that each slave device has a unique, unalterable read-only memory (ROM), 64-bit, factory-lasered serial number (ID) that will never be repeated in another device. Besides providing a unique electronic ID to the end product, this 64-bit ROM ID allows the master device to select a slave device among the many that can be connected to the same bus wire. Also part of the 64-bit ROM ID is an 8-bit family

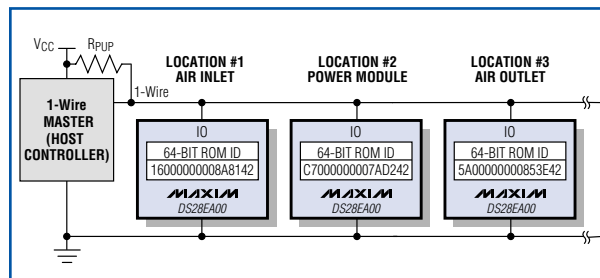


Figure 2. A typical 1-Wire network without the chain function is shown.

code that identifies the device type and functionality supported.

Typically, when a system initially starts up, the 1-Wire master might not know the number of devices on the 1-Wire bus or their ROM IDs. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify all devices. Through the *Search ROM** function,² the master can determine the ROM IDs of devices on the bus. However, Search ROM results do not provide information on an individual device’s location. For example, for the ROM IDs shown in Figure 2, the devices are discovered in the sequence shown in **Table 1**.

Table 1. Device Discovery Sequence

Sequence	ROM ID (Hexadecimal)	Position in Network
1	C7000000007AD242	Location #2
2	5A00000000853E42	Location #3
3	16000000008A8142	Location #1

The Chain-Function Concept

Using the chain function to determine the device’s physical location in a 1-Wire networked environment is based on:

- System-level knowledge of the physical routing of the 1-Wire network, i.e., where the first, second, etc., device/node is physically located.
- Learning the sequence, first to last, in which devices (ROM IDs) are physically connected.

Item a) is “by-design” system knowledge that comes from the physical layout of the 1-Wire network wiring. Item b) is typically the unknown set of information, which is easily discovered using the chain-function communication. This chain function (**Figure 3**) uses two pins, an input ($\overline{\text{EN}}$) to enable a device to respond during the discovery, and an output ($\overline{\text{DONE}}$) to inform the next device in the chain that the discovery of the previous device is done. The $\overline{\text{DONE}}$ signal connects to the $\overline{\text{EN}}$ input of the next device. The $\overline{\text{EN}}$ input of the first device in the chain is hardwired to GND. The connections to operate the chain function are shown as thick, blue lines. Aside from the $\overline{\text{EN}}$ and $\overline{\text{DONE}}$ pins, sequence discovery requires a new network function command, *Conditional Read ROM*. This command reports a device’s ROM ID only if certain conditions (explained below) are met. *Read ROM*, in contrast, causes all devices in a network to transmit their ROM IDs at the same time. The DS28EA00 is the first device to implement and support this new chain function (as shown in Figure 3).

Besides their use in sequence discovery, the $\overline{\text{EN}}$ and $\overline{\text{DONE}}$ pins can serve as digital PIOs. To achieve this coexistence,

*Commands and states are capitalized for clarity (and the first instance is italicized).

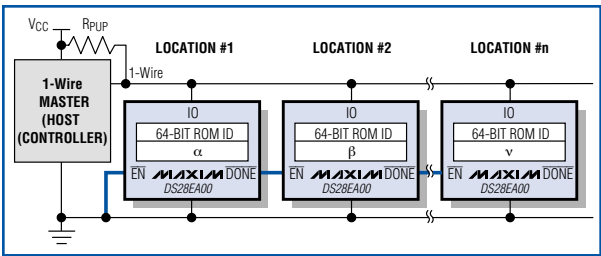


Figure 3. The DS28EA00 is shown in a typical 1-Wire network employing the chain function.

the chain function defines three chain states, *OFF*, *ON*, and *DONE*. The transition from one chain state to another is controlled through the new *Chain* command. **Table 2** summarizes the chain states and their associated behaviors.

Table 2. Chain States

Chain State	Device Behavior		
	$\overline{\text{EN}}$ (PIOB)	$\overline{\text{DONE}}$ (PIOA)	Conditional Read ROM
OFF (default)	PIO (high impedance)	PIO (high impedance)	Ignored
ON	$\overline{\text{EN}}$ input	Pullup on	Recognized if $\overline{\text{EN}}$ is logic 0
DONE	No function	Pulldown on ($\overline{\text{DONE}}$ is logic 0)	Ignored

The power-on default chain state is OFF, where $\overline{\text{DONE}}$ (PIOA) and $\overline{\text{EN}}$ (PIOB) are solely controlled through separate *PIO Access Read* and *Write* commands, as described in the DS28EA00 data sheet.³ In the Chain ON state, $\overline{\text{DONE}}$ is pulled high to the device’s internal V_{DD} supply through an on-chip ~40kΩ resistor (R_{CO}), thus applying a logic 1 to the $\overline{\text{EN}}$ pin of the next device. The Conditional Read ROM command is recognized only in the Chain ON state, provided that $\overline{\text{EN}}$ is at logic 0. This condition is met by a maximum of one device in the network during the sequence-discovery procedure.

To transition a device from the Chain OFF to the Chain ON or Chain DONE state, the master uses the Chain command. **Figure 4** shows the possible transitions. After the Chain command code, the master must send a suitable *Chain Control* byte. To minimize the possibility of receiving an erroneous Chain command, this control byte is first transmitted in its true form, and then in its inverted form. As a feedback for a successful state change, the master receives AAh confirmation bytes.

To begin a sequence discovery, the master must put all devices into the Chain ON state. After a device’s ROM ID

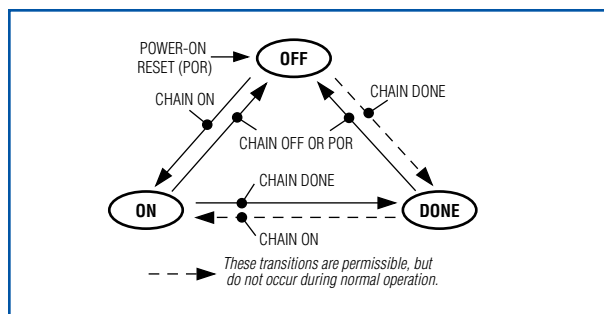


Figure 4. This diagram illustrates transitions between chain states.

is read through Conditional Read ROM, the master puts the device into the Chain DONE state, which enables the next device in the Chain to respond to the Conditional Read ROM command. As the sequence discovery progresses, devices are sequentially transitioned into the Chain DONE state until all devices are identified. Finally, all devices are put into the Chain OFF state, which releases the \overline{EN} and \overline{DONE} pins to become PIOs and restores their power-on default state.

Sequence Discovery Example

Precondition A master controls a network as shown in Figure 3. All devices support the chain function. To discover the sequence of devices in the chain, i.e., the number of locations and for each location the device's ROM ID (also known as the Registration Number), the master performs the following procedure.

Initialization The master issues a *Skip ROM* command followed by a Chain ON command, which puts all devices in the Chain ON state. The pullup of the \overline{DONE} pin through R_{CO} changes the $\overline{DONE}/\overline{EN}$ connections to logic 1 at all devices except for the first device in the chain.

First Cycle The master sends a Conditional Read ROM command, which causes the first device in the chain to respond with its 64-bit ROM ID. The master memorizes the ROM ID and the fact that this is the first device in the chain. Next, the master transmits a Chain DONE command. Passed through the \overline{DONE} pin of device #1, this command asserts logic 0 at the \overline{EN} pin of the second device in the chain and also prevents device #1 from responding again.

Second Cycle The master sends a Conditional Read ROM command. Because device #2 is now the only device in the chain with a logic 0 at \overline{EN} , it responds with its ROM ID, which is stored by the master with the sequence number '2'. (Device #1 cannot respond to the command, as it is in Chain DONE state.) Next, the master transmits a Chain DONE command.

Additional Cycles To identify the ROM IDs of the remaining devices and their physical sequence, the master repeats the steps of Conditional Read ROM and

Chain DONE. If there is no response to the Conditional Read ROM command, all devices in the chain have been identified.

Ending At the end of the discovery process, all devices in the chain are in the Chain DONE state. The master ends the sequence discovery by issuing a Skip ROM command followed by a Chain OFF command. This puts all the devices into the Chain OFF state, and transfers control of the PIO pins to the *PIO Access Function* commands (e.g., to blink a LED). For the full description of the Conditional Read ROM and the Chain command and flow charts, refer to the DS28EA00 data sheet.⁴

Assuming a standard 1-Wire speed (960 μ s for a reset/presence detect cycle and 65 μ s per time slot), the initialization and ending combined take ~7ms (one-time overhead). The discovery and location detection takes ~7.7ms per device. Under the same conditions, Search ROM takes ~14ms per device. Within 100ms, for example, one could identify and locate 12 devices with the chain function, but only identify 7 devices if relying solely on the Search ROM function.

Additional Aspects

Cable Capacitance Category 5 phone cables, which are commonly used to build 1-Wire networks, have a capacitance of approximately 50pF/m between the wires of a twisted pair. Depending on the size of the network, this can add a significant load on the line when putting all devices into the Chain ON state. Active pullup of the 1-Wire line may be necessary when in parasite-power mode to prevent the voltage from dropping below the permissible minimum value. This precaution is not needed with central or local V_{CC} power supply.

Conditional Read ROM The DS2401 also understands this command code as Read ROM for compatibility with the DS2400 Silicon Serial Number, which was discontinued in 1993. For this reason, do not connect any DS2401 to a network that uses the chain function. Therefore, when using a 1-Wire port adapter, select one that does not include the DS2401. The DS2405 revision A also responds to the Conditional Read ROM command code like a DS2401. The DS2405 revision B, in production since 1998, ignores the Conditional Read ROM command code.

1-Wire Master Circuits For the embedded environment, a variety of low-cost, discrete and IC-based 1-Wire masters can be implemented. Discrete solutions range from a resistor pullup to a spare μ C port pin or advanced drivers.⁵ Integrated drivers optimized to drive 1-Wire lines include the DS2480B⁶ (serial port, UART), the DS2490⁷ (USB port), and the DS2482^{8,9} (I²C port, **Figure 5**). The 8-channel version of the DS2482 has three address pins, which allow a single host controller to operate up to 64

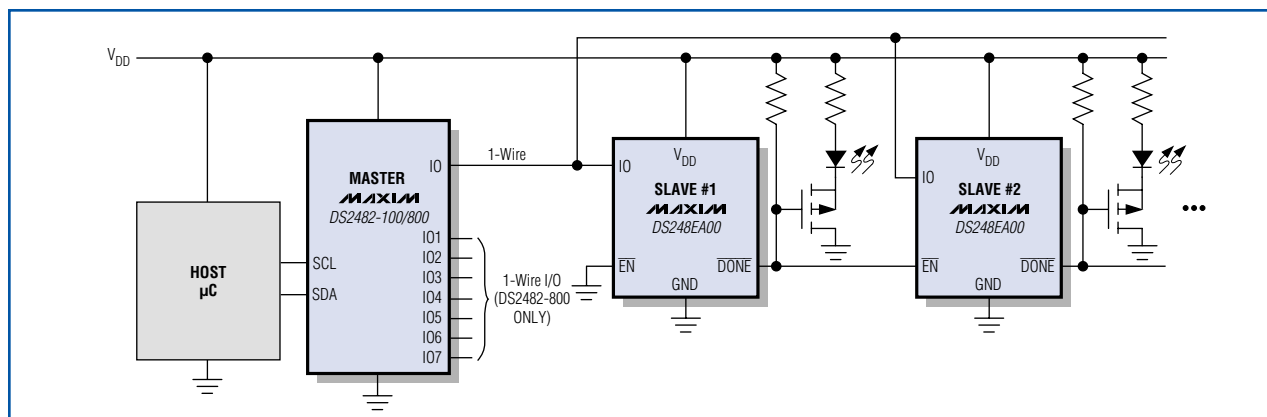


Figure 5. The DS2482 single-channel, I²C-to-1-Wire bridge device is used as a 1-Wire master. The \overline{DONE} output is also used to drive an LED, which does not affect the chain function.

separate 1-Wire networks. Application Note 192, *Using the DS2480B Serial 1-Wire Line Driver*,¹⁰ explains the DS2480B from the software developer's point of view. A similar document is also available for the DS2482 driver.¹¹

Power Supply If V_{CC} power is available, all DS28EA00s can perform a temperature conversion simultaneously. A subsequent *Conditional Search* command can be issued to identify only those devices that report an alarming temperature. The device's ROM ID, in conjunction with its location determined from the sequence discovery, quickly tells where corrective action is required. Without V_{CC} power, temperature conversions must occur sequentially. In addition, one must ensure that the voltage on the 1-Wire data line does not drop too far at the beginning of the sequence discovery (when all devices transition from Chain OFF to Chain ON).

Speed The fast timing of overdrive speed is not suited to operate a 1-Wire network that contains multiple devices or extends over ~3m; standard speed should be used instead. Depending on the number of devices in the network, particularly if using a parasitic power supply, extended recovery time is required, even if using standard speed.¹²

Troubleshooting If the sequence detection does not work as expected, look for a voltage drop on the 1-Wire line after issuing the Chain ON command. If the voltage dips below 3.0V, there is a risk that the command was not executed properly. To prevent such a drop, either use a 1-Wire driver circuit with active pullup after Chain ON, or use a central power supply. The sequence detection will also fail if the first device in the chain has its \overline{EN} input open, \overline{EN} tied to the 1-Wire line, or \overline{EN} tied to V_{CC} . Make sure that the network does not contain a DS2401. Connecting two or more networks in parallel to the same 1-Wire port is not permissible as all "first devices" will respond simultaneously, resulting in a ROM ID with an invalid CRC byte.

Conclusion

The chain function is a new feature that allows the master to determine the physical sequence of devices in a linear network under software control, without human intervention. The DS28EA00 1-Wire digital thermometer is the first device to integrate this chain function. Compared to concepts that derive device location data from address pins, the DS28EA00 is the most cost-effective choice for multipoint temperature-measurement applications.

References

1. Application Note 3967: *Selecting a Serial Bus*, www.maxim-ic.com/AN3967
2. Application Note 187: *1-Wire Search Algorithm*, www.maxim-ic.com/AN187
3. DS28EA00 data sheet, www.maxim-ic.com/DS28EA00
4. *Ibid.*
5. Application Note 244: *Advanced 1-Wire Network Driver*, www.maxim-ic.com/AN244
6. DS2480B data sheet, www.maxim-ic.com/DS2480B
7. DS2490 data sheet, www.maxim-ic.com/DS2490
8. DS2482-100 data sheet, www.maxim-ic.com/DS2482-100
9. DS2482-800 data sheet, www.maxim-ic.com/DS2482-800
10. Application Note 192: *Using the DS2480B Serial 1-Wire Line Driver*, www.maxim-ic.com/AN192
11. Application Note 3684: *How to Use the DS2482 I²C 1-Wire Master*, www.maxim-ic.com/AN3684
12. Application Note 3829: *Determining the Recovery Time for Multiple-Slave 1-Wire Networks*, www.maxim-ic.com/AN3829