Online Simulator Validates Buck Converter Output Error Budget Analysis

Introduction

We need to perform an output voltage error budget analysis for one of our buck converter designs. The biggest contributor to the error is the output droop consequent to the load step. Having tried different methods to estimate the droop has led to different results. How do we make sense of it? In this article, we perform a buck converter output error budget analysis. In estimating the droop amplitude, we compare a simulated result with two different back-of-the-envelope estimates and reconcile the different approaches.

The Error Budget

For this calculation, the buck converter parameters of interest are:

V_{IN} = 5V, V_{OUT} = 3.3V

V_{OUT} DC accuracy ±2% = ±66mV

The other defining elements of the buck converter are:

Clock frequency = 695kHz

L = 2.7µH, C = 2 x 22µF

The design for this buck converter is created with the online EE-Sim® DC-DC Converter Design Tool. Simulation results provided by this tool indicate the following:

V_{OUT} ripple = 2.6mV_{P-P} or ≈ ±1.3mV (Figure 1)

V_{OUT} transient droop from 1A to 2A = 157mV (Figure 2)

Accordingly, the estimated worse-case error budget (negative deviation of the output voltage) is:

V_{ERROR} = 66 + 157 + 1.3 = 224.3mV

The given target error budget is 240mV against an estimated error of 224.3mV. All is well, but why is the result not in line with our back-of-the-envelope calculations?

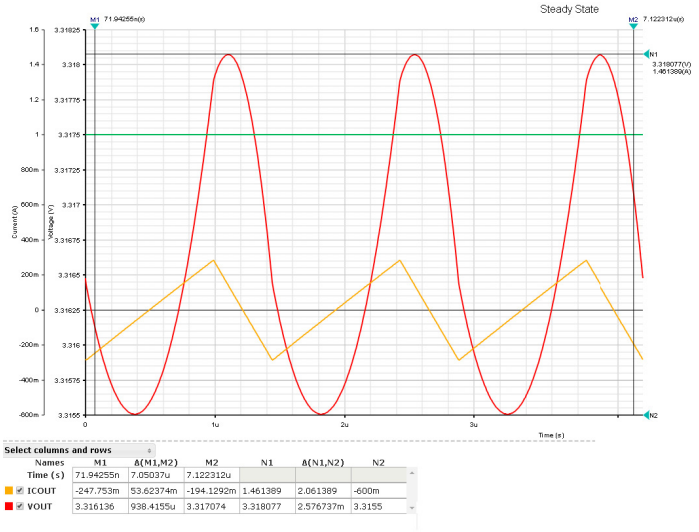

Figure 1. Output Voltage Ripple (Red) and Capacitor Current (Yellow)

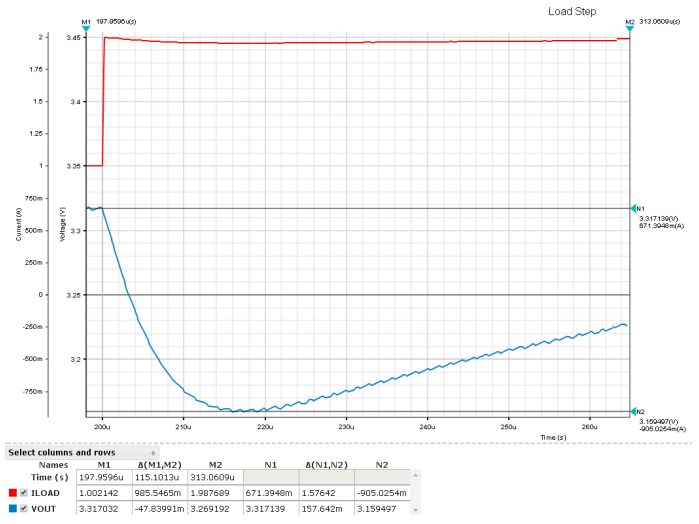

Figure 2. Load Step (Red) and Response (Blue)

CdV/dt Back-of-the-Envelope Estimate

A formula often used for this calculation is:

$$V_{droop} = \frac{I}{2\pi \times f_{BW} \times C} \quad (1)$$

Where I is the load step (1A), C is the output capacitor (2 x 22µF), and f_{BW} is the regulator closed-loop bandwidth. For the closed-loop bandwidth, f_{BW}, one can take a fraction of the clock frequency as a set value. In figure 3, we have the luxury of an online simulation (18.8kHz).

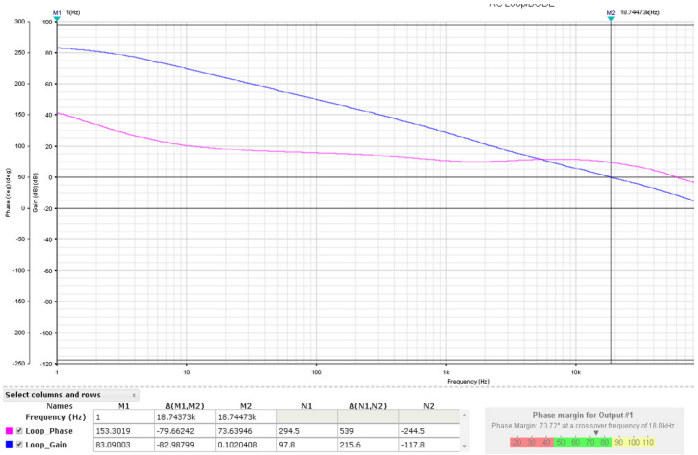

Figure 3. Closed-Loop Bandwidth (Blue) and Phase Margin (Purple)

The rationale for this formula is that if the load step is steep the capacitors takes all the hit, linearly discharging according to the law:

$$\frac{V_{droop}}{\tau} = \frac{I}{C} \quad (2)$$

Where τ is the discharge time. The capacitor's discharge lasts until the loop responds after a delay proportional to the inverse of the closed-loop bandwidth, f_{BW}:

$$\tau = \frac{1}{2\pi f_{BW}} \quad (3)$$

By substitution of equation (3) into equation (2), we get equation (1). With this formula, the estimated droop is:

$$V_{droop} = \frac{1}{2\pi \times 18.8k \times 44.6\mu} = 190mV$$

Note that an unusual capacitance value, 44.6µF, is used. This is because high-density ceramic capacitors have capacitance that can vary dramatically with applied voltage. We use the actual capacitance with a bias of V_{OUT} (3.3V) based on data provided by the device manufacturer and used by the EE-Sim design tool. This leads to a total error of:

$$V_{ERROR} = 66 + 190 + 1.3 = 257.3mV$$

257.3mV is above the 240mV budget. This is the estimate we are concerned with. At first, the rationale for the formula appears to be sound, but what is wrong with it?

LC Resonant Back-of-the-Envelope Estimate

The first thing we notice is that the formula completely neglects the presence of the inductor (2.7µH). During the time the loop is unresponsive, the output is essentially an LC resonant circuit as shown in Figure 4 (a SIMPLIS® simulation).

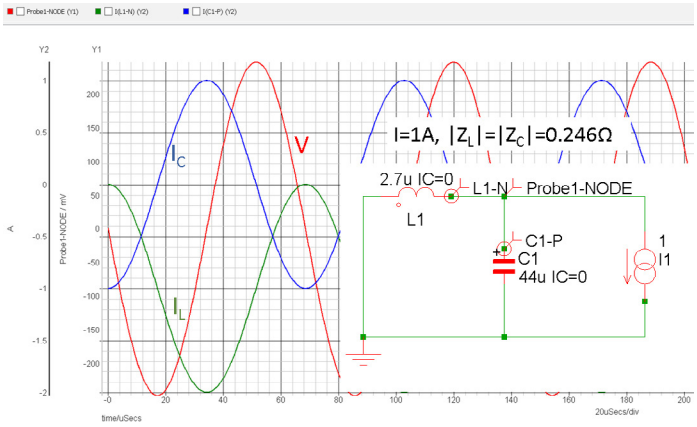

Figure 4. LC Resonant Response to Current Step

In this case, the circuit tends to develop an oscillation of amplitude:

$$v = ZI \sin 2\pi \times f_{RES} \times t$$

Where t is time, I is the 1A load step and:

$$Z = \sqrt{L/C} = \sqrt{\frac{2.7}{44.6}} = 0.246\Omega$$

$$ZI = 0.246 \times 1 = 246mV$$

$$f_{RES} = \frac{1}{2\pi\sqrt{LC}} = \frac{1000}{2\pi\sqrt{2.7 \times 44.6}} \; k = 14.5kHz$$

Naturally, this oscillation unfolds only until the loop responds after a delay time τ given by equation (3). Accordingly, the sinusoid will stop at:

$$v(t) = V_{droop} = ZI \sin\left(2\pi \times f_{RES} \; \frac{1}{2\pi f_{BW}}\right) =$$

$$ZI \sin\left(\frac{f_{RES}}{f_{BW}}\right) = 246mV \times \sin\left(\frac{14.5}{18.8}\right) =$$

$$246mV \times 0.697 = 171mV$$

With the inductor back in the picture, the estimated droop value is 171mV, much closer to the simulated 157mV. With a 171mV droop estimate, the error is 238.3mV, still within the 240mV budget.

Reconciliation

Short of simulating it or building the circuit and exercising it with a current load step generator, we can find the first-order estimate of the droop amplitude with two formulas, one for the linearized droop model:

$$V_{droopC} = \frac{1}{2\pi \times f_{BW} \times C}$$

and another with the resonant model:

$$V_{droopLC} = ZI \sin\left(\frac{f_{RES}}{f_{BW}}\right)$$

Which one should be used in lieu of a full-fledged simulation or breadboard construction? As often is the case, it depends. If $f_{RES} << f_{BW}$, then by using the approximation $\sin x \approx x$ in $V_{droopLC}$, we have:

$$V_{droopLC} \approx ZI \frac{f_{RES}}{f_{BW}}$$

And by substituting Z and f_{RES} with their expressions, we have:

$$V_{droopLC} \approx I \sqrt{L/C} \ \frac{1}{2\pi\sqrt{LC}} \ \frac{1}{f_{BW}} = \frac{I}{2\pi \times f_{BW} \times C}$$

For $f_{RES} << f_{BW}$, either expression works. Figure 5 shows the difference between the two approaches and the linearization error.

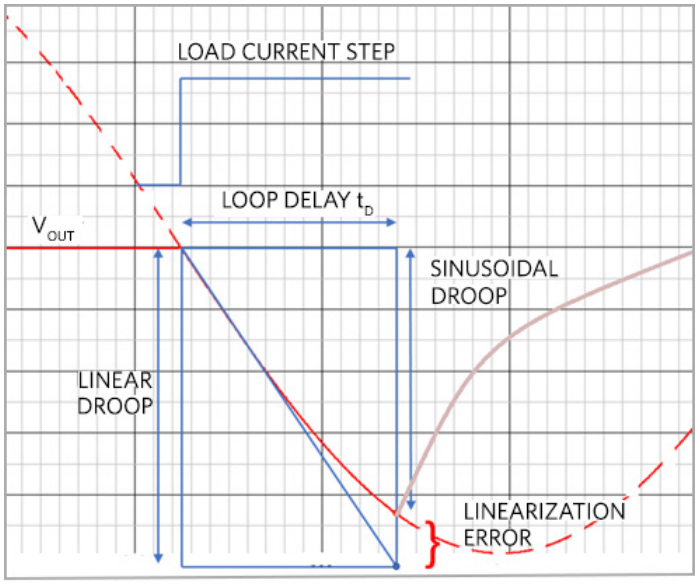

Figure 5. LC Resonant vs. Linear Models

The Simulation Advantage

The EE-Sim design tool uses SIMPLIS to simulate the performance of a circuit. SIMPLIS was developed and optimized for simulating switching circuits like DC-DC converters. Unlike our simple back-of-the-envelope calculations, a simulation takes into account all the factors of the circuit, or at least those that are in the component models. Naturally, our hand calculations are crude estimates with simplified equations that do not include all the effects of the circuit and neglect the component parasitics (e.g., ESR, etc.). Hence, the simulation provides the most accurate results.

Conclusion

We performed an output voltage error budget analysis for the MAX17242 buck converter design. We simulated the ripple and load step voltage droop amplitude contributions to the error using the EE-Sim online DC-DC tool. Our initial hand calculations of the voltage droop appeared to be pessimistic compared to the simulations. We reviewed our assumptions and developed a more accurate back-of-the-envelope approach to the step-response calculation. The result from this approach came much closer to the simulated result. This, and more importantly the simulation result, eased our initial concerns about the ability to meet the error budget.

Glossary

Buck: Step-down voltage regulator

EE-Sim: EE-Sim DC-DC Converter Tool, part of the EE-Sim Design and Simulation Environment, which uses design requirements to quickly create a complete power design including a schematic, BOM, and simulation waveforms.

EMI: Electromagnetic interference

SIMPLIS: Simulation of Piecewise LInear Systems is a time-domain circuit simulator specifically designed to handle the simulation challenges of switching power systems.

Learn more:

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MAX17242 3.5V–36V, 2A, Synchronous Buck Converter with 15µA Quiescent Current and Reduced EMI

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