LINEAR TECHNOLOGY

DESIGN NOTES

10Mbps Multiple Protocol Serial Chip Set: Net1 and Net2 Compliance by Design – Design Note 174

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Introduction

With the increase in multinational computer networks, comes the need for the network equipment to support different serial protocols. When the designer becomes occupied with the details of the interface specification, there is always the possibility that one small detail will be missed. This compliance headache causes designers to seek out a cost-effective, integrated solution.

The LTC®1543, LTC1544 and LTC1344A have taken the integrated approach to multiple protocol. By using this chip set, the Net1 and Net2 design work is done (see Figure 1). In fact, Detecon Inc. documents compliance in Test Report No. NET2/102201/97. With this chip set, network designers can concentrate on functions that increase the end product value rather than on standards compliance.

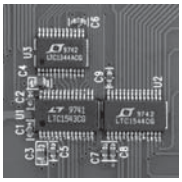

Figure 1. The LTC1543, LTC1544 and LTC1344A Multiple Protocol Serial Chip Set

Review of Interface Standards

The serial interface standards V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 specify the electrical characteristics of each signal, the connector type, the transmission rate and the data exchange protocols. In general, the U.S. standards start with RS or EIA and the equivalent European standards start with V or X. The single-ended standard, V.28 (RS232) has a lower data rate than the other differential standards. The current maximum RS232 data rate is 128kbps. As for the V.35, V.36, RS449, EIA-530, EIA-530A and X.21 standards, the maximum data rate is 10Mbps.

Typical Application

Like the LTC1343 software-selectable multiprotocol transceiver, the LTC1543 and LTC1544 use the LTC1344A for switching resistive termination. The main difference between these parts is the functional partition: the LTC1343 can be configured as a data/clock chip or a control-signal chip using the CTRL/CLK pin, whereas the LTC1543 is a dedicated data/clock chip and the LTC1544 is a control-signal chip.

Figure 2 shows a typical application using the LTC1543, LTC1544 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The chip set supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode. Shown here is a DCE mode connection to a DB-25 connector.

The mode select pins M0, M1 and M2 are used to select the interface protocol, as summarized in Table 1. There are internal 50µA pull-up current sources on the mode select pins, DCE/DTE and the INVERT pins. The protocol may be selected by plugging the appropriate interface cable into the connector. The mode pins can be routed to the connector and are unconnected (logic 1) or wired to ground (logic 0). If all the mode-select pins are not connected (logic 1), the chip set enters the no cable mode in which the chip set lowers the supply current to less than 700µA and three-states the driver and receiver outputs, and the LTC1344A disconnects the termination resistors.

Table 1. Mode Selection

Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
V.28/RS232	1	1	0
No Cable	1	1	1

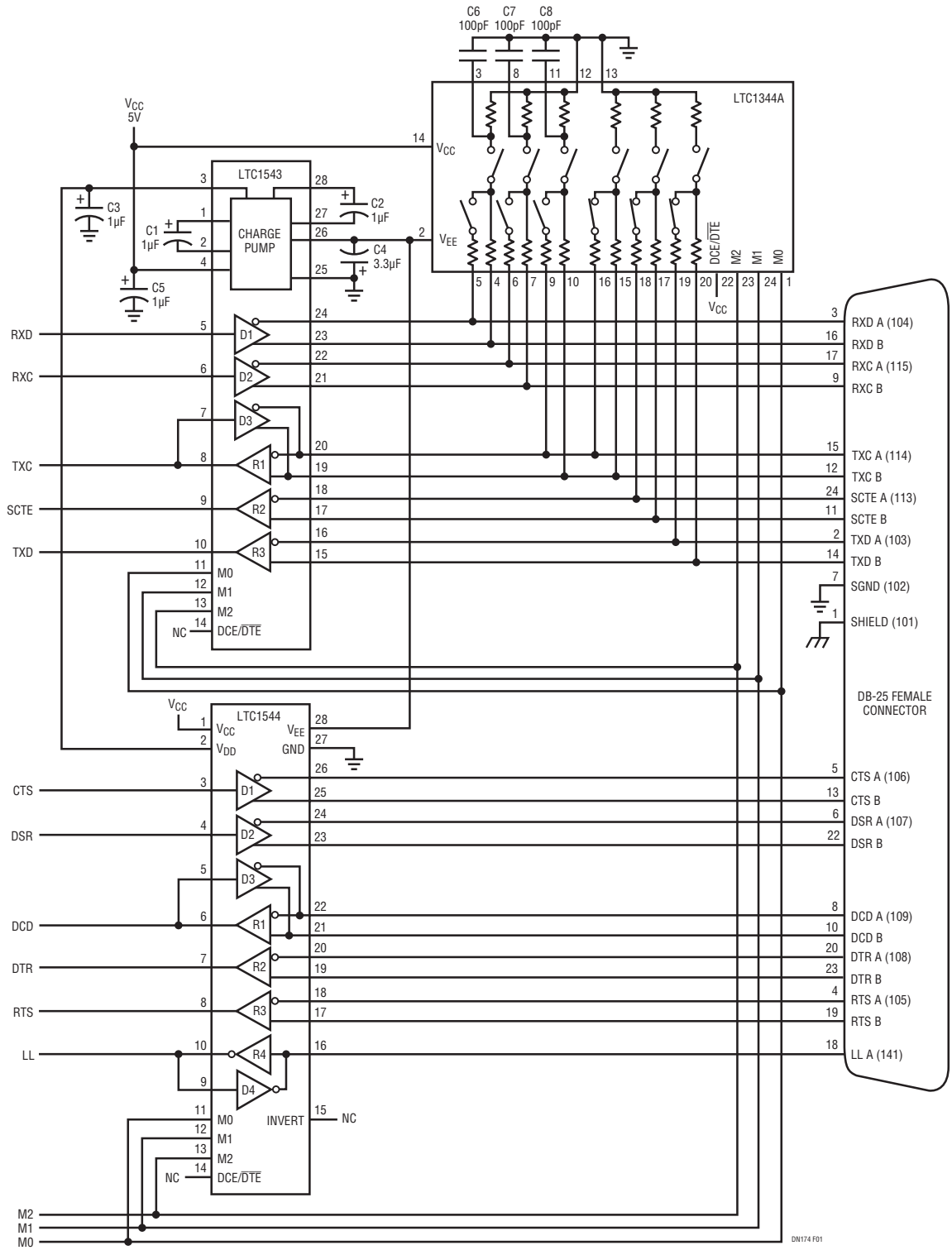

Figure 2. Controller-Selectable Multiple Protocol DCE Port with DB-25 Connector

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