Keywords: CLAD, clock rate adapter, clock, adapter

APPLICATION NOTE 3409

Configuration of CLAD for DS318x

Dec 21, 2004

Abstract: This application note describes how to configure the clock rate adapter (CLAD) functions in the DS3184. It also applies to other Maxim devices like the DS3181, DS3182 and DS3183. The DS3181, DS3182, DS3183, and DS3184 (DS318x) integrate ATM cell/HDLC packet processors with DS3/E3 framers and LIUs to map/demap ATM cells or packets into a maximum of four DS3/E3 physical copper lines with DS3-framed (C-bit or M23), E3-framed (G.751 or G.832), or clear-channel data streams on a per-port basis.

Introduction

This application note is an overview about configuring the clock rate adapter (CLAD) functions in the DS3184. The information here is applicable to other Maxim devices like the DS3181, DS3182 and DS3183. The DS318x (DS3181, DS3182, DS3183, and DS3184) integrate ATM cell/HDLC packet processors with DS3/E3 framers and LIUs to map/demap ATM cells or packets into a maximum of four DS3/E3 physical copper lines with DS3-framed (C-bit or M23), E3-framed (G.751 or G.832), or clear-channel data streams on a per-port basis.

The CLAD in the DS318x is used to create multiple internally-required DS3, E3 or STS-1 clock(s) from a single clock-reference input on the CLKA pin. The clock frequency applied to CLKA must be one of the following:

A. DS3 (44.736MHz)
B. E3 (34.368MHz)
C. STS-1 (51.84MHz)

Given one of these clocks, the other two clocks will be generated. The internally generated clocks can be driven on output pins CLKB and CLKC for external use, if needed.

Clad Functional Features

The CLAD of DS318x can generate the internally needed DS3 (44.736MHz), E3 (34.368MHz), and STS-1 (51.84MHz) clocks from a single input-reference clock. This input reference clock can be either 51.84MHz, 44.736MHz, or 34.368MHz. These internally derived clocks can be used as references for the LIU and jitter attenuator, and can be transmitted off-chip for external system use.

Configuring the Clad

If using the LIU of DS318x, the CLAD supplies the clock to the Receive LIU of DS318x. The CLAD of DS318x is configured by the CLAD bits in the GL.CR2 register. In this case, the user must supply a DS3, E3, or STS-1 clock to the CLKA pin.

The user must supply at least one of the three frequency rates (DS3, E3, STS-1) to the CLKA pin. The CLAD[3:0] bits inform the PLL of the frequency applied to the pins. **Figure 1** shows the CLAD block for the DS318x.

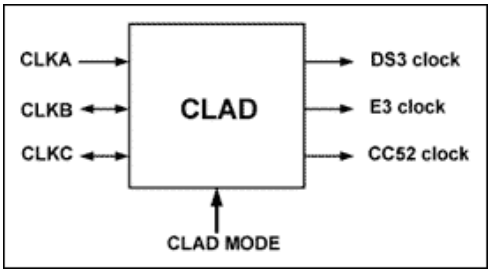

Figure 1. CLAD block for the DS318x.

Selection of the output clock of the CLAD applied to the LIU and to the transmitter is controlled by the FM bits (located in PORT.CR2). The CLAD provides maximum flexibility. The application may supply any of the three clock rates and use the CLAD to provide the clock rate required.

The CLAD can also be disabled and all three clocks supplied externally using the CLKA, CLKB, and CLKC pins as inputs. When the CLAD is disabled, the three reference clocks (DS3, E3 and STS-1) are applied to the CLKA, CLKB, and CLKC pins. If any of the three frequencies is not required, it need not be applied to the CLAD clock pins.

The CLAD MODE inputs to the CLAD are composed of CLAD[3:0] control bits (located in the GL.CR2 Register) which determine which pins are input and output and which clock rate is on which pin. Please see Table 1 for more details.

When CLAD[3:0] = 00XX, the PLL circuits are disabled and the signals on the input clock pins (CLKA, CLKB and CLKC) are used as the internal LIU reference clocks. When CLAD[3:0] = (01XX or 10XX or 11XX), none, one, or two PLL circuits are enabled to generate the required clocks as determined by the CLAD[3:0] bits, the framing mode (FM[5:0]), and the Line-Mode control bits (LM[2:0] located in PORT.CR2).

The line-mode bits select main port-interface operational modes. If a clock rate is not required on the CLAD output clock pins or for a reference clock for the LIU, then the PLL used to generate that clock is disabled and powered down.

The Clad Configuration Registers

The two registers required to configure the CLAD are described below.

Register Name: GL.CR2
Register Description: Global Control Register 2
Register Address: 004h

Bit #	15	14	13	12	11	10	9	8
Name	-	-	-	G8KRS2	G8KRS1	G8KRS0	G8K0S	G8KIS
Default	0	0	0	0	0	0	0	0
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	-	-	-	-	CLAD3	CLAD2	CLAD1	CLAD0
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: CLAD IO Mode [3:0] (CLAD[3:0])

These bits control the CLAD clock IO pins CLKA, CLKB, and CLKC. These register bits control which clock is used to recover the RX Clock from the line in the LIU. See **Table 1** for more details.

Table 1. CLAD IO Pin Decode			
GL.CR2 CLAD[3:0]	**CLKA PIN**	**CLKB PIN**	**CLKC PIN**
00 XX	DS3 clock input	E3 clock input	STS-1 clock input
01 00	DS3 clock input	Low output	Low output
01 01	DS3 clock input	E3 clock output	Low output
01 10	DS3 clock input	Low output	STS-1 clock output
01 11	DS3 clock input	STS-1 clock output	E3 clock output
10 00	E3 clock input	Low output	Low output
10 01	E3 clock input	DS3 clock output	Low output
10 10	E3 clock input	Low output	STS-1 clock output
10 11	E3 clock input	STS-1 clock output	DS3 clock output
11 00	STS-1 clock input	Low output	Low output
11 01	STS-1 clock input	E3 output	Low output
11 10	STS-1 clock input	Low output	DS3 clock output
11 11	STS-1 clock input	DS3 clock output	E3 clock output

The CLAD supplies a reference clock to the receive LIU. The receive LIU selects the clock frequency based on the mode the user selects through the framing mode (FM) bits. The FM bits select the main framing operational modes. The CLAD output is also available as a transmit clock source, if selected with the PORT.CR3.CLADC register bit.

Register Name: PORT.CR3
Register Description: Port Control Register 3
Register Address: (0, 2, 4, 6)44h

Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	-	-	RCLKS	RSOFOS	RPFPE	TCLKS	TSOFOS	TPFPE
Default	0	0	0	0	0	0	0	0
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	P8KRS1	P8KRS0	P8KREF	LOOPT	CLADC	RFTS	TFTS	TLTS
Default	0	0	0	0	0	0	0	0

Bit 3: CLAD Transmit Clock Source Control (CLADC)

This bit is used to enable the CLAD clocks as the source of the internal transmit clock. This bit's function is conditional on other control bits.

0 = Use CLAD clocks for the transmit clock as appropriate
1 = Do not use CLAD clocks for the transmit clock (if no loopback is enabled, TCLKIn is the source)

Conclusion

Maxim DS318x devices can be very useful for creating multiple clocks as LIU reference clocks or to transmit clocks for

the user's application. The decision of creating and transmitting multiple clocks should be made based on the designer's needs in their application board. For further questions on the operation of the CLAD on Maxim parts, please contact the Maxim Telecommunications applications support team.

Related Parts		
DS3181	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples
DS3182	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples
DS3183	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	
DS3184	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 3409: http://www.maximintegrated.com/an3409
APPLICATION NOTE 3409, AN3409, AN 3409, APP3409, Appnote3409, Appnote 3409