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APPLICATION NOTE 5321

Calibrating the ADC Internal Offset of the DS4830 Optical Microcontroller

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Abstract: The DS4830 optical microcontroller's analog-to-digital converter (ADC) offset can change with temperature and gain selection. However, the DS4830 allows users to measure the ADC internal offset. The measured ADC offset is added to the ADC offset register to nullify the offset error. This application note demonstrates the DS4830's ADC internal offset calibration in the application program.

Introduction

An analog-to-digital converter (ADC) converts an input voltage to a corresponding digital code. The perfect ADC represents this behavior across the code space. **Figure 1** illustrates the transfer function of a 3-bit ADC with 2V reference.

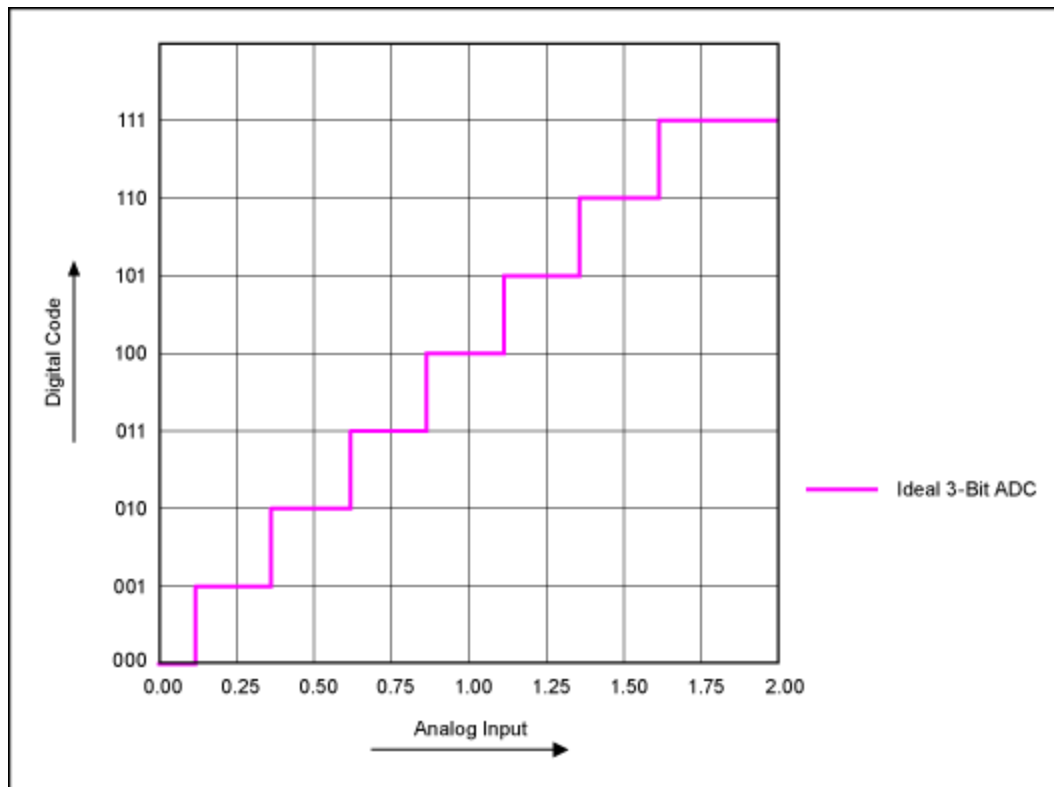


Figure 1. A 1/2 LSB-compensated ideal 3-bit ADC.

However, it is difficult to design an ADC that meets a perfect ADC's characteristics in all architectures. There are various errors, such as integral nonlinearity (INL), differential nonlinearity (DNL), gain, and offset introduced to the ADC output, due to various design limitations or constraints.

Offset error is the most common error in the ADC. The ADC's digital code output for the zero voltage input (the ADC input is connected to the ground) is called **ADC offset**. **Figure 2** depicts the transfer function of a 3-bit ADC with offset.

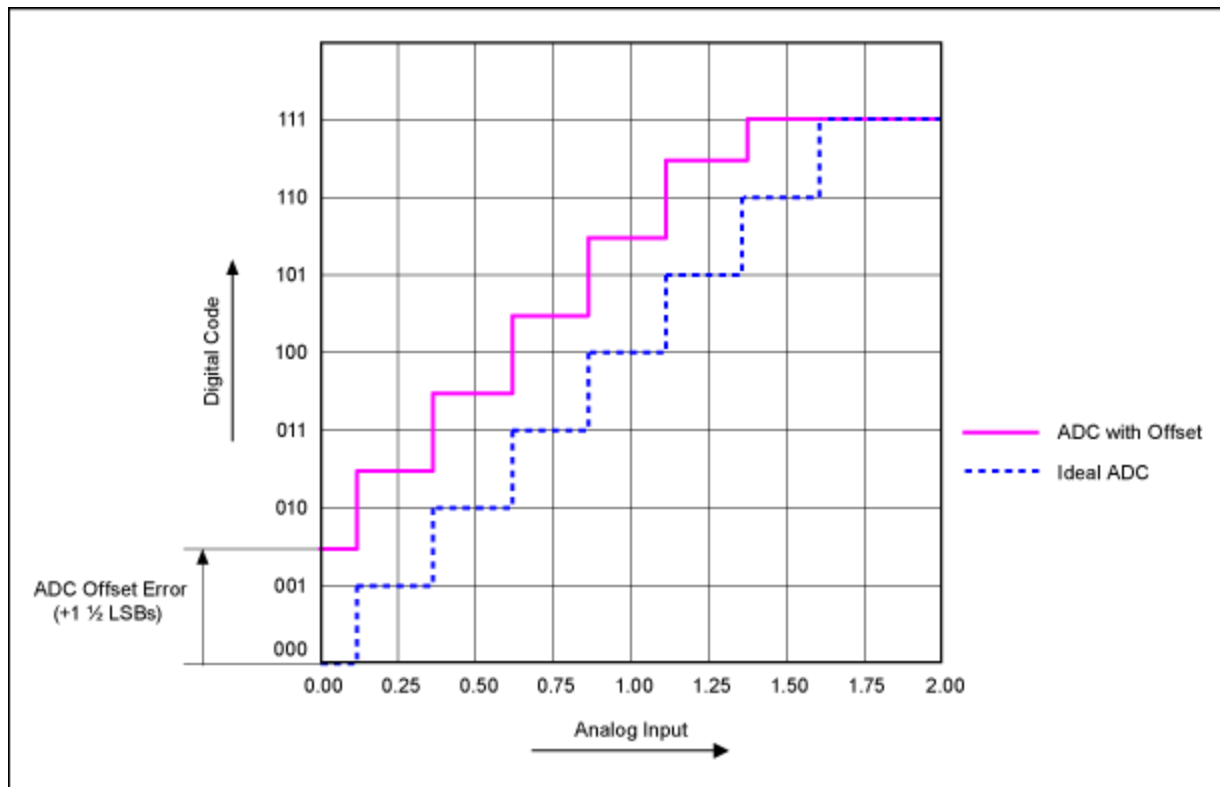


Figure 2. A 1/2 LSB-compensated 3-bit ADC with offset.

The DS4830 ADC Internal Offset

The [DS4830](#) optical microcontroller has a 13-bit ADC and the ADC Offset Register (ADVOFF) to calibrate the ADC internal offset. The offset is factory calibrated for every DS4830 for ADC gain ADCG1 (1.216V full scale) at room temperature. However, the DS4830 ADC internal offset can change with temperature and gain selection.

The DS4830 can measure the ADC internal offset for any of the available ADC gain settings. This measurement can then be used to calibrate the ADVOFF register. To measure the ADC internal offset, the ADC controller connects internal ground to the ADC input and starts conversion on the ADC. The ADC controller has a dedicated channel select at location **25** that instructs the ADC controller to measure the ADC internal offset. The ADC controller does not have a dedicated data buffer to store the ADC internal offset conversion result. To access the internal offset conversion result, the location override option in the ADC controller must be used.

Location Override Option for ADC Internal Offset

By default, the ADC conversion results are stored at the ADC buffer location corresponding to the channel number. The ADC controller provides a "location override" option. This option allows the ADC conversion results to be placed at any data buffer location (0-24 data buffer locations). The ADC Control Register (ADCN) has the location override LOC_OVR bit. Setting this bit to 1 will enable the user to select an alternate location for storing the ADC conversion result. The alternate location is defined by the ADDATA[12:8] bits (ALT_LOC[4:0]) when the ADC Conversion Configuration Register Select bit

(ADCFG) in the ADC Status Register (ADST) is set to 1.

ADC Configuration Steps for Internal Offset Measurement

The steps below explain the DS4830's ADC Data and Configuration Register (ADDATA) configuration for ADC internal offset measurement.

1. The following bits are set to corresponding values in ADCN and ADST registers.
 1. Location override bit (ADCN.LOC_OVR) to 1
 2. ADC Configuration Select bit (ADST.ADCFG) to 1
 3. ADC Register Index bits (ADST.ADIDX[4:0]) to 0
2. Write to the ADDATA Register (ADDATA). The ADC Channel Select bits ADCH[4:0] in the ADDATA[4:0] bits should be 25. Additionally, write (any value between 0 to 24) at the alternate location bits ALT_LOC[4:0] in the ADDATA register. The ADC internal offset conversion result is placed at the data buffer location pointed by the alternate location bits for the configuration. For example,
 1. **ADDATA = 0x0039**; This configures the ADC for internal offset measurement, differential mode, alternate location 0, gain 1, and ADC right alignment.
 2. **ADDATA = 0x4139**; This configures the ADC for internal offset measurement, differential mode, alternate location 1, gain 3, and ADC right alignment.
 3. **ADDATA = 0x6439**; This configures the ADC for internal offset measurement, differential mode, alternate location 4, gain 4, and ADC right alignment.
3. Set ADC Configuration Select (ADST.ADCFG) to 0 and ADC Register Index bits (ADST.ADIDX[4:0]) to 0.

ADC Internal Offset Measurement and Calibration

After configuring the ADC for internal offset measurement, the ADC Conversion Start bit (ADCONV) in the ADCN register is set to 1 to begin the ADC conversion. The ADC controller connects internal ground to the ADC input to measure the ADC internal offset and starts conversion on the ADC. The conversion result is the **measured ADC internal offset**. This can be read from the data buffer location indicated by the ALT_LOC[4:0] bits, which are set during the ADC configuration.

To calibrate the ADC internal offset, add the negative value (2's complement) of the measured ADC internal offset to the ADVOFF register. A few examples for ADVOFF values based on the measured ADC internal offset are shown in **Table 1**. These ADVOFF values assume that the factory-calibrated ADVOFF value is 0. During normal ADC operation, the value in ADVOFF is added to the conversion result prior to final result to the data buffers.

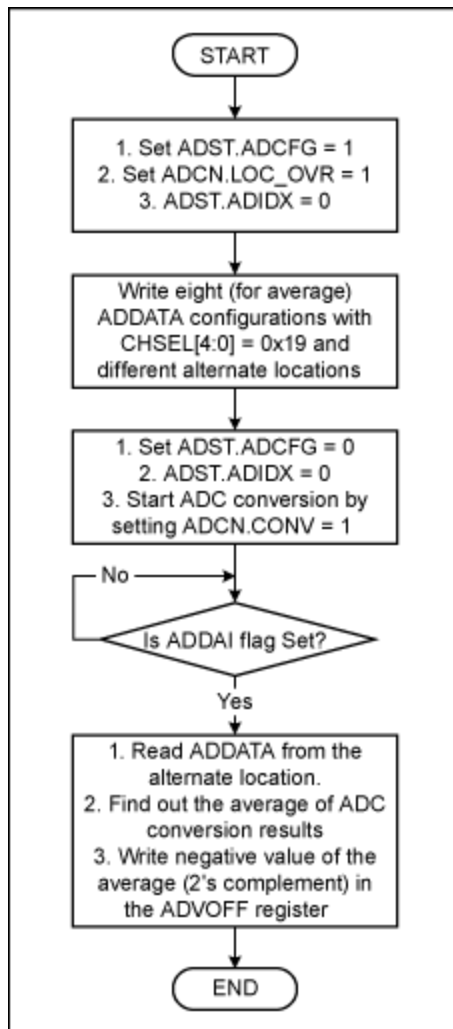
Table 1. ADVOFF Register Values for ADC Internal Offset		
Measured ADC Internal Offset		ADVOFF Register (in Hex)
(in Decimal)	(in Hex)	
-2	FFFEh	0002h
-1	FFFFh	0001h
0	0000h	0000h
1	0001h	FFFFh
2	0002h	FFFEh

Note: During power-on-reset (POR), the calibrated value is overwritten with the factory default value.

Sample Code

The code in [main.c](#) demonstrates the ADC internal offset calibration steps.

Flow Chart



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