Keywords: max3580, dvb-t, gb20600, tuner, terrestrial, nordig, mbrai

APPLICATION NOTE 4258

Application considerations for the MAX3580 DVB-T tuner

Jun 24, 2008

Abstract: This application note contains the information necessary for implementing a MAX3580 DVB-T tuner solution that is NorDig 1.0.3 compliant. The information supplements the MAX3580 data sheet and C-code driver. Trade-offs between dual-loop and single-loop AGC control are discussed. The dual-loop AGC control option also satisfies MBRAI. Schematics and programming recommendations are presented.

Introduction

This application note, together with the MAX3580 data sheet and C-code driver, contains the necessary information for implementing a MAX3580 DVB-T tuner solution that is NorDig 1.0.3 compliant. The solution contains a MAX3580 with a discrete LNA and loop-through. This article analyzes the trade-offs between dual-loop and single-loop AGC control, and details each solution. Corresponding application schematics are provided. Register programming recommendations for optimal performance are presented. Details for an optimal demodulator interface are included.

Click here for an overview of the wireless components used in a typical radio transceiver.

The dual-loop AGC control option also satisfies MBRAI. The single-loop AGC control option has not been tested for MBRAI.

Performance comparison between dual-loop and single-loop AGC

The MAX3580 gain can be controlled by either a dual-loop or single-loop AGC solution. While a dual-loop approach has better maximum signal performance and slightly lower BOM cost, it requires use of a demodulator with two PWM outputs and the software is somewhat more complex. Measurements show that both solutions are NorDig 1.0.3 compliant.

For dual-loop AGC, one filtered demodulator PWM output controls the BB_AGC and a second PWM output controls the RF_AGC. For single-loop AGC, one filtered demodulator PWM output controls the BB_AGC; the RF_AGC is subsequently controlled by connecting to the BB_AGC through a simple PNP transistor circuit. The more flexible dual-loop AGC offers better maximum signal performance, because it supplies a more optimal RF_AGC voltage under strong signal conditions. Further details are provided later in the section, *Dual-loop AGC control description*.

Figure 1 shows a performance comparison between dual-loop and single-loop AGC control of the

MAX3580.

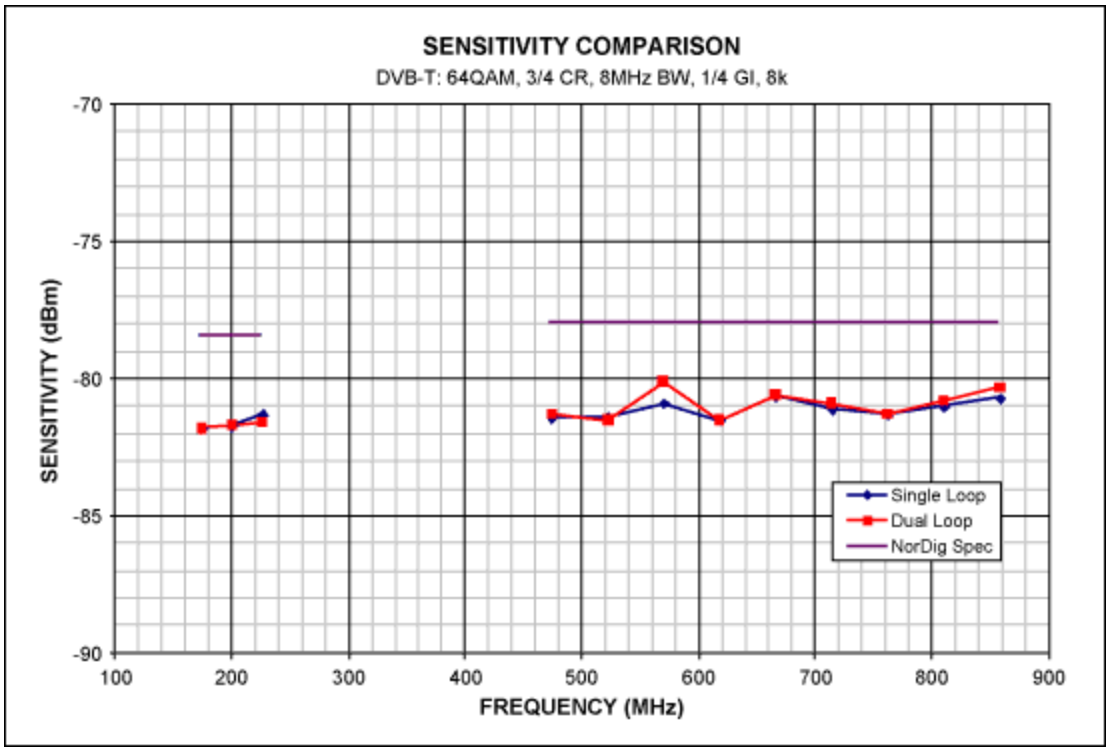


Figure 1. Sensitivity comparison between dual-loop and single-loop AGC control.

Figure 1 shows that sensitivity is similar for dual-loop and single-loop AGC control. The margin to NorDig exceeds 2dB. The QEF limit here is BER = 2e-4. Due to measurement system limitations, an 8MHz bandwidth signal is used for both VHF-III and UHF measurements. Note that a 0.6dB improvement in VHF-III sensitivity is expected when measured with the 7MHz bandwidth signal specified by NorDig.

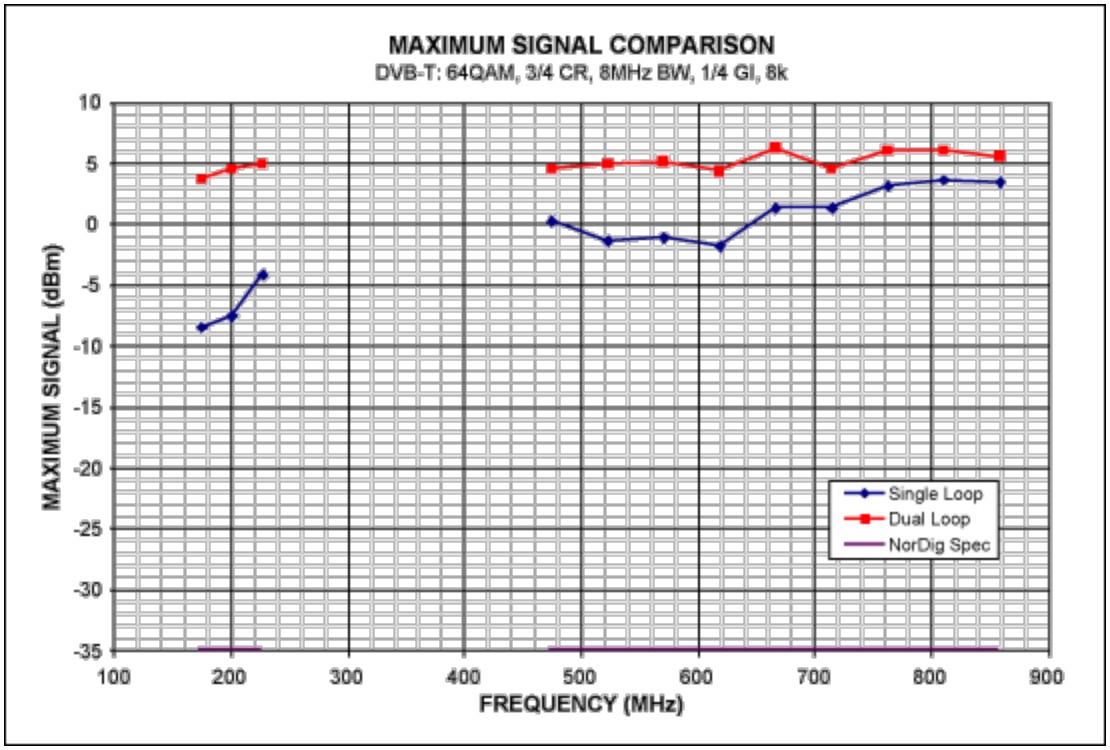


Figure 2. Maximum signal comparison between dual-loop and single-loop AGC control.

Although maximum signal performance for both AGC solutions exceeds the NorDig requirement by more than 25dB, **Figure 2** shows that the dual-loop maximum signal performance is at least 9dB better than the single loop for VHF-III, and at least 2dB better for UHF. Dual-loop maximum signal performance exceeds 3dBm for both bands, while the worst-case measurement for single-loop AGC is -8.4dBm at 174MHz. Again, the QEF limit here is BER = 2e-4.

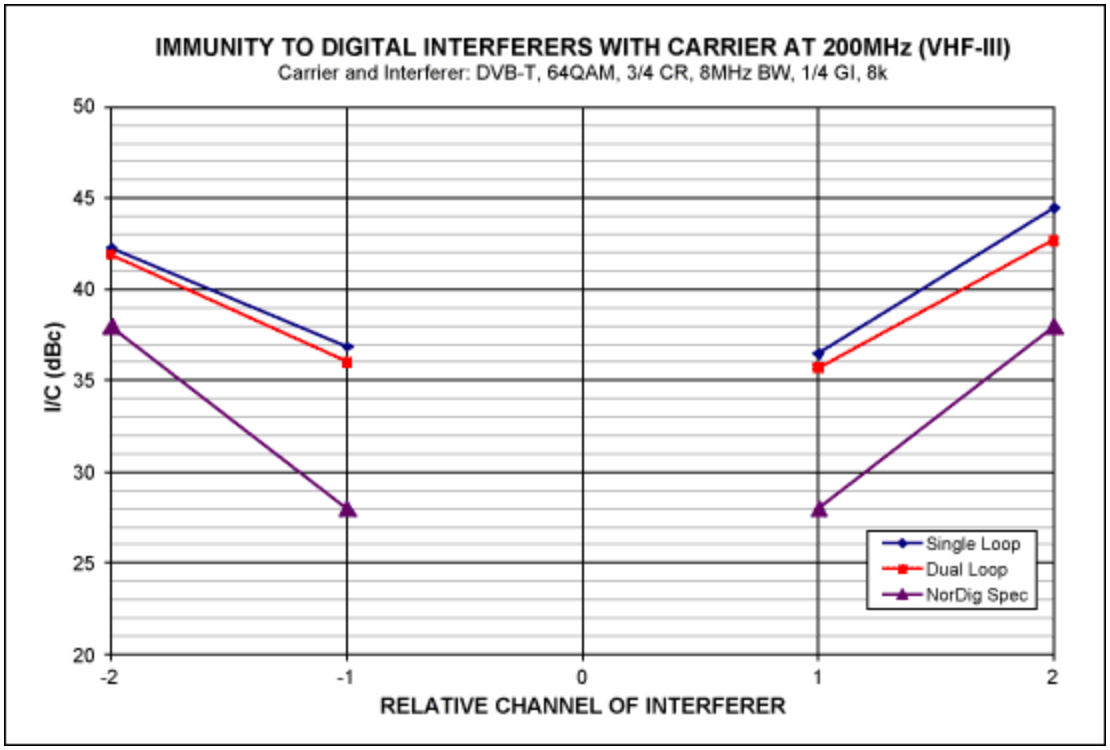


Figure 3. Digital Interference-to-Carrier (I/C) comparison between dual-loop and single-loop AGC control at VHF-III.

Figure 3 shows that the digital I/C performance at VHF-III is similar for both AGC options; at least 4dB of margin is present for both options. Again, the QEF limit here is BER = 2e-4.

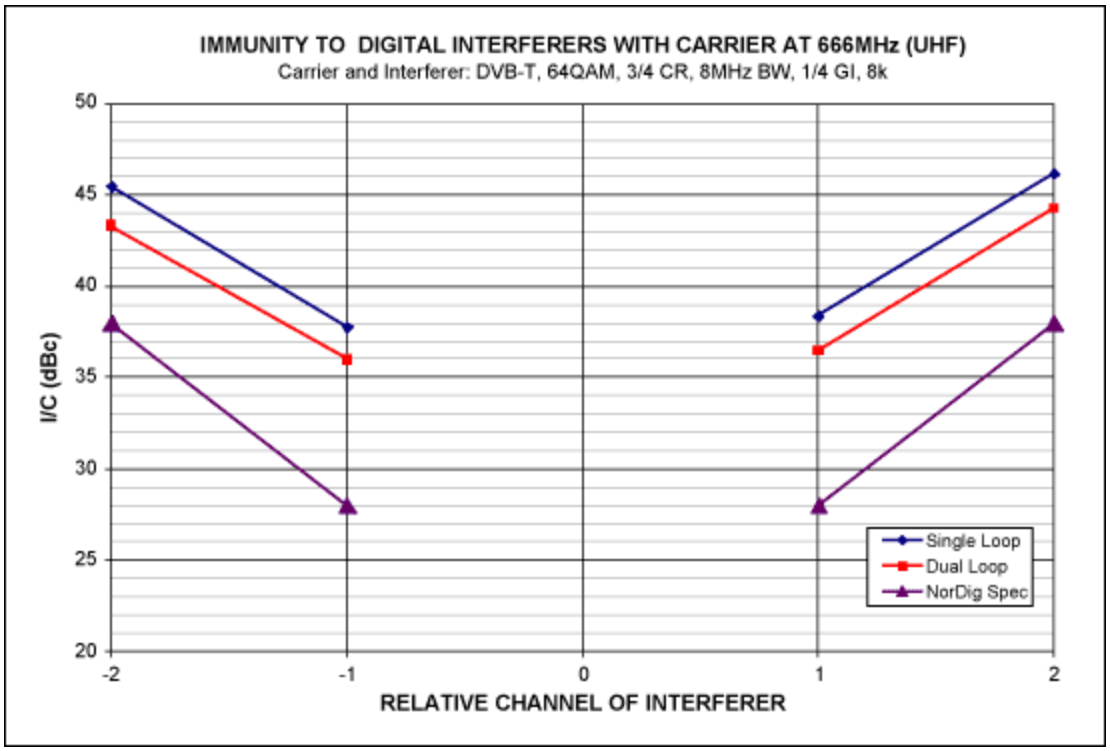


Figure 4. Digital I/C comparison between dual-loop and single-loop AGC control at UHF.

Figure 4 shows that the digital I/C performance at UHF is about 2dB better for dual-loop AGC control. Again, the QEF limit here is BER = 2e-4.

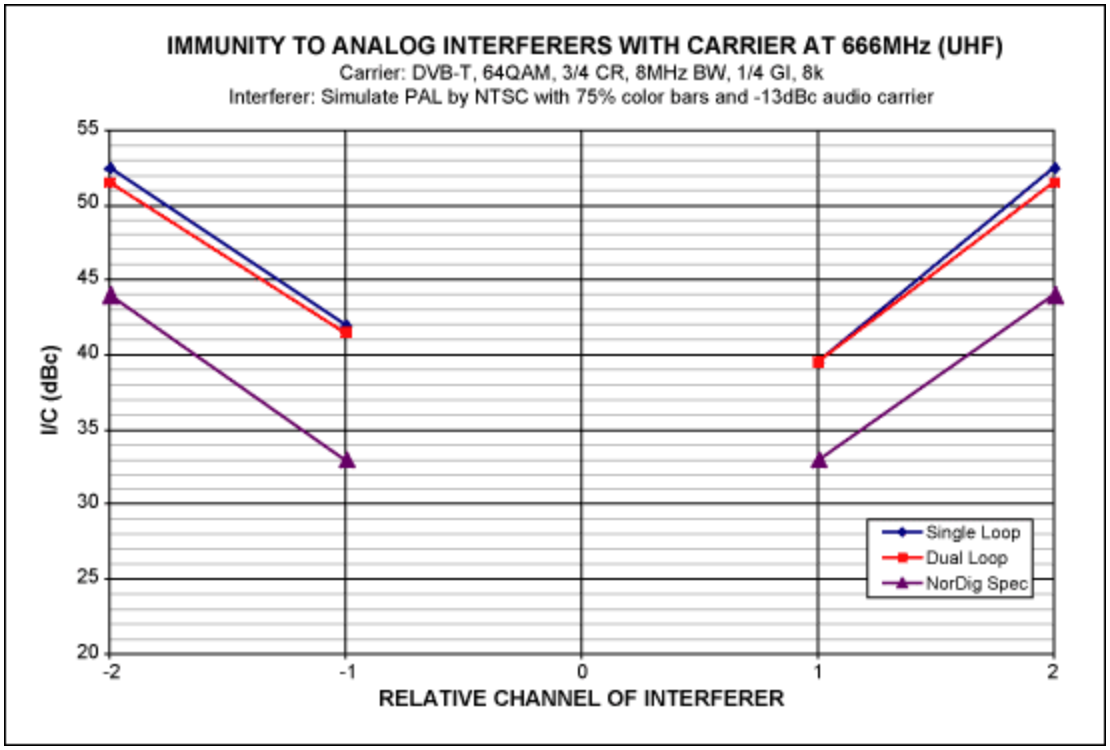


Figure 5. Analog I/C comparison between dual-loop and single-loop AGC control.

Figure 5 shows that the analog I/C is similar for both AGC options. At least 6dB of margin is present. The QEF limit here is "no packet errors in 60 seconds."

Due to measurement equipment availability, a PAL interferer is simulated by a NTSC signal with 75% color bars and audio carrier at -13dBc. Since the NTSC signal is designed for a 6MHz channel, the NTSC signal is shifted in the 8MHz channel to the edge closest to the wanted carrier.

Dual-loop AGC control description

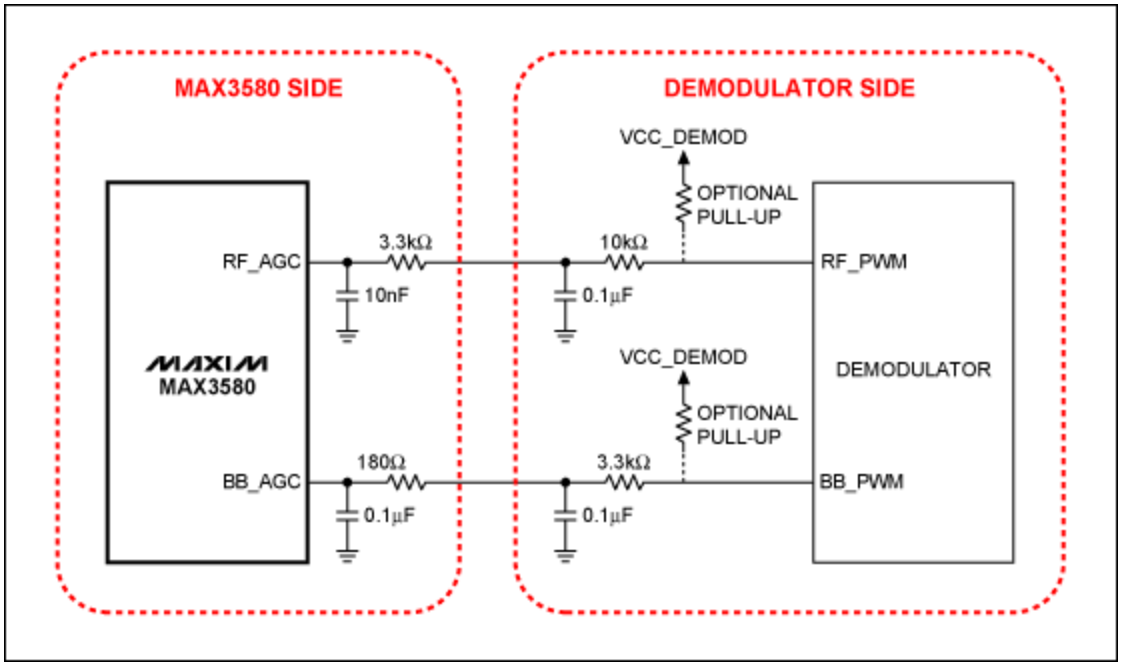


Figure 6. Dual-loop AGC schematic.

Figure 6 shows a schematic for dual-loop AGC control. Two PWM demodulator outputs are each RC-filtered twice before connecting to the MAX3580 AGC control pins. To give the best interference rejection on each line, one RC filter is placed near its PWM output and the second is placed near the MAX3580, at the edge of the MAX3580 shield.

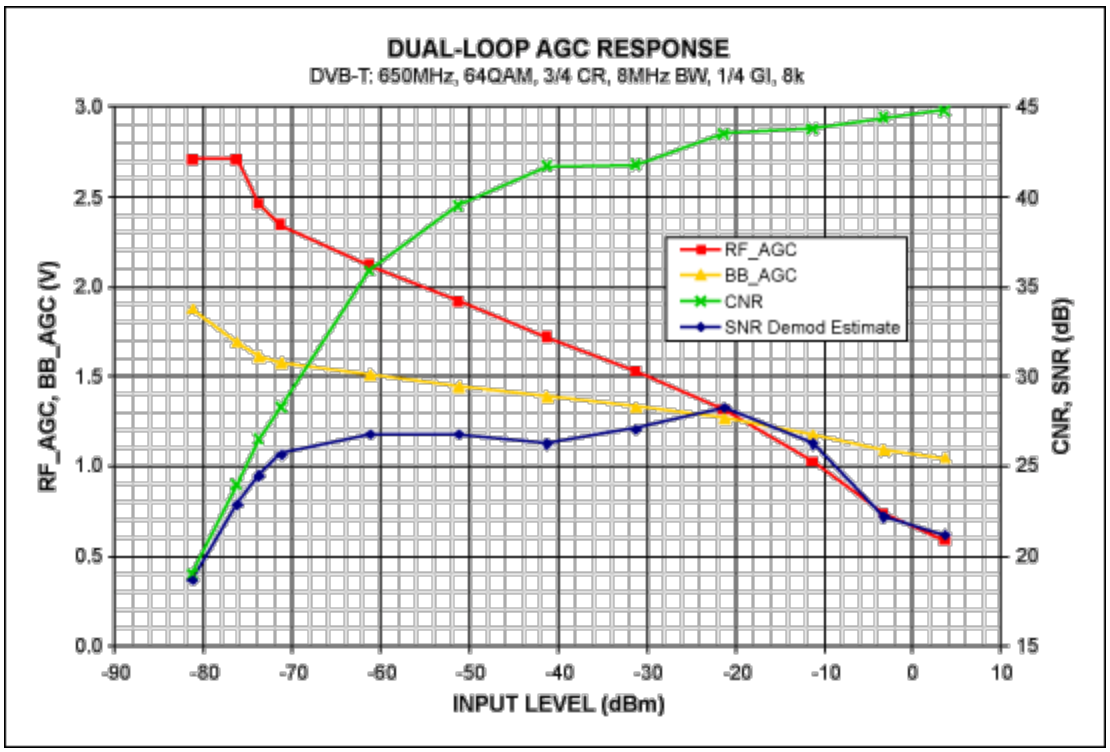


Figure 7. Dual-loop AGC response with wanted signal only.

Figure 7 shows the recommended AGC control voltages for the MAX3580 as the input level is increased. The demodulator PWMs provide these voltages. A PWM receives a hex word as an input from a software algorithm, and then outputs a pulse train that is RC-filtered, resulting in a DC control voltage. As the input level increases from sensitivity, the BB_AGC is active and reduces gain to keep the demodulator ADC input at the target level. The RF_AGC remains at maximum gain. Then when the BB_AGC reduces to 1.7V, the RF_AGC also becomes active. As the input level continues increasing, the demodulator ADC input level is adjusted to the target level by reducing both RF_AGC and BB_AGC according to a fixed ratio. A linearly-decreasing response for both AGC voltages is observed above -72dBm. The RF_AGC dominates through this region, as observed by its steeper slope. A transitional region occurs between -76dBm and -72dBm, where the RF_AGC gain adjustment is nonlinear with control voltage.

The CNR increases from 19.0dB at sensitivity to near the measurement system limit of 45dB for the maximum signal. CNR is measured with a spectrum analyzer probe at the demodulator input by freezing the AGCs and measuring channel power with the carrier turned on and off. The SNR plot is the demodulator estimate. The typical demodulator maximum SNR measurement limitation of about 24dB to 26dB occurs for input levels in the -72dBm to -10dBm range. The drop in SNR at input levels above -10dBm is explained by in-band intermodulation, which is included in the SNR measurement but not in the CNR measurement.

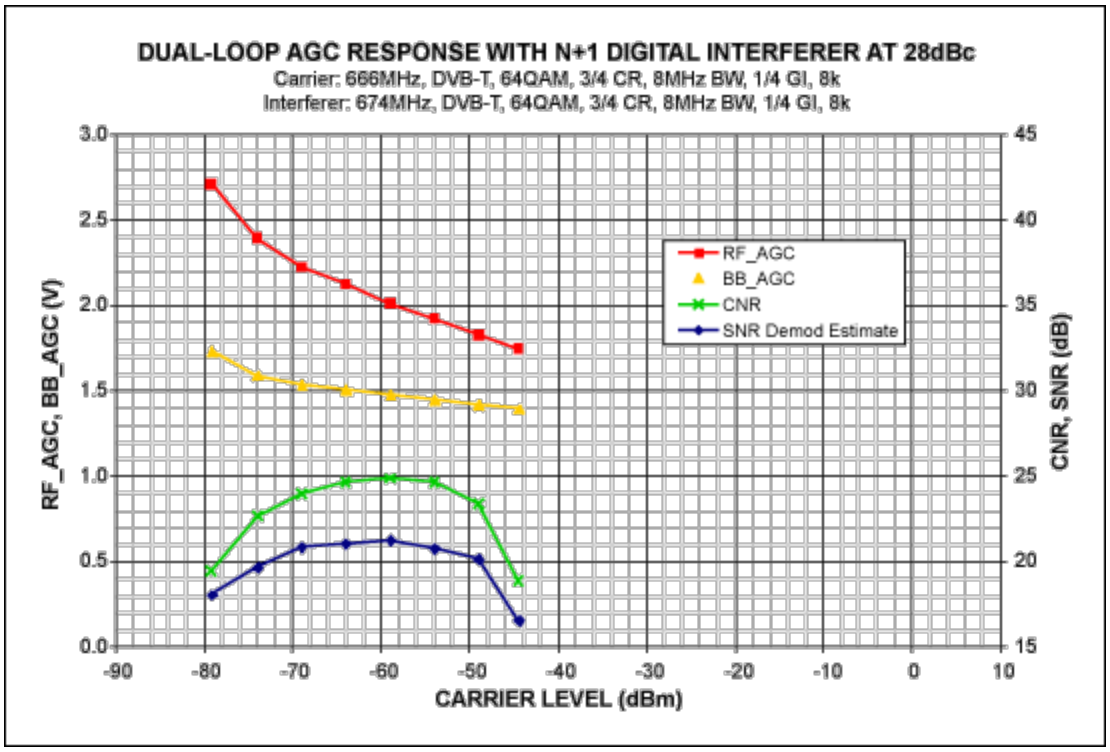


Figure 8. Dual-loop AGC response with a N+1 digital interferer at 28dBc.

Figure 8 shows that RF_AGC is lower (compared to Figure 7) when an interferer is added. This results in lower CNR and SNR values. Intermodulation from the interferer causes the CNR and SNR to drop when the wanted carrier level increases to the -54dBm to -44dBm range.

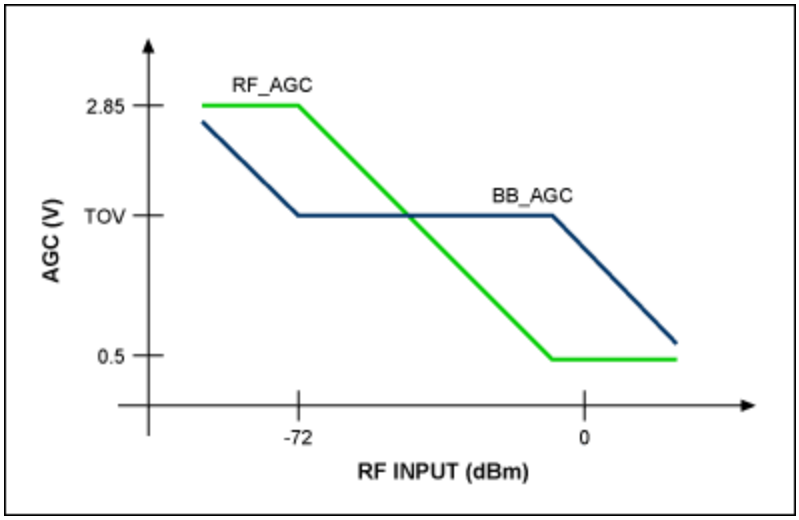


Figure 9. Alternate dual-loop gain control.

Figure 9 shows an alternate dual-loop gain control response, which has not been tested but is also likely to work well. Software for certain demodulators supports this approach.

A RF input power of -72dBm is the recommended take-over voltage (TOV) point for the RF_AGC. As the RF input power increases from the sensitivity level to the TOV, the BB_AGC reduces the baseband gain to maintain the desired level into the ADC. Meanwhile the RF_AGC is kept at maximum RF gain. When the BB_AGC digital word is reduced to the TOV, the demodulator freezes the BB_AGC and the RF_AGC becomes active. The RF_AGC remains active until reduced to 0.5V (minimum control voltage for the MAX3580 RF_AGC). The RF_AGC is now frozen and the BB_AGC again becomes active, further reducing the BB_AGC.

Single-loop AGC control description

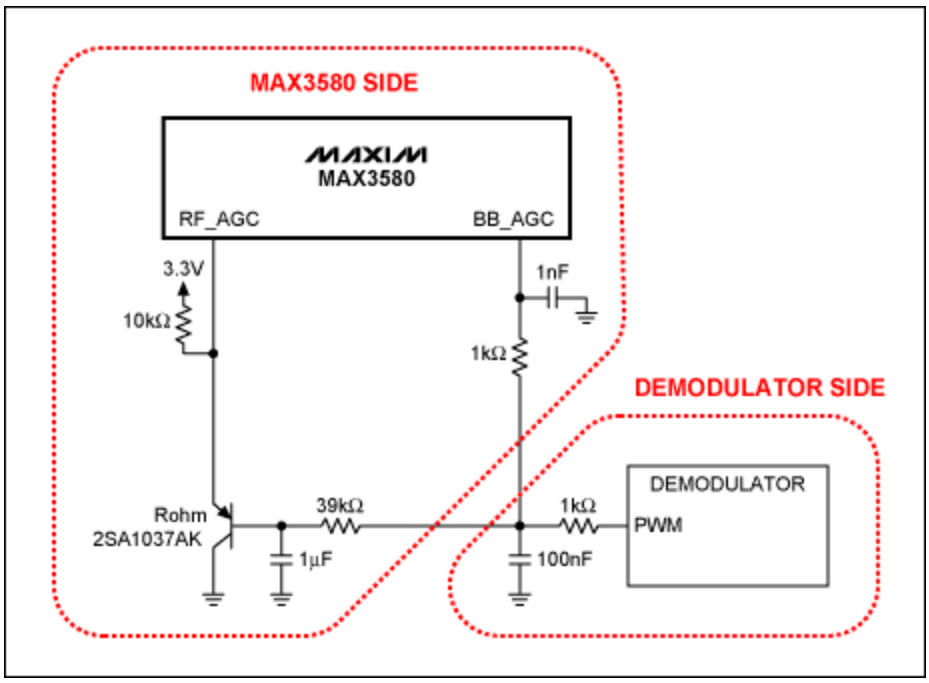


Figure 10. Single-loop AGC schematic.

In the single-loop AGC control solution of **Figure 10**, the BB_AGC is controlled by a filtered version of the demodulator PWM output. The RF_AGC is also controlled indirectly by a filtered version of the same PWM output. When the BB_AGC voltage is pulled low enough to turn on the PNP transistor, the RF_AGC voltage is pulled down approximately one diode drop above the BB_AGC voltage. If the BB_AGC rises high enough, the transistor is turned off, which results in the RF_AGC pulling up to nearly 3.3V by the pullup resistor.

In Figure 10 the components to place near the demodulator in the layout are enclosed within one dashed line, while the components to place near the MAX3580 are enclosed within a second dashed line. The 1µF and 1nF capacitors should be placed at the edge of the MAX3580 shield.

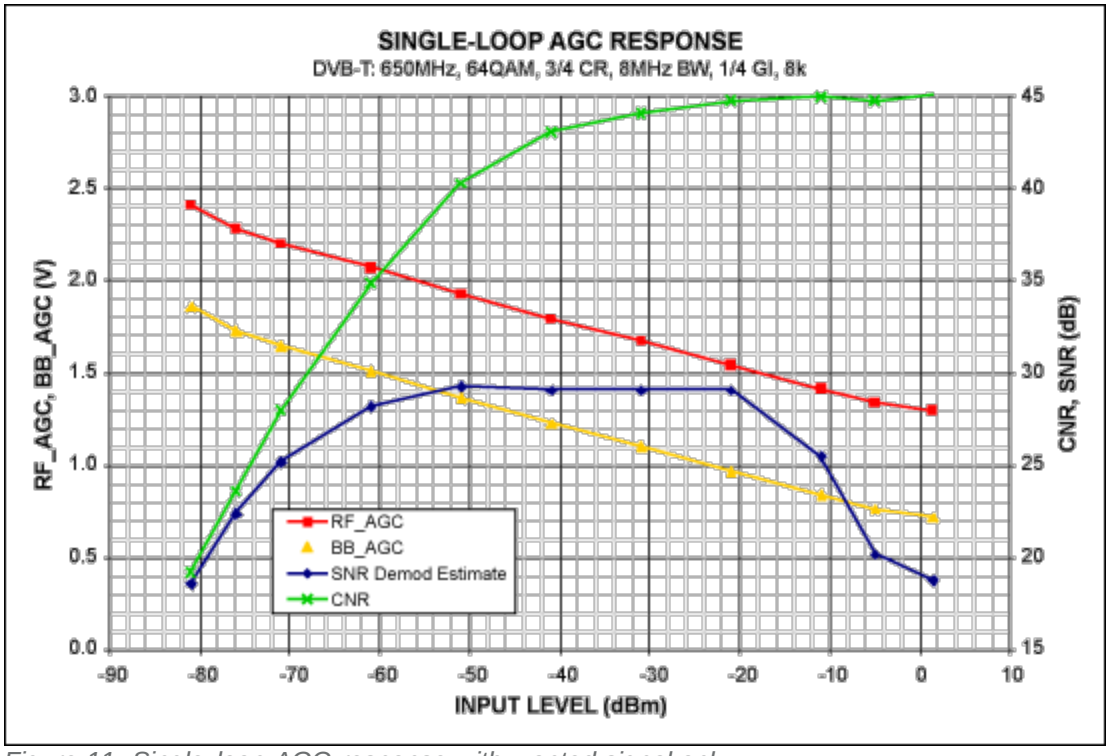


Figure 11. Single-loop AGC response with wanted signal only.

Figure 11 shows that as the input level increases, the RF_AGC is pulled down at ~0.6V above the BB_AGC voltage. The CNR increases from 19.2dB at sensitivity to the measurement system limit of 45dB for maximum signal. The drop in SNR at input levels above -20dBm is explained by in-band intermodulation, which is included in the SNR measurement but not in the CNR measurement.

Register programming

A brief overview of the required MAX3580 register programming is described here. Some register settings that optimize performance are also highlighted. The MAX3580 data sheet includes the complete details for programming its registers. A C-code driver is also available from Maxim to assist customers with the details of programming all MAX3580 registers in the recommended way. **Note**: Readers can request the MAX3580 C-code driver from their local Maxim field applications engineer or account manager.

To downconvert a particular RF frequency, the tracking filter must be programmed based on calculations using factory-tuned values stored in the on-chip Fuse Table (also called ROM Table). Similarly, the baseband filter bandwidth must be programmed to the corresponding factory-tuned value stored in the on-chip Fuse Table. One factory-tuned value is provided for 7MHz channels, typically VHF; a second factory-tuned value is provided for 8MHz channels, typically UHF. Furthermore, band select, N divider, and RF input select must all be programmed.

For optimal performance:

- Program the ICP bit (register 0x06 <6>) for 600µA.
- Program the SHDN_PD bit (register 0x08 <5>) to turn off the power detector.
- Program the RDIV bit (register 0x06 <7>) to 2 for VHF and to 1 for UHF.
- Optimize the DC Offset-Correction Threshold bits (register 0x0B <1:0>) for the specific demodulator, based on VHF sensitivity. Start at 0 and increase as high as 3 while sensitivity continues to improve.
- Optimize the DC Correction Speed bits (register 0x0B <3:2>) for the specific demodulator, based on VHF sensitivity. Start at 1 and increase to 2 if sensitivity improves.

I/Q interface

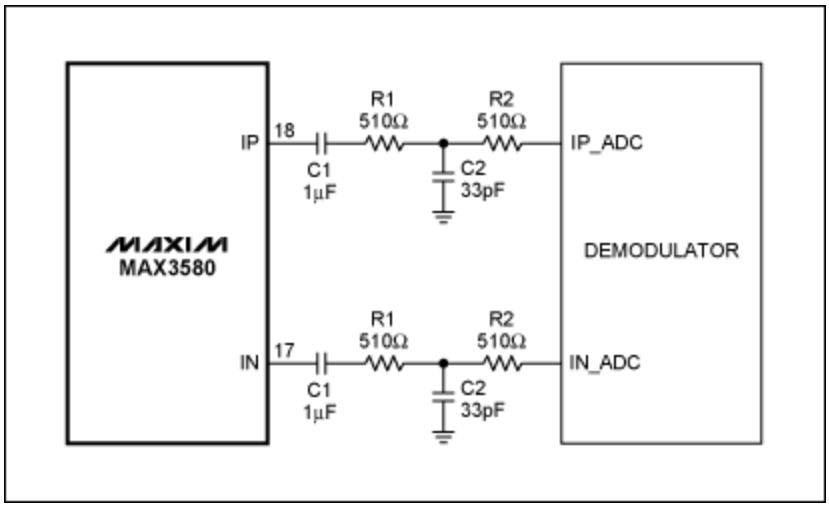


Figure 12. Recommended I channel interface (duplicate for Q channel).

Figure 12 shows T-shaped RC filters added to each I/Q differential line. These RC filters reject high-order digital clock harmonics at RF frequencies that otherwise conduct from the demodulator through the I/Q interface to the MAX3580 RF input and subsequently downconvert. These harmonics are attenuated by the R2-C2 lowpass RC filter and R1 resistive pad.

R1 and C2 serve a dual purpose as an anti-alias filter. Capacitor C1 is for AC coupling.

I²C interface

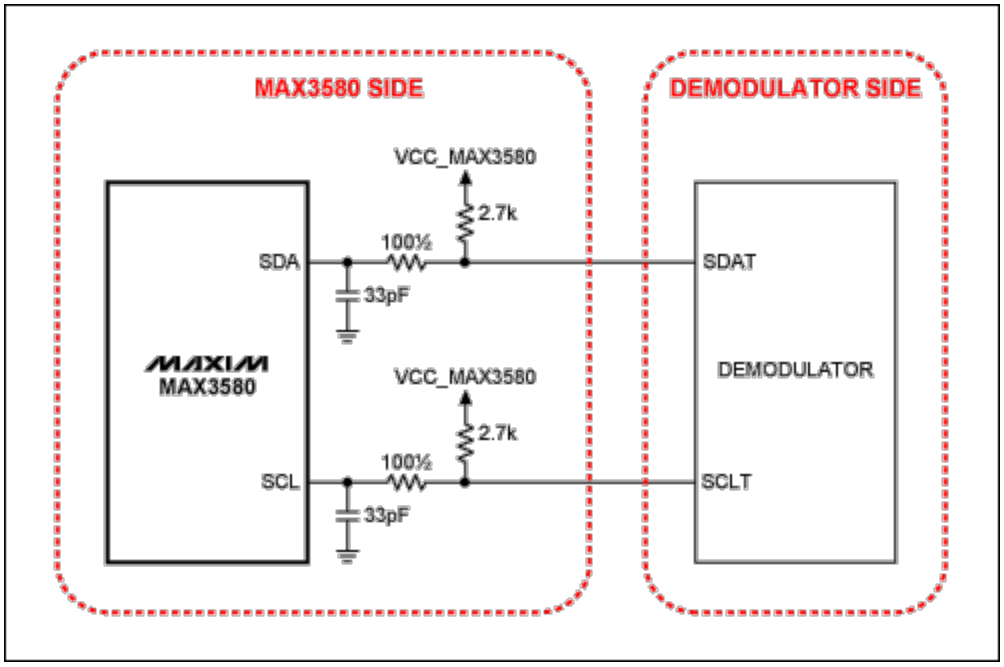


Figure 13. Recommended I²C line filtering.

Figure 13 shows the RC filtering recommended to reject interference conducted on the I²C lines. Place the 33pF capacitors at the edge of the MAX3580 shield.

Crystal oscillator reference

The MAX3580 crystal oscillator reference can typically be shared with the demodulator, which saves the cost and real estate for the demodulator crystal. The MAX3580's crystal oscillator operates over a wide range of frequencies, so that a frequency acceptable to the demodulator clock can be selected. Then the MAX3580's reference buffer pin drives the demodulator reference pin through a series 1kΩ resistor and 10nF capacitor. Note that the lowest usable frequency is preferable. Lower reference frequencies provide more sensitivity margin by reducing MAX3580 fractional PLL noise, particularly in the VHF band.

Care is required to ensure that the MAX3580's crystal-oscillator reference frequency tolerance is adequate to satisfy the typical ±50kHz derotation requirement of the demodulator. To do this, select an appropriate crystal frequency tolerance and ensure that the total capacitance of the series feedback capacitors (C19, C18, and C20 in the schematic in **Appendix A**) equals the crystal's load capacitance. A good starting point is to keep these feedback capacitors equal. Please contact your local Maxim field applications engineer or account manager to request assistance.

The MAX3580's reference oscillator circuitry can be also used as a high-impedance reference input driven by an external source. (This approach is not preferred, since reference harmonics could degrade MAX3580 performance.) When using an external reference, drive the MAX3580 XB input through an AC-coupling capacitor with an amplitude of approximately $1.5V_{P-P}$, and leave XE unconnected. Note that the phase noise of the external reference needs to exceed -140dBc/Hz at offsets of 1kHz to 100kHz.

Other guidelines

- The MAX3580 should be supplied by a dedicated regulator to minimize digital interference.
- To minimize coupling between different sections of the MAX3580 IC, the ideal power-supply routing

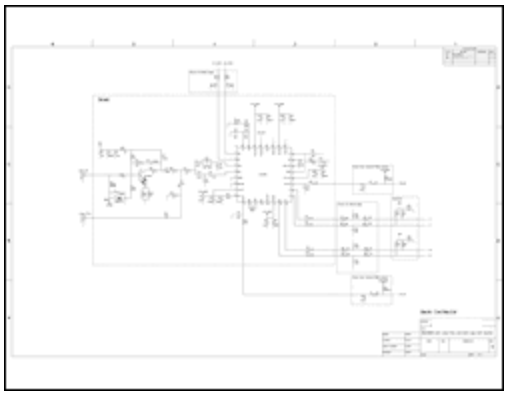
layout is a star configuration with a large bypass capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, with each trace going to separate V_{CC} pins on the MAX3580. To each V_{CC} pin connect a bypass capacitor, placed as close as possible to the pin. When multiple bypass capacitors are used at a single V_{CC} pin, place the smaller value capacitor closest to the pin. Use at least one via per bypass capacitor for a low-inductance ground connection.

- Place the crystal close to the XB and XE pins on the MAX3580.
- The three ground pins (GND_PLL, GND_CP, and GND_TUNE) must be connected to the ground plane by separate ground vias. They must not be directly connected to the exposed paddle.
- Route close together the two traces for the differential I channel. Do the same for the Q channel. Keep the I and Q short traces short.
- The target level into the demodulator is an important parameter in setting up an AGC control solution. For this application note, the target demodulator input level is 285mV_{P-P} differential with a CW signal. To measure this level, freeze the AGCs after the closed-loop AGC control reaches steady state with a DVB-T input signal at 666MHz and about -50dBm with 64QAM and 3/4 code rate. Then turn off the modulation and increase the input CW frequency to 667MHz, so a 1MHz baseband signal results. Finally, measure the resulting level at the demodulator input using a high impedance differential probe (200kΩ || < 1pF).
- A MAX3580 diplexer application note 3700 is available, "Front-End Diplex Filter for MAX3580."

Conclusion

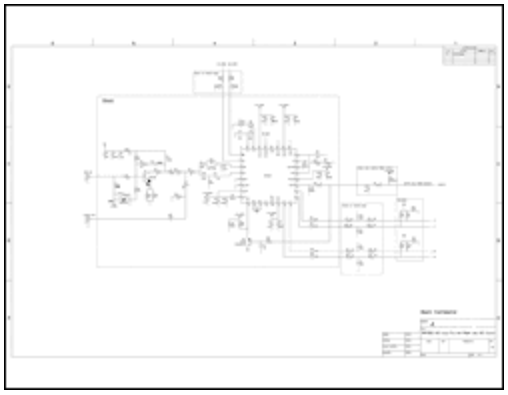
The MAX3580 gain can be controlled by either a dual-loop or single-loop AGC solution. Dual loop has better maximum signal performance and slightly lower BOM cost, but requires use of a demodulator with two PWM outputs and more complex software. Measurements show that both solutions are NorDig 1.0.3 compliant. This application note shows application details for implementing both solutions.

Appendix A. Dual-loop AGC application schematic



More detailed image (PDF, 211kB)

Appendix B. Single-loop AGC application schematic



More detailed image (PDF, 210kB)

Related Parts		
MAX3580	Direct-Conversion TV Tuner	Free Samples

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