

SCOPE: VOLTAGE-OUTPUT, 12-BIT MULTIPLYING DACs

<u>Device Type</u>	<u>Generic Number</u>	
01	MAX502A(x)/883B	12-Bit, 4 Quadrant, Voltage-Output
02	MAX502B(x)/883B	Multiplying Digital to Analog Converter

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
MAXIM SMD RG L	GDIP1-T24 or CDIP2-T24	24 LEAD CERDIP	J24

Absolute Maximum Ratings

V_{DD} to DGND	-0.3V, +17V
V_{SS} to DGND.....	+0.3V, -17V
V_{DD} to AGND	-0.3V, +17V
V_{OUT} to AGND 1/	$V_{DD} + 0.3V$, $V_{SS} - 0.3V$
AGND to DGND	-0.3V to V_{DD}
Digital Input Voltage to DGND	-0.3V to V_{DD}
V_{REF} to AGND	$\pm 25V$
RFBF to AGND	$\pm 25V$
RA to AGND	$\pm 25V$
RB to AGND	$\pm 25V$
RC to AGND	$\pm 25V$

Lead Temperature (soldering, 10 seconds) +300°C

Storage Temperature -65°C to +150°C

Continuous Power Dissipation $T_A = +70^\circ C$

24 pin CERDIP(derate 12.5mW/°C above +70°C) 1000mW

Junction Temperature T_J +150°C

Thermal Resistance, Junction to Case, θ_{JC}

24 pin CERDIP..... 40°C/W

Thermal Resistance, Junction to Ambient, θ_{JA} :

24 pin CERDIP..... 80°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
Positive Supply Voltage, (V_{DD})	+11.4V to +15.75V
Negative Supply Voltage (V_{SS}).....	-11.4V to -15.75V

NOTE 1: V_{OUT} may be shorted to AGND, V_{DD} , or V_{SS} if the power dissipation of this package is not exceeded.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125°C 2/, 3/, 5/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES		1,2,3	All	12		Bits
Relative Accuracy	INL		1	01 02		±0.5 ±0.75	LSB
			2,3	01 02		±0.75 ±1.0	
Differential Nonlinearity	DNL		1,2,3	All		±1.0	LSB
Zero Code Offset Error	VOE		1 2,3	All		±2.0 ±3.0	mV
Gain Error	AE	RFB, V _{OUT} connected	1,2,3	All		±3.0	LSB
		RC or RB connected to V _{OUT} , V _{REF} =2.5V				±4.5	
		RA, V _{OUT} connected, V _{REF} =2.5V				±6.0	
Reference Input Resistance	R _{IN}		1,2,3	All	8	16	kΩ
Application resistor ratio matching	R _{MATCH}	RA to RB to RC match	1,2,3	All		0.5	%
Input Current	I _{IN}	V _{IN} =0V and V _{DD}	1 2,3	All		±1.0 ±10	μA
Input High Level Voltage	V _{IH}		1,2,3	All	2.4		V
Input Low Level Voltage	V _{IL}		1,2,3	All		0.8	V
Supply Current	I _{DD}	V _{OUT} unloaded	1,2,3	All		10	mA
	I _{SS}					4	
Power Supply Rejection	PSR	V _{REF} =-10V, -8.9V, V _{DD} =+15V ±5%, +12V ±5%	1,2,3	All		±0.02	%/%
		V _{REF} =+10V, +8.9V, V _{SS} =-15V ±5%, -12V ±5%					
Open Loop Gain	AVO	V _{OUT} = ±10V, R _L =2kΩ, RFB not connected NOTE 4	4,5,6	All	90		dB
Functional test	FT	See Figure 2, Verify truth table	7,8				
Output-Voltage settling time	t _s	To ±0.01% of full scale, NOTE 4	9 10,11	All		5	μs
Chip select to write-setup time	t _{CS}	See Figure 1b	9,10,11	All	0		ns
Write Pulse Width	t _{WR}	See Figure 1b	9 10,11	All	40 60		ns
Data-setup time	t _{DS}	See Figure 1b	9,10,11	All	60		ns
Data-hold time	t _{DH}	See Figure 1b	9,10,11	All	10		ns

NOTE 2: Dual supply: V_{DD}=+11.4V to +15.75V, V_{SS}=-11.4V to -15.75V, V_{REF}=+10V, AGND=DGND=0V, R_L=2kΩ, C_L=100pF.

NOTE 3: V_{OUT} must be less than V_{DD}-2.5V and greater than V_{SS}+2.5V to ensure correct operation.

NOTE 4: Parameter is guaranteed to the limit specified but is not tested.

NOTE 5: Unused feedback resistors should be shorted to analog ground.

Figure 1b: See Commercial Datasheet.

	Package	ORDERING INFORMATION:	SMD Number
01	24 pin Cerdip	MAX502AMRG/883B	5962-8876701LA
02	24 pin Cerdip	MAX502BMRG/883B	5962-8876702LA

FIGURE 1: **TERMINAL CONNECTIONS**

	24 PIN CERDIP		
1	V _{OUT}	13	D1
2	D11	14	D0
3	D10	15	$\overline{\text{WR}}$
4	D9	16	$\overline{\text{CS}}$
5	D8	17	V _{REF}
6	D7	18	AGND
7	D6	19	V _{SS}
8	D5	20	V _{DD}
9	D4	21	RA
10	D3	22	RB
11	D2	23	RC
12	DGND	24	RFB

FIGURE 2: **TRUTH TABLE** H=High state L=Low state
R=Rising edge X=don't care

$\overline{\text{WR}}$	$\overline{\text{CS}}$	OPERATION
H	X	No Operation
X	H	No Operation
L	L	Input register is transparent
L	R	Input register is latched
R	L	Input register is latched

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.