MAX96724/MAX96724F/MAX96724R DEV_REV=1 (B-0A) ERRATA SHEET

Corresponds to Data sheet 19-101575; Rev 4; 1/2023 Errata

DEV_REV=1 (per reading of register 0x4C)

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a four-digit code in the form yyww, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. The revision of these components can be found by reading DEV_REV from register 0x4C.

1) Certain Datatypes and pixel line counts will assert ERRB pin for SRAM LCRC error

Description:
There is no video corruption, only an errant flag causing the ERRB pin to assert.
The combined configuration of 4WxH aggregation + Pixel mode + DPHY mode + 4x2 MIPI has the potential to assert ERRB pin for SRAM LCRC error.

Workaround:
If not safety critical application, disable flag assertion to ERRB pin by setting register 0x458[7:4] = 0x0.
If safety critical, certain datatypes and pixel lengths in this configuration do function properly. Contact factory for further details of specific configuration.

Resolution:
No planned fix

2) SRAM LCRC errors will occur in Tunnel Mode if Frame or Line counters enabled in MIPI packet header

Description:
There is no video corruption, only an errant flag causing the ERRB pin to assert.
In Tunnel Mode, MIPI short packets containing Frame Start, Frame End, Line Start or Line End including a non-zero frame or line count will cause ERRB pin to assert for SRAM LCRC error.

Workaround:
If not safety critical application, disable flag assertion to ERRB pin by setting register 0x458[7:4] = 0x0.
Disable frame or line count from MIPI source if possible.

Resolution:
No planned fix

3) MIPI video output in synchronous aggregation modes can be masked or held in reset at the start of video output

Description:
Synchronous aggregation (4WxH, Wx4H) configurations may trigger the video mask timeout timer depending on when initial video is transmitted from incoming sensors.

Workaround:
Disable Video Mask timeout timer before start of video and re-enable after all MIPI video output has started. Disable Video Mask timeout timer by setting register 0x446[7:4] = 0x00.

Resolution:
No planned fix

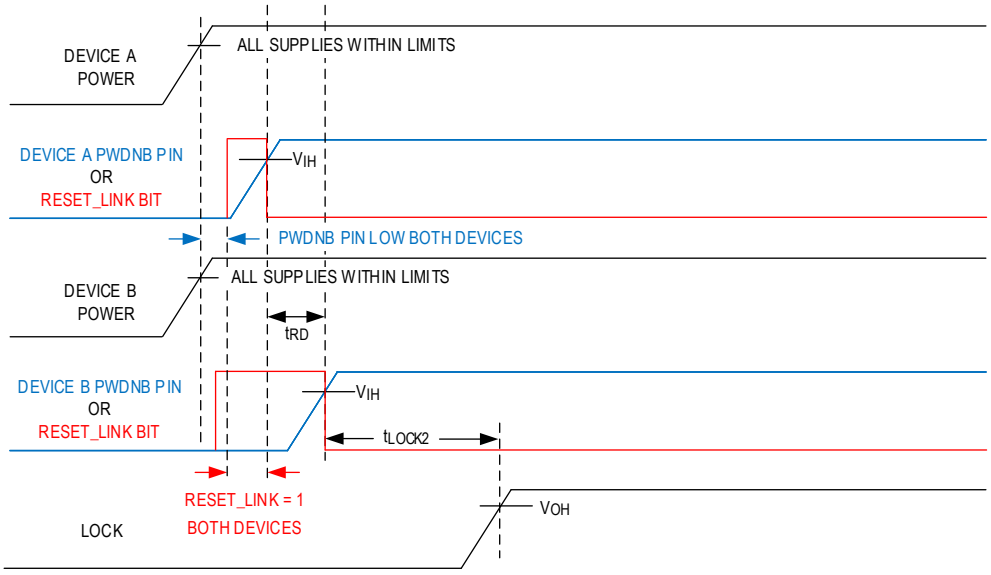
4) GMSL link lock times may increase if DES and SER are powered up or released from reset with significant delay relative to each other

Description:

Due to timeouts in the link layer, GMSL link lock times (t_{LOCK2}) may increase above 160ms[1] (or 200ms[2]) if deserializer (DES) and serializer (SER) links are powered up or released from reset with more than 90ms[1] (or 70ms[2]) delay (t_{RD}) relative to each other. This issue applies only if the SER is released from reset first.

Note 1: The first values (t_{LOCK2}>160ms and t_{RD}>90ms) refer to the links in which DES and SER devices have typical lock time <55ms.
Note 2: The second set of values (t_{LOCK2}>200ms and t_{RD}>70ms) are for the links where the typical lock times of either the SER or DES are greater than or equal to 55ms.

In certain configurations, devices must be programmed after the power-up (e.g. to set the link rate) and the link must be reset to trigger the configuration change. As the user-issued link resets may interrupt on-going link lock attempts, it is critical to ensure that link resets are issued on both SER and DES sides and are overlapping in time as shown on the diagram below. Without overlapping resets of both SER and DES devices, one of the devices may have to wait to complete its timeout sequence before it becomes available for the next link lock attempt. Overlapping link resets on SER and DES devices should be released within t_{RD} time window relative to each other if the SER is released from reset first, similar to the power up t_{RD} requirement.



Workaround:

1. Implement DES and SER programming sequence such that DES is powered up or released from link reset before SER. If link resets are used, make sure that they overlap.
2. If SER is powered up or released from link reset after DES, implement DES and SER programming sequence to power up or release DES and SER link resets within t_{RD}<90ms (or t_{RD}<70ms) of each other. If link resets are used, make sure that they overlap.
3. If workarounds #1 or #2 cannot be used, contact factory for further guidance on optimizing the lock time.

Resolution:

No silicon revision is planned.

5) GMSL2 Link requires register writes for robust 6 Gbps operation.

Description:
There are internal circuits (Error Channel) that are, by default, periodically power cycled to perform receiver optimization functions. This power cycling can degrade performance (e.g., link performance, video integrity, etc.) under certain conditions (higher VDD voltages; low temperatures). This problem is prevented by disabling the power cycling function, so the Error Channel is powered on continuously.

Gbps	Mode of operation	Workaround Requirement
6	Single Link	Recommended at next software update cycle
6	Multiple Link	Required
3	Single/Multiple Link	Not needed

Workaround:
The Error Channel must be forced to remain on (not power cycled) via register writes below.

RLMS49 (0x1449, 0x1549, 0x1649, 0x1749)

Bit	7	6	5	4	3	2	1	0
Field	-	RSVD	RSVD	RSVD	RSVD	ErrChPwrUp	RSVD	RSVD
Reset	-	1	1	1	0	0	0	1
Access Type	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

Bitfield	Bits	Description	Decode
ErrChPwrUp	2	Error Channel Power Up control	0x0: Automatic control 0x1: Force always on

Register	Default	Workaround	Description
0x1449	0x71	0x75	Force Channel A Error Channel always on
0x1549	0x71	0x75	Force Channel B Error Channel always on
0x1649	0x71	0x75	Force Channel C Error Channel always on
0x1749	0x71	0x75	Force Channel D Error Channel always on

These register writes must be performed immediately after every power-up and device reset. Receiver optimization and all other functions are not impacted by this workaround. Total current increase is insignificant and does not impact the EC table values.

Resolution:
No silicon revision is planned.

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REVISION HISTORY

REV	CHANGES MADE	DATE	INIT.
0	Initial Release	6/22	PF
1	Added errata 5, “GMSL2 Link requires register write for robust operation”.	5/23	CC