*Click here to ask an associate for production status of specific part numbers.*

# 5.5V Input, 0.4A/1.05A Switching Current Buck-Boost Converter with 400nA IQ

**MAX77837**

## General Description

The MAX77837 is the industry's smallest nanoPower buck-boost converter optimized for single-cell battery chemistries that are used in wearable and Internet of Things (IoT) applications.

The converter operates on an input supply between 1.8V to 5.5V. Output voltages between 1.8V to 5.2V are set through resistors connected to two hardware control pins. The IC can operate in Continuous Conduction Mode (CCM), Skip Mode, and a Low-Power Mode to ensure high efficiency over a wide load current range. In addition, the IC features an ultra-low quiescent current of 430nA (typical) and a shutdown current of 10nA (typical), making it ideal for battery-powered applications requiring a long standby time.

The MAX77837 offers two unique hardware control pins, SEL1 and SEL2. The resistor connected at SEL1 ($R_{SEL1}$) selects a predefined combination of two output voltages between 1.8V to 5.2V, OUT1 and OUT2. The resistor connected at SEL2 ($R_{SEL2}$) allows two different configurations of switch current limit at 1050mA and 400mA to optimize external component size, enable or disable Dynamic Voltage Scaling (DVS) function, and select either hiccup or latch-off mode during a hard short event. $R_{SEL2}$ can also configure the startup voltage as OUT1 or OUT2, and the DVS function can change the output voltage from a lower $V_{OUT}$ to a higher $V_{OUT}$ as required without powering down the part.

The MAX77837 is available in both a 1.84mm x 1.03mm, 8-bump wafer-level package (WLP) with a bump pitch of 0.4mm and a 2.5mm x 2.0mm, 8-lead Flip Chip QFN package (FC2QFN).

## Benefits and Features

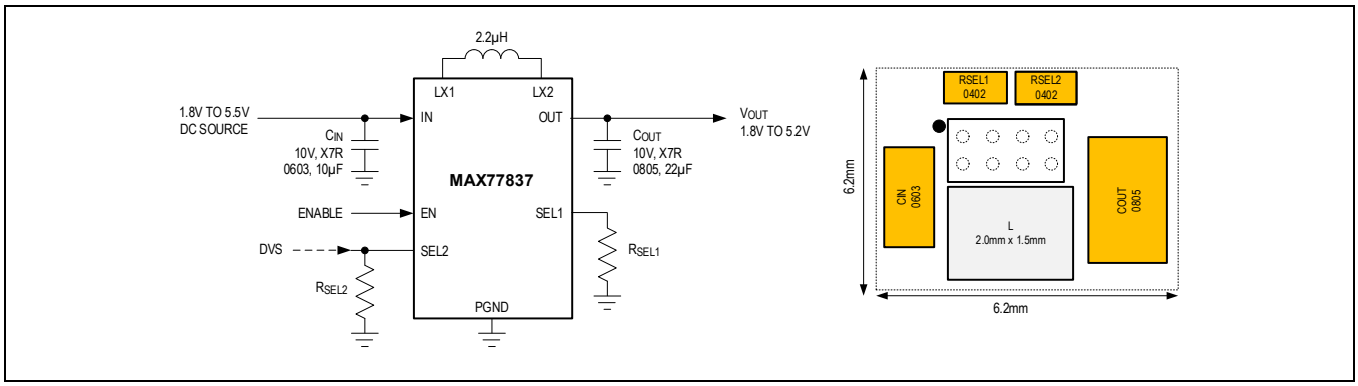
- 1.8V to 5.5V Input Voltage
- Output Voltages Combination from 1.8V to 5.2V
- Peak Efficiency of 95% (5.5$V_{IN}$, 3.8$V_{OUT}$)
- 430nA Typical Quiescent current
- 10nA Shutdown Current
- $R_{SEL}$ Configurations
  - OUT1 and OUT2
  - 1.05A or 0.4A Switch Current Limit
  - DVS Function On or Off
  - Hiccup or Latch-Off Mode
- Protections Features
  - Input Undervoltage Lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal Shutdown
- 1.84mm x 1.03mm, 8-Bump WLP
- 2.5mm x 2.0mm, 8-Lead FC2QFN

## Applications

- LPWAN SoC Companion Power Solution
- IoT and Wearable Applications
- Asset Trackers
- Smart Meters

***Ordering Information* appears at end of the data sheet**

## Simplified Application Circuit




*19-101627; Rev 0; 2/23*

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## Absolute Maximum Ratings

IN, OUT, LX1, LX2, EN, SEL1, SEL2 to GND....-0.3V to +6.0V

Continuous Power Dissipation for WLP package ($T_A$ = +70°C (Derate 13.55mW/°C above +70°C) (Note 1))..... 1084mW

Junction Temperature ..... -40°C to +150°C

Storage Temperature..... -65°C to +150°C

Soldering Temperature (reflow)..... +260°C

**Note 1:** Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

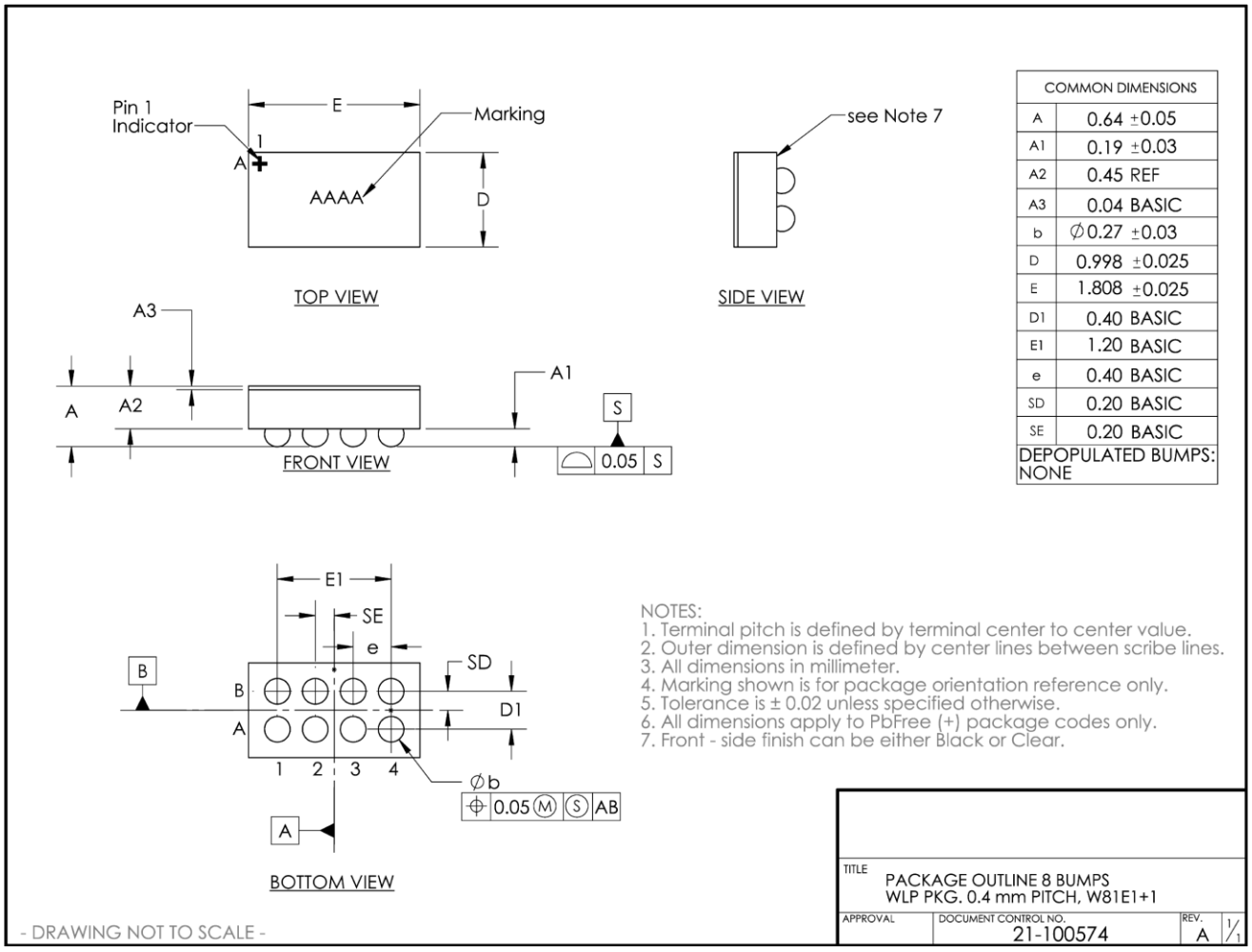
## Recommended Operating Conditions

| PARAMETER | SYMBOL | TYPICAL RANGE |
|---|---|---|
| Input Voltage Range | $V_{IN}$ | 1.8V to 5.5V |
| Switch Current Limit | $I_{LIM}$ | 0mA to 1050mA |
| Operating Junction Temperature | $t_J$ | -40°C to +125°C |

## Package Information

### WLP

| | |
|---|---|
| Package Code | W81E1+1 |
| Outline Number | *21-100574* |
| Land Pattern Number | Refer to *Application Note 1891* |
| **Thermal Resistance, Four-Layer Board** | |
| Junction-to-Ambient ($\theta_{JA}$) | 73.8°C/W |




Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *http://www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *http://www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

## Electrical Characteristics

($V_{IN}$ = +3.6V, $V_{OUT}$ = +3.3V. Typical values are at $T_J \approx T_A$ = +25°C. Limits are 100% tested at $T_J$ = +25°C. Limits over the operating temperature range ($T_J$ = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| Operating Voltage Range | $V_{IN}$ | | 1.8 | | 5.5 | V |
| Input Undervoltage Lockout | $V_{UVLO\_R}$ | $V_{IN}$ rising | 1.7 | 1.75 | 1.8 | V |
| UVLO Hysteresis | $V_{UVLO\_HYS}$ | $V_{UVLO\_R} - V_{UVLO\_F}$ | | 60 | | mV |
| Shutdown Supply Current | $I_{SHDN}$ | $V_{EN}$ = 0V, $T_J$ = +25°C | | 10 | 100 | nA |
| Input Quiescent Current | $I_Q$ | $V_{EN} = V_{IN}$, no switching, $T_J$ = +25°C | | 430 | 930 | nA |

($V_{IN}$ = +3.6V, $V_{OUT}$ = +3.3V. Typical values are at $T_J \approx T_A$ = +25°C. Limits are 100% tested at $T_J$ = +25°C. Limits over the operating temperature range ($T_J$ = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **OUTPUT VOLTAGE** | | | | | | | |
| Output Voltage Range | $V_{OUT}$ | | | 1.8 | | 5.2 | V |
| Output Voltage Accuracy | $V_{OUT\_ACC}$ | In CCM, $T_J$ = -40°C to +125°C | | -2 | | +2 | % |
| | | Skip mode at $T_J$ = +25°C | | -1.0 | | +4.0 | |
| **EN LOGIC LEVEL** | | | | | | | |
| Input LOW Level | $V_{IL}$ | | | | | 0.4 | V |
| Input HIGH Level | $V_{IH}$ | | | 1.2 | | | V |
| **THERMAL PROTECTION** | | | | | | | |
| Thermal Shutdown Threshold | $T_{SHDN\_R}$ | $T_J$ rising (Note 3) | | | 165 | | °C |
| Thermal Shutdown Hysteresis | $T_{SHDN\_HYS}$ | $T_{SHDN\_R} - T_{SHDN\_F}$ (Note 3) | | | 20 | | °C |
| **BUCK-BOOST REGULATOR** | | | | | | | |
| Startup Delay Time | $t_{DLY\_EN}$ | Delay from rising edge of EN signal to start of $V_{OUT}$ ramp (Note 2) | | | 1.6 | | ms |
| SEL2 Logic Input Debounce Time | $t_{SEL2\_DEB}$ | Minimum time SEL2 pin must be High/Low for $V_{OUT}$ to respond | | 40 | 50 | 60 | µs |
| Soft Start Slew Rate | $\Delta V_{OUT}/\Delta t$ | | | | 2 | | V/ms |
| Soft Start Switch Current Limit | $I_{LIM\_SS}$ | $V_{IN}$ = 1.8V to 3.6V (Note 3) | Low $I_{LIM}$ setting | | 200 | | mA |
| | | $V_{IN}$ = 2.3V to 5.5V (Note 3) | High $I_{LIM}$ setting | | 525 | | |
| High Side Switch Current Limit | $I_{LIM}$ | $V_{IN}$ = 1.8V to 3.6V | Low $I_{LIM}$ setting | 300 | 400 | 500 | mA |
| | | $V_{IN}$ = 2.3V to 5.5V | High $I_{LIM}$ setting | 900 | 1050 | 1200 | |
| High Side Switch On Resistance | $R_{DSON\_HS}$ | $I_{LX}$ = +180mA | | | 150 | | mΩ |
| Low side Switch On Resistance | $R_{DSON\_LS}$ | $I_{LX}$ = -180mA | | | 150 | | mΩ |
| Line Regulation | $\Delta V/V_{OUT}$ | $V_{IN}$ = 1.8V to 5.5V, $I_{OUT}$ = 300mA | | -1.1 | | +1.1 | % |
| Load Regulation | $\Delta V/V_{OUT}$ | $V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 35mA to Max Load | | | -1.5 | | % |
| Output Active Discharge Resistance | $R_{DISCHG}$ | $V_{EN} < V_{IL}$ or $V_{IN} < V_{UVLO\_F}$ | | | 100 | | Ω |
| Minimum Effective Output Capacitance | $C_{EFF(Min)}$ | | | | 2.2 | | µF |

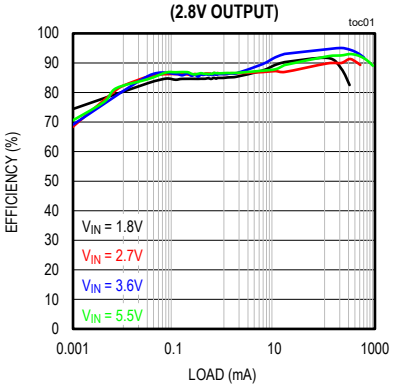
**Note 2:** Guaranteed by design. Not production tested.

**Note 3:** Characterized by ATE or bench test, not production tested.

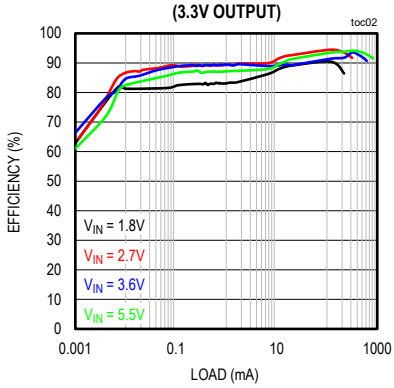
## Typical Operating Characteristics

($V_{IN}$ = 3.6V, $V_{OUT}$ = 3.3V, L = 2.2µH (CIGT201610EH2R2MN), $C_{OUT}$ = 22µF, $I_{LIM}$ = 1050mA, $T_A$ = +25°C unless otherwise noted.
**Note 4:** Measurement limited by switching current limit. Actual maximum output current depends on system thermal performance.)

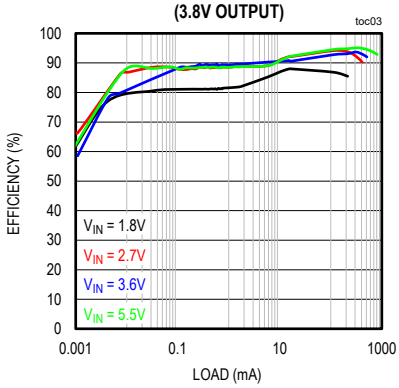
EFFICIENCY vs. LOAD (2.8V OUTPUT)



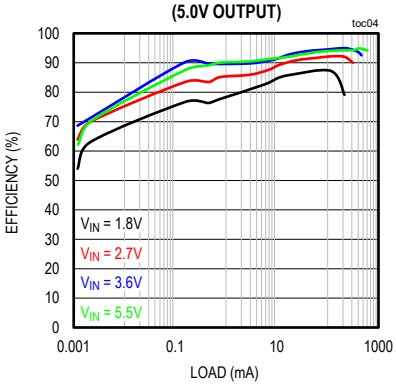

EFFICIENCY vs. LOAD (3.3V OUTPUT)



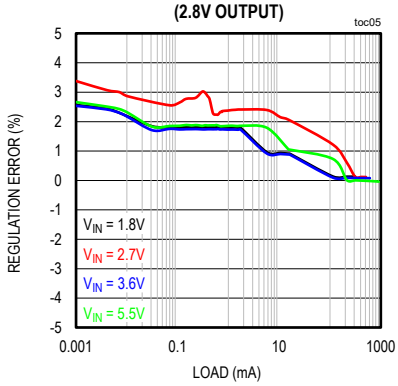

EFFICIENCY vs. LOAD (3.8V OUTPUT)




EFFICIENCY vs. LOAD (5.0V OUTPUT)




LOAD REGULATION (2.8V OUTPUT)

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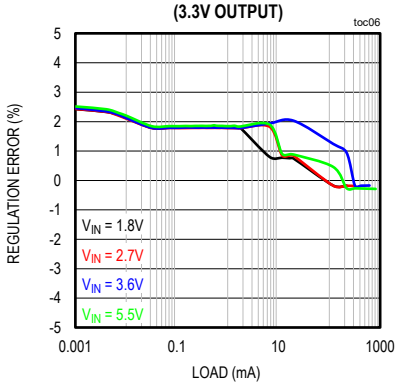


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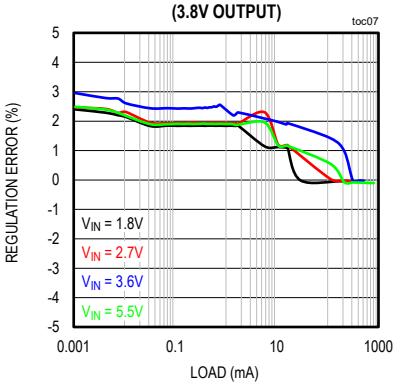


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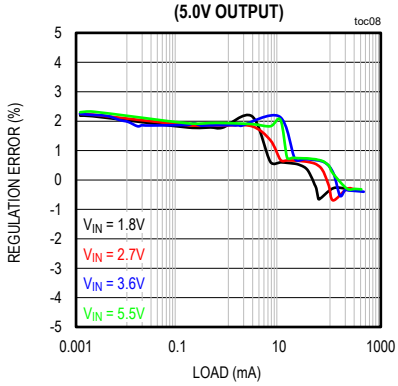
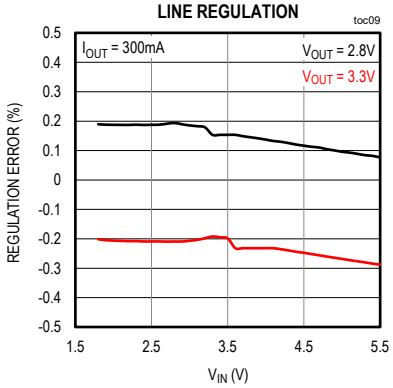



LINE REGULATION



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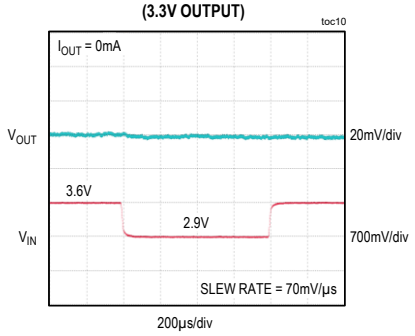
**LINE TRANSIENT RESPONSE (3.3V OUTPUT)**

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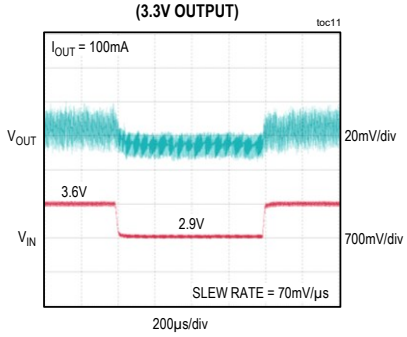


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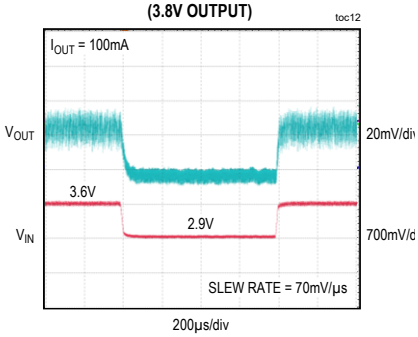


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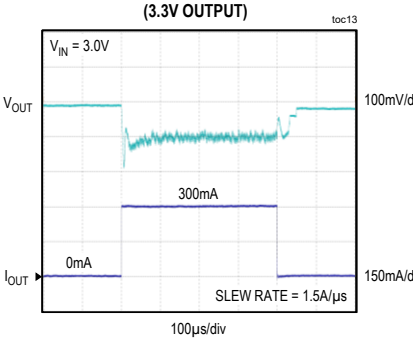


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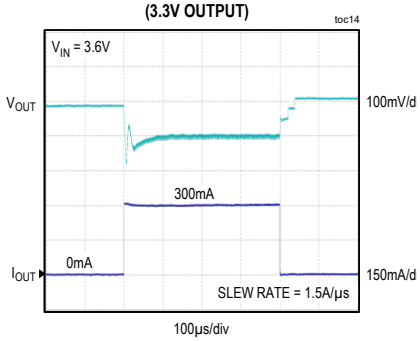
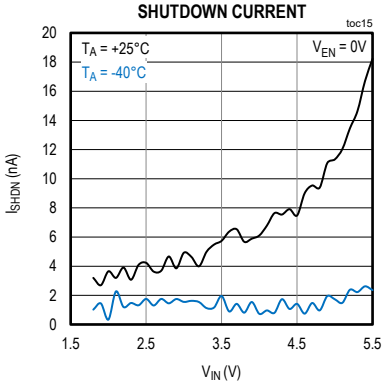
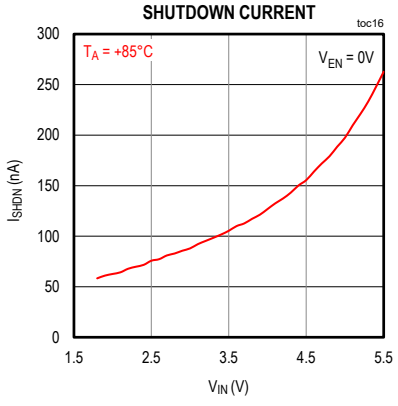


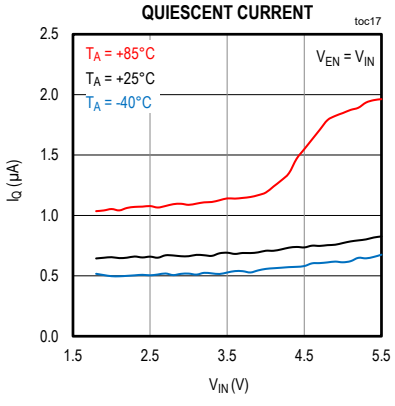

**SHUTDOWN CURRENT**



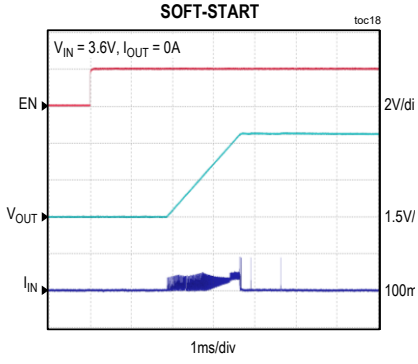

**SHUTDOWN CURRENT**




**QUIESCENT CURRENT**




**SOFT-START**



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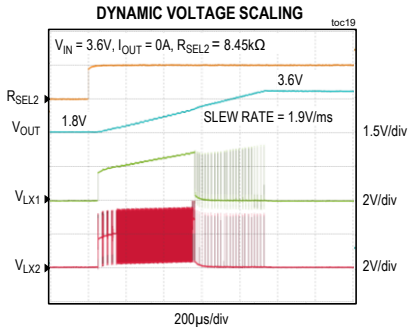


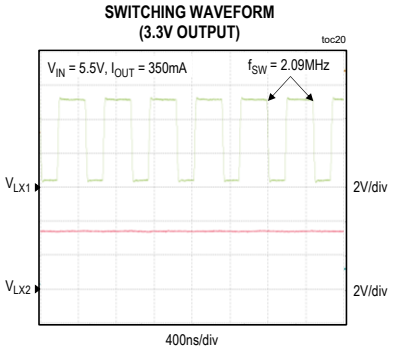


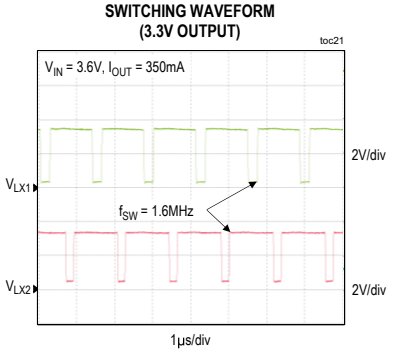


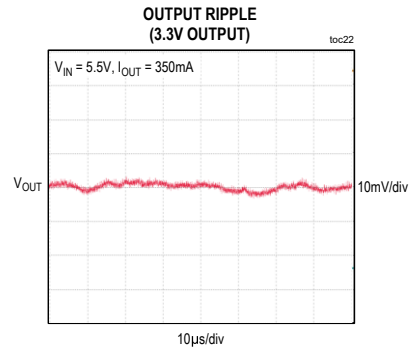


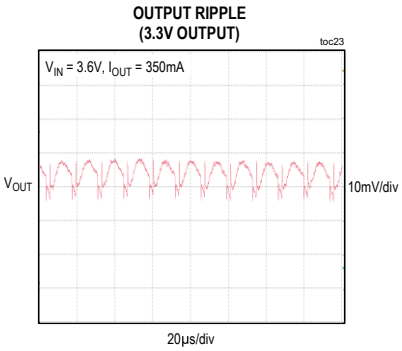


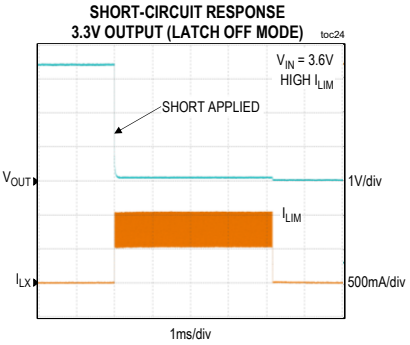


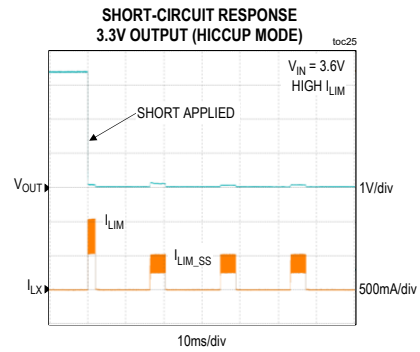


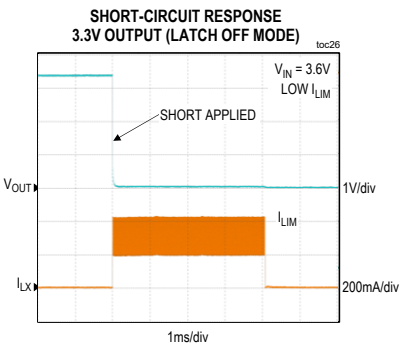


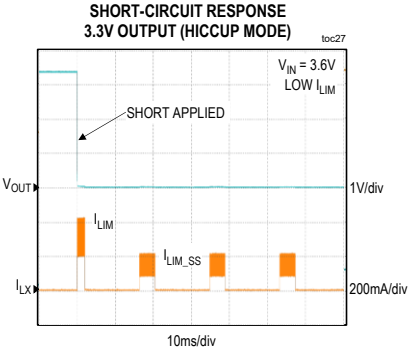

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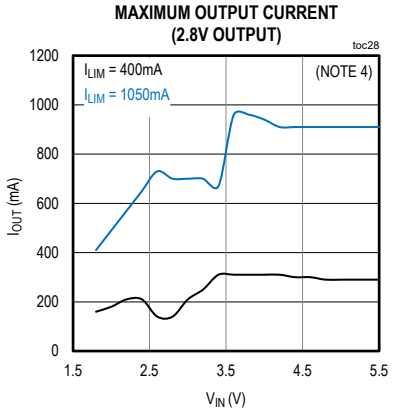
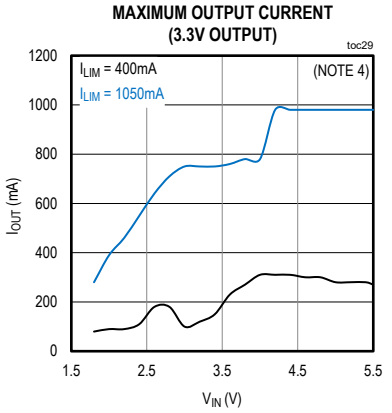
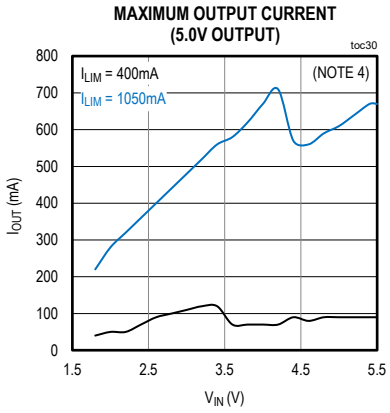
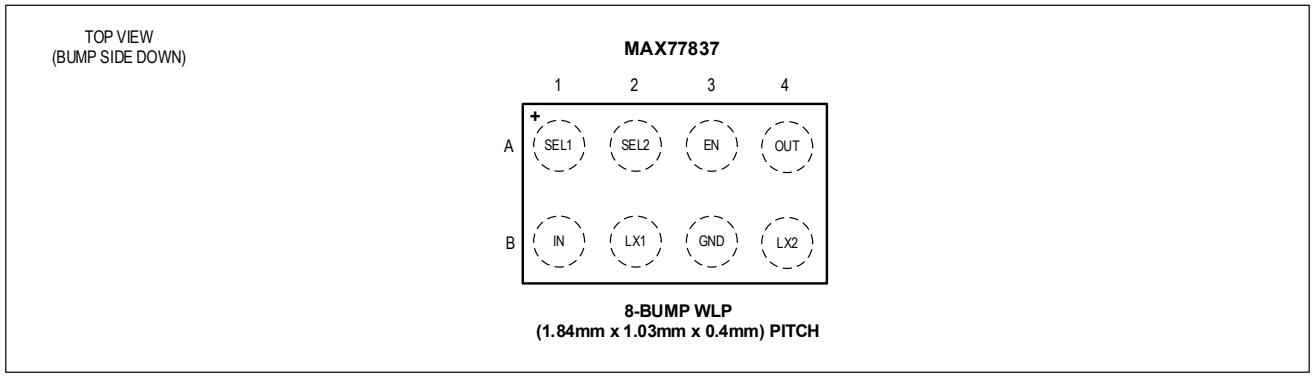



## Pin Configurations

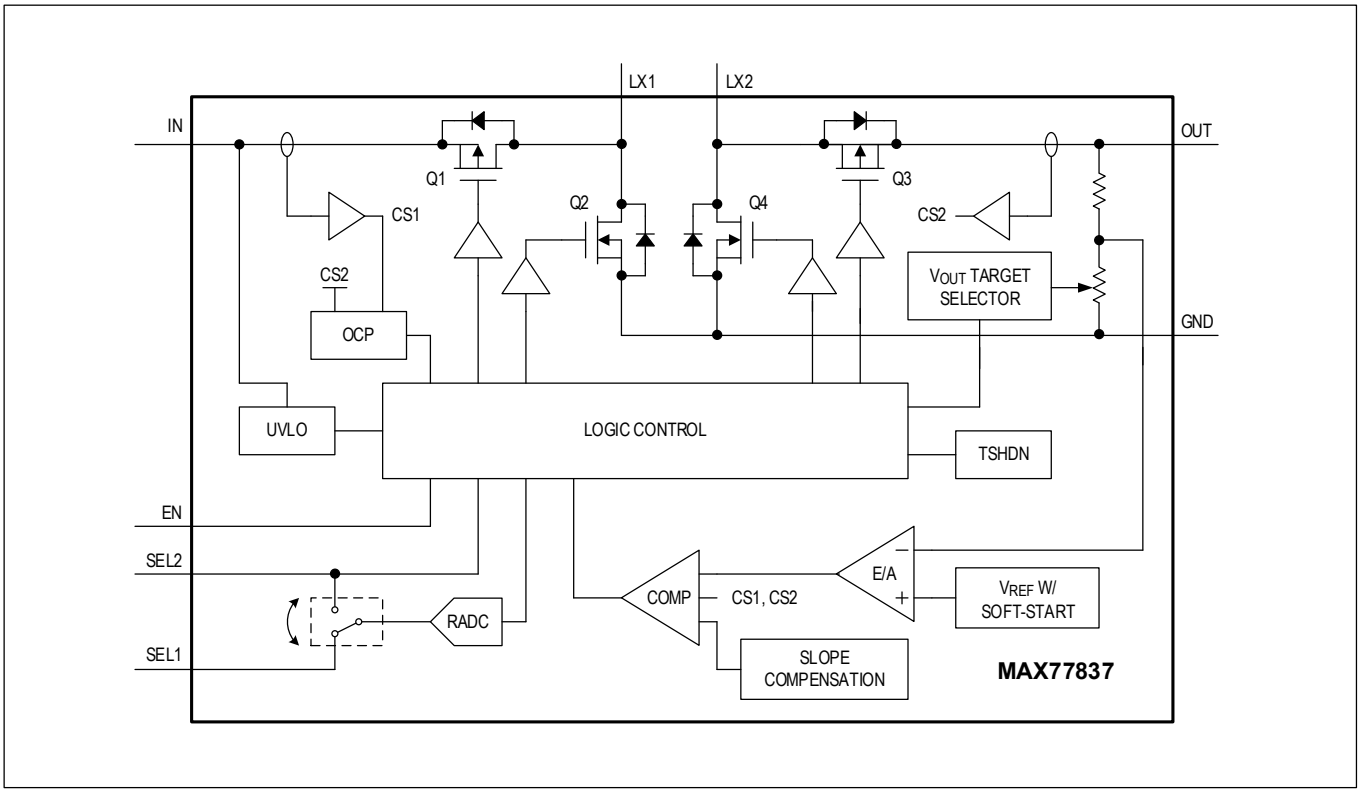
**8 WLP**




## Pin Descriptions

| PIN | NAME | FUNCTION | TYPE |
|---|---|---|---|
| A1 | SEL1 | Configuration Selection. Connect a resistor between SEL1 and GND. See *Table 1* for resistor values and configurations. | Analog |
| A2 | SEL2 | Configuration Selection. Connect a resistor between SEL2 and GND. See *Table 2* for resistor values and configurations. | Analog |
| A3 | EN | Active-High Buck-Boost Enable Input. | Digital |
| A4 | OUT | Buck-Boost Output. Bypass to GND with 10V 22µF ceramic capacitor. | Power |
| B1 | IN | Buck-Boost Input. Bypass to GND with 10V 10µF ceramic capacitor. | Power |
| B2 | LX1 | Buck-Boost Switching Node 1. | Power |
| B3 | GND | Ground Pin. Use this pin as both the power and analog ground. | Ground |
| B4 | LX2 | Buck-Boost Switching Node 2. | Power |

## Functional Block Diagram



# Detailed Description

## General Description

The MAX77837 is a nano power buck-boost with ultra-low quiescent current (430nA typical) and high efficiency with an input range of 1.8V to 5.5V. The IC is ideal for either Li-ion/Li-Poly or double alkaline battery-powered applications which require long standby/idling time with short working time, such as asset tracking devices or door-lock devices. The IC operates in Low-Power Mode (LPM), Skip Mode, or CCM mode, depending on operating conditions to optimize the efficiency.

Use the resistor between the SEL1 pin and GND ($R_{SEL1}$) to select two output voltage levels (OUT1 and OUT2) within a range of 1.8V to 5.2V. The IC can start up into either OUT1 or OUT2 by changing the value of the resistor at SEL2.

Use the resistor between the SEL2 pin and GND ($R_{SEL2}$) to set the following:

- Switch current limit (1050mA and 400mA)
- Hiccup or Latch Off Mode
- DVS Function (On/Off)
- Startup Voltage (OUT1 or OUT2).

See the *SEL Pin Configuration* section for more information. Use the SEL2 pin changes into a logic input pin for the Dynamic Voltage Scaling (DVS) function after soft-start, and the DVS function to change the output voltage from the startup voltage (OUT1) to OUT2 without powering down the part (DVS function is disabled when the startup voltage is OUT2). The DVS function can only ramp up the output voltage. When a DVS is applied to bring $V_{OUT}$ down, the part stops switching, waits for the output voltage to reach the lower target value (due to load or leakage) and starts operating after it reaches the target. See the *Dynamic Voltage Scaling (DVS)* section for more information.

The MAX77837 is equipped with a thermal shutdown and cycle-by-cycle switch current limit to protect the system and the device.

## Start-Up

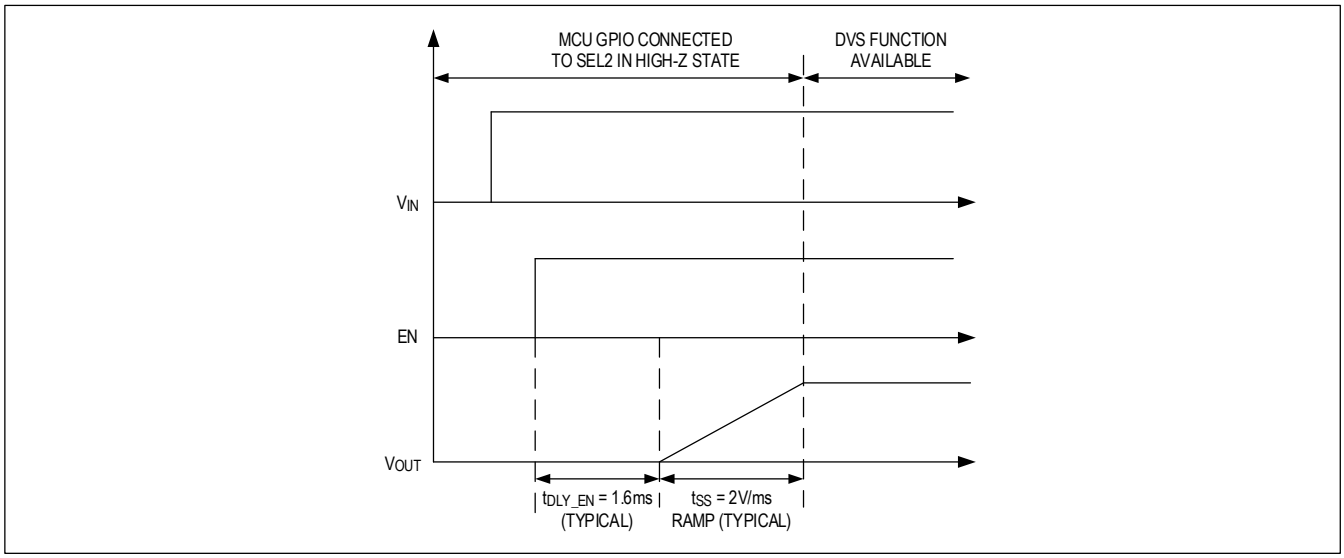



*Figure 1. Startup Behavior*

See *Figure 1* for The start-up behavior. When EN goes logic HIGH and $V_{IN} > V_{UVLO\_R}$, IC starts up by turning on the bias circuits, after which the resistance value at the two SEL pins is read sequentially. The IC typically takes 1.6ms (Start-up delay time) after the rising edge of the EN signal to start the soft-start process.

During soft-start, output voltage ramps with a slew rate of 2V/ms (typical). The IC limits the switch current limit during soft-start to 50% of the set value. When the output voltage reaches the target value, the soft-start is complete, and the switch current limit level is increased to the normal level. The soft-start function helps prevent the IC from drawing too much current from the system during startup.

If the IC sees output voltage below the output short protection threshold level of 1V (typical), for 4ms (typical) after the rising edge of enable signal and startup delay time, then the output of the regulator is disabled and depending on the protection mode selection, the device either latches off or auto-restarts the output. Recovering from latch-off requires toggling the EN pin or the recycling power supply after removing the faulty condition.

## Dynamic Voltage Scaling (DVS)

The MAX77837 allows the user to change the output voltage without powering the part down using the DVS function. The DVS function can be enabled or disabled by selecting an appropriate resistor between SEL2 and GND.

The resistor between SEL1 and GND ($R_{SEL1}$) is used to select a pair of output voltage levels (OUT1 and OUT2). See *Table 1* to select the appropriate resistors for the application. The startup voltage (OUT1 or OUT2) is set by selecting the appropriate resistor between SEL2 and GND ($R_{SEL2}$). If the startup voltage is selected as OUT2, the DVS function is disabled. The IC regulates to OUT1 or OUT2 (according to the value of $R_{SEL2}$) after the soft-start.

After the soft-start is complete, the SEL2 pin turns into a logic input pin. If the SEL2 pin is pulled high, the IC changes the regulated output voltage from OUT1 to OUT2. If the SEL2 pin is pulled LOW, the IC changes the regulated output voltage from OUT2 to OUT1. See *Table 1* and *Table 2* to select the appropriate resistors for the application.

The DVS function ramps up the reference voltage at 2V/ms (typical) when the output voltage is changed from a lower to a higher value, but when the output voltage is changed from a higher value to a lower value using the DVS function, there is no slew down control, and the part resumes switching after the output voltage reaches the lower value (due to load or leakage). See *Figure 2* for more information.

The DVS function is activated only after soft-start is complete. Applying logic voltage to the SEL2 pin for DVS control before soft-start is complete is not allowed. The MCU GPIO pin connected to SEL2 must be in a High-Z state before the soft-start is complete.

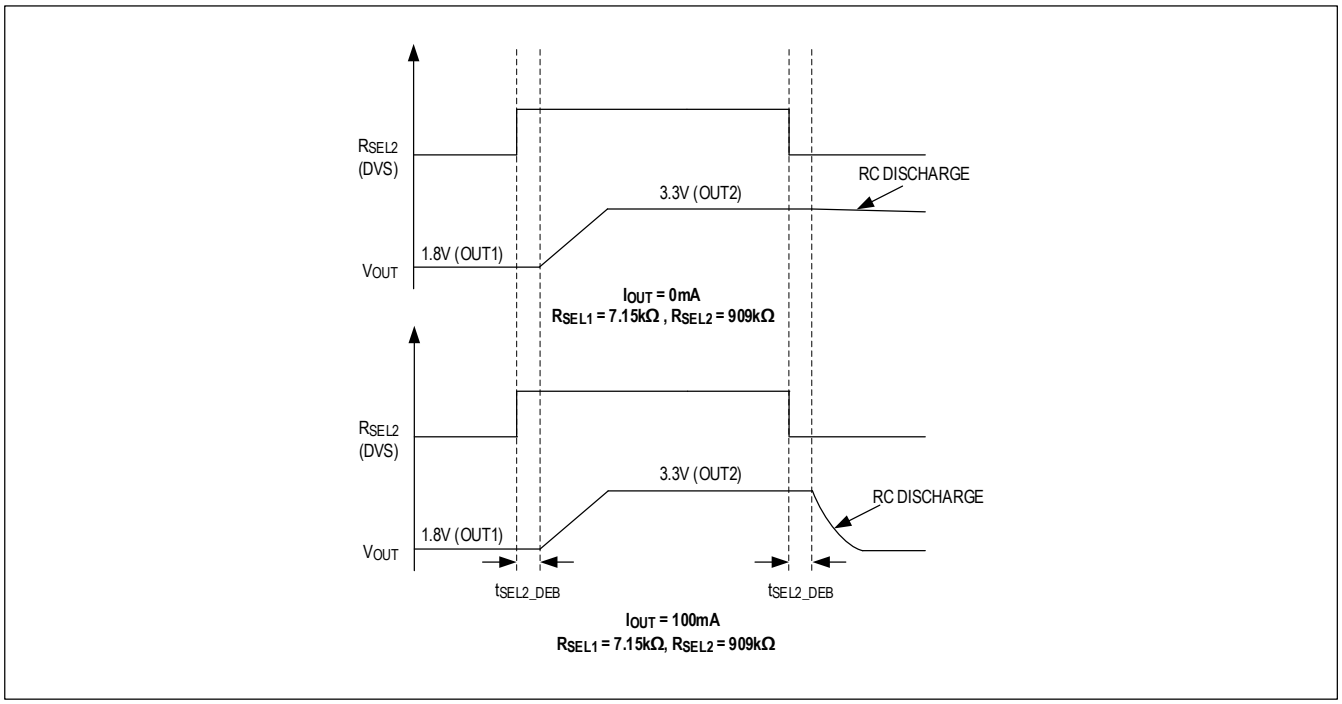



*Figure 2. Dynamic Voltage Scaling (DVS)*

## Buck-Boost Control Scheme

The buck-boost converter operates using adaptive on time current-mode control. The buck-boost utilizes an H-bridge topology to regulate the output voltage using a single inductor and output capacitor.

The H-bridge topology has three switching phases. See *Figure 2* for details.

- Φ1 Switch period (Phase 1: HS1 = ON, LS2 = ON) stores energy in the inductor. Inductor current ramps up at a rate proportional to the input voltage divided by inductance: $V_{IN}/L$.
- Φ2 Switch period (Phase 2: HS1 = ON, HS2 = ON) ramps inductor current up or down depending on the differential voltage across the inductor: $(V_{IN} – V_{OUT})/L$.
- Φ3 Switch period (Phase 3: LS1 = ON, HS2 = ON) ramps inductor current down at a rate proportional to the output voltage divided by inductance: $(-V_{OUT}/L)$.

Boost operation ($V_{IN} < V_{OUT}$) utilizes Φ1 and Φ2 within one cycle to bring the voltage within regulation. See the representation of the inductor current waveform for boost mode operation in *Figure 2*.

Buck operation ($V_{IN} > V_{OUT}$) utilizes Φ2 and Φ3 within one cycle to bring the voltage within regulation. See the representation of the inductor current waveform for buck mode operation in *Figure 2*.

Three-phase operation ($V_{IN}$ close to $V_{OUT}$) utilizes Φ1 till the inductor current reaches a certain level, Φ2 is triggered for pre-configured on time, and then Φ3 is triggered till the current reaches zero. Three-phase operation is utilized only in Skip Mode. See the representation of the inductor current waveform for the three-phase mode operation in *Figure 2*.

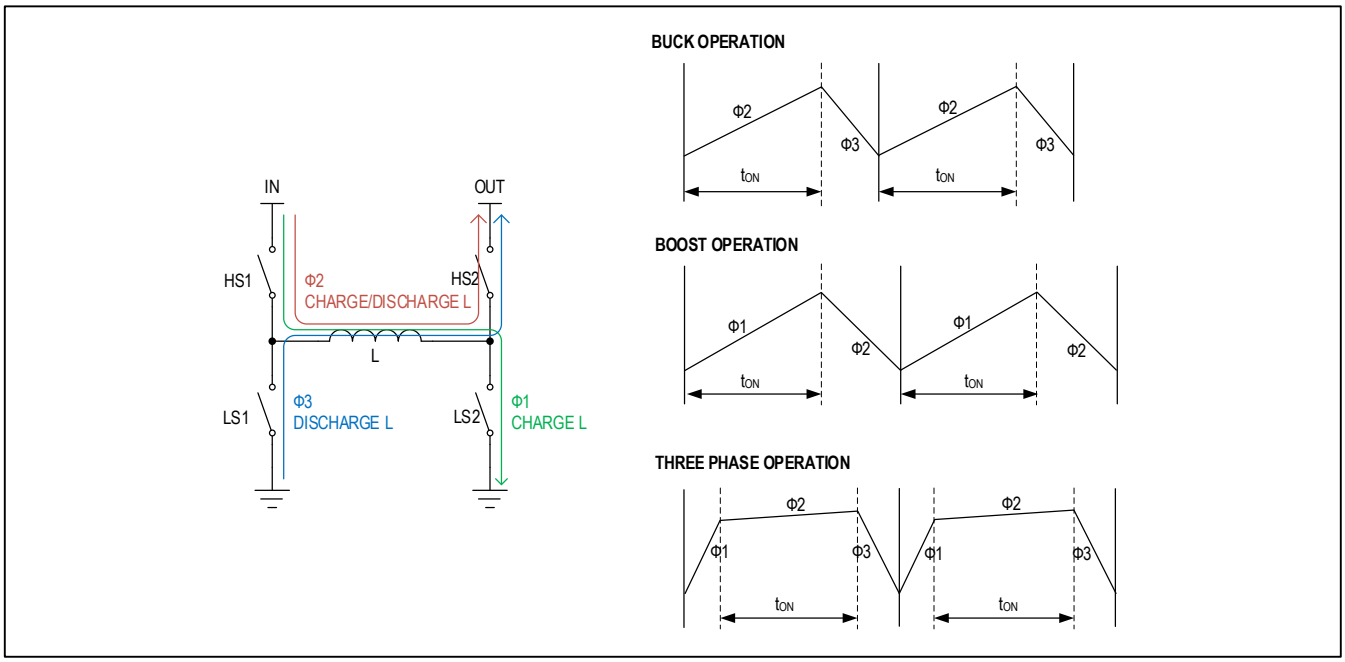



*Figure 3. Buck-Boost H-Bridge Topology*

## Low-Power Mode

The MAX77837 automatically enters a low-power mode (LPM) when the load current is very low to achieve high efficiency at light loads. The error amplifier and other internal blocks are deactivated in this mode to lower $I_Q$ consumption. A low-power voltage comparator is used to monitor the output voltage in LPM.

When the load current reduces and the switching frequency falls to $f_{MIN}$ (58kHz typical), the part switches at $f_{MIN}$ till the output voltage reaches above 3% of the output voltage target. After the output voltage crosses this level, the part is in LPM. In low-power mode, the IC generates an on-time of predetermined length when the output voltage reaches 3% above the output voltage target. When the load is increased, the IC must switch at a higher frequency to service the load, and when the switching frequency reaches $f_{MIN}$, the part switches at $f_{MIN}$ till the output voltage falls to the target voltage. The target voltage is set to 1% above the output voltage target if the part enters Skip Mode. See *Figure 4* for more information.

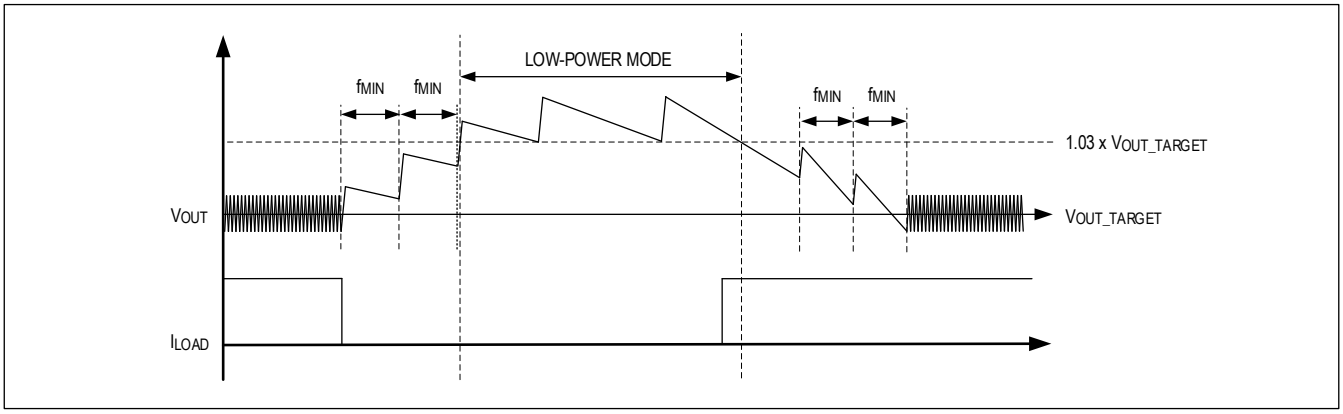



*Figure 4. Low-power Mode Operation*

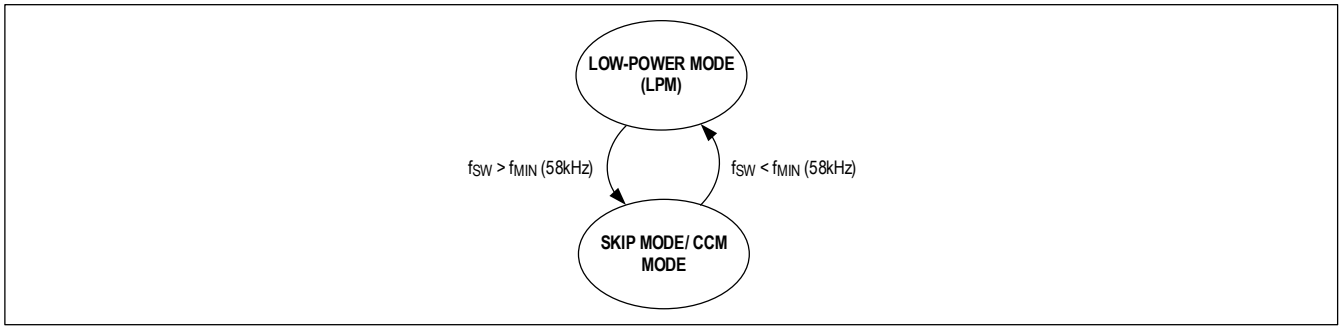



*Figure 5. Low-power Mode to Skip/CCM Transition*

## Skip Mode and CCM Mode

When the load is high enough, and the switching frequency is higher than $f_{MIN}$ (58kHz typical), the part exits low-power mode and enters Skip Mode. In the Skip mode of operation, an on-time of predetermined length is triggered when the output voltage reaches 1% higher than the target value. During the Skip Mode of operation, the negative inductor current is prevented by turning off the FETs after the inductor current crosses 0A.

At higher output load currents, when the inductor current does not have zero crossing, the part enters CCM Mode, which operates using adaptive on-time control. The IC regulates to target voltage during the CCM mode of operation.

## Shutdown Conditions

When the part enters Shutdown mode, the buck-boost regulator turns off. The IC has a few shutdown conditions to protect itself and the system from fault and to allow the user to turn off the part when required. These conditions are listed below:

- Enable: $V_{EN} < V_{IH}$ (1.2V typical value)
- Input UVLO: $V_{IN}$ < Input UVLO Threshold (1.75V typical value)
- Thermal Shutdown: $t_J$ > Thermal Shutdown Rising Temperature (165°C typical value)
- Overcurrent Protection: $V_{OUT}$ < Short-Circuit Protection Threshold Level (1V typical) after soft-start or High-Side switching current > High-side switching current limit ($I_{LIM}$) for 4ms (In Latch-Off Mode) or 2ms (In Auto-restart Mode) the IC enters latch-off or Auto-restart mode depending on the resistor between SEL2 and GND. See the *Switching Current Limit* section for more information.

## Thermal Shutdown

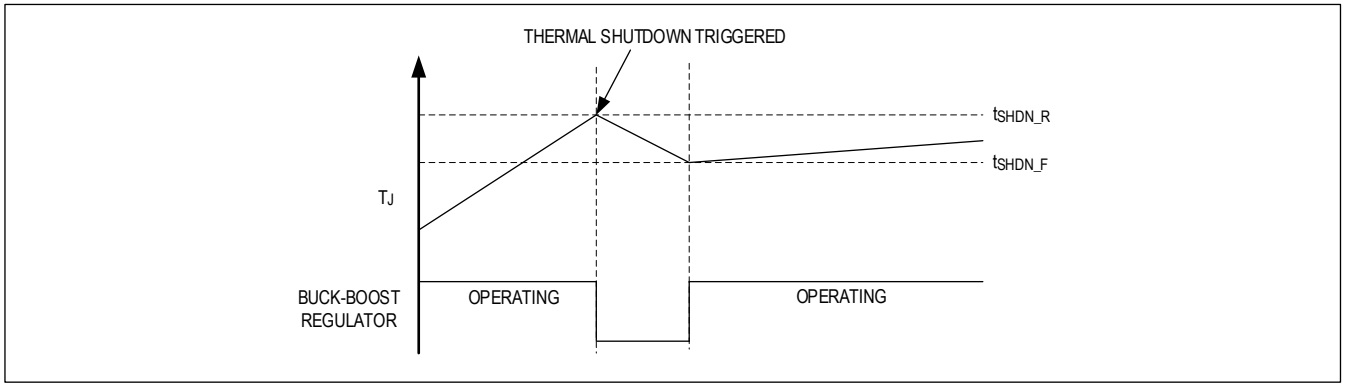



*Figure 6. Thermal Shutdown Recovery*

When junction temperature exceeds $t_{SHDN\_R}$ (165°C typical value), thermal protection of the MAX77837 is triggered. Then, the Buck-Boost converter output is disabled until the junction temperature drops below thermal protection falling threshold level $t_{SHDN\_F}$ (145°C typical) after which the part starts up again, as shown in *Figure 6*.

## Undervoltage Lockout

When $V_{IN}$ falls below $V_{UVLO\_F}$ (1.7V typical), the buck-boost regulator is disabled, all registers are reset, and active discharge is enabled. The IC is ready to restart only when the $V_{IN}$ rises above $V_{UVLO\_R}$ (1.75V typical value).

## Switching Current Limit

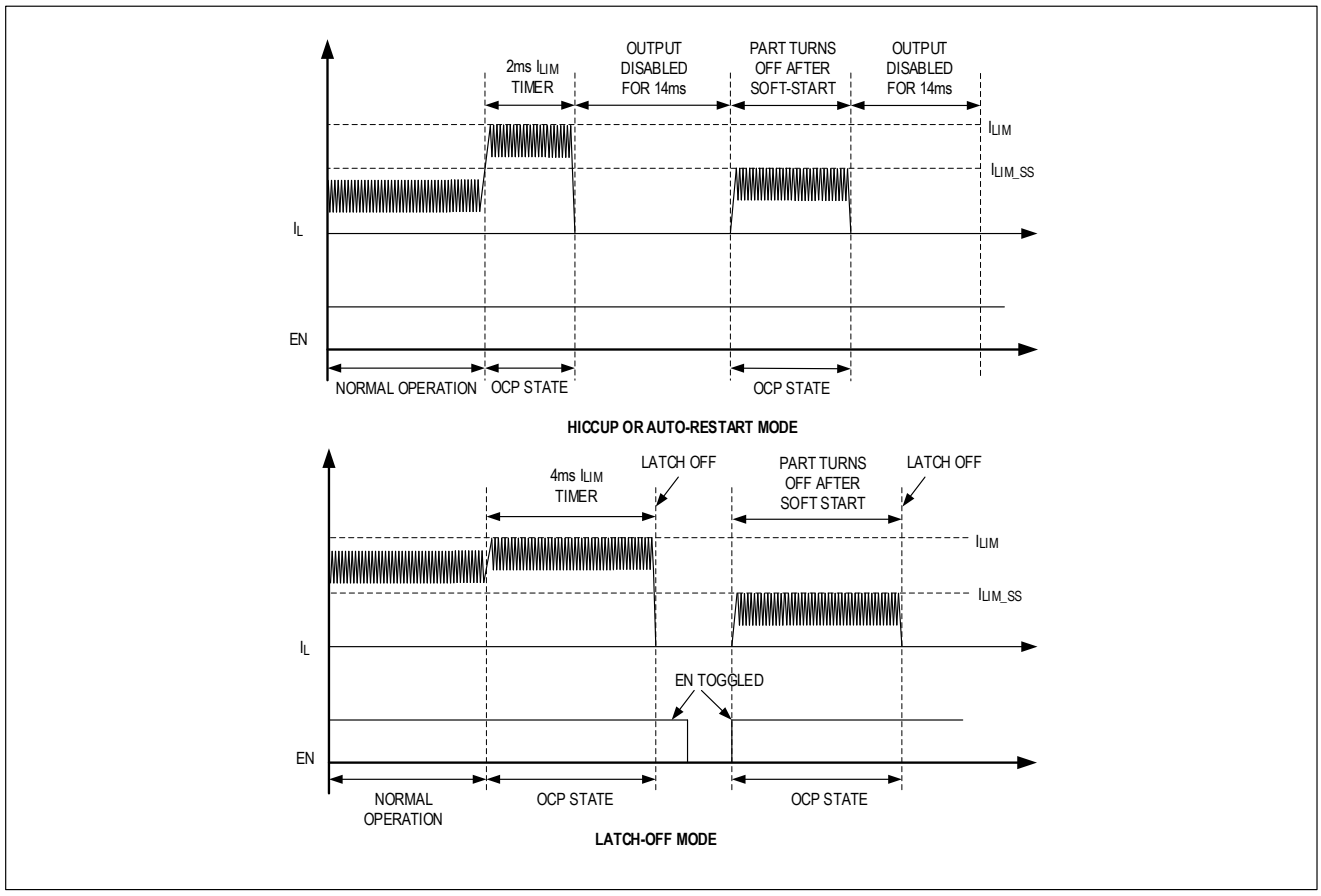



*Figure 7. Overcurrent Protection in Latch-off and Hiccup Mode*

The MAX77837 provides a cycle-by-cycle switch current limit to protect the IC and the system. The IC senses the peak switch current of high side switches during the on time, and when the peak current reaches the $I_{LIM}$ threshold level, the switches for the charging phase are turned off, and the switches used to discharge the inductor current are turned on for the rest of the cycle. The IC supports two switching current limits 400mA (Lower Limit), and 1050mA (Higher Limit) which can be set using $R_{SEL2}$. For more information, see *SEL Pin Configuration*.

After soft-start, when the IC is set to auto-restart mode using $R_{SEL2}$, and the device sees $I_{LIM}$ for 2ms (typical), the device will disable the output for 14ms (typical) and re-start the output. With $R_{SEL2}$ setting for Latch off, after soft-start, the IC latches off after seeing an $I_{LIM}$ continuously for 4ms (typical). When the IC is latched off, the EN signal needs to be toggled or $V_{IN}$ voltage recycled to recover from the latch-off status. See *Figure 7* for more information regarding overcurrent protection.

### Active Discharge

When the EN pin is set to LOW or $V_{IN}$ <$V_{UVLO\_F}$, the MAX77837 stops switching and turns on an internal switch of 100Ω that provides a path to discharge the energy stored in the output capacitor to GND.

### SEL Pin Configuration

MAX77837 has two hardware configuration pins (SEL1 and SEL2) to configure the part's features. A resistor between SEL1 and ground ($R_{SEL1}$) is used to select two output voltage levels (OUT1 and OUT2). A resistor between SEL2 and ground ($R_{SEL2}$) is used to select the startup output voltage, switch current limit and protection mode, and enable/disable the DVS function. See *Table 1* for more information regarding the $R_{SEL1}$ value selection. *Table 2* lists $R_{SEL2}$ values to configure each of the previously mentioned settings. If the user requires OUT2 as the startup voltage, the part can only be operated with DVS disabled and in Auto-Restart Mode.

When $R_{SEL2}$ enables DVS, the SEL2 pin is configured as logic control input for the DVS function after soft-start. When SEL2 is pulled HIGH, the output voltage is switched from OUT1 to OUT2, and when SEL2 goes LOW, the output voltage is switched from OUT2 to OUT1. The SEL2 pin should be in a High-Z state during and before the soft-start. The DVS function can only ramp up the output voltage level. There is no slew-down control when the DVS function is used to transition from a higher output voltage to a lower output voltage. The IC changes the reference voltage and waits till load or leakage current brings the output voltage to the lower value, then starts operating normally. See the *Dynamic Voltage Setting* section for more information.

## Table 1. $R_{SEL1}$ Selection Table

| $R_{SEL1}$ (kΩ) | OUT1 (V) | OUT2 (V) | $R_{SEL1}$ (kΩ) | OUT1 (V) | OUT2 (V) |
|---|---|---|---|---|---|
| 4.99 | 1.8 | 2.5 | 66.5 | 3.3 | 3.8 |
| 5.90 | 1.8 | 2.8 | 80.6 | 3.3 | 5.0 |
| 7.15 | 1.8 | 3.3 | 95.3 | 3.6 | 2.8 |
| 8.45 | 1.8 | 3.6 | 113 | 3.6 | 3.3 |
| 10.0 | 2.5 | 1.8 | 133 | 3.6 | 5.0 |
| 11.8 | 2.5 | 2.8 | 162 | 3.6 | 5.2 |
| 14.0 | 2.5 | 3.3 | 191 | 3.8 | 3.3 |
| 16.9 | 2.5 | 3.6 | 226 | 3.8 | 3.6 |
| 20.0 | 2.8 | 1.8 | 267 | 3.8 | 5.0 |
| 23.7 | 2.8 | 2.5 | 324 | 5.0 | 3.3 |
| 28.0 | 2.8 | 3.3 | 383 | 5.2 | 3.3 |
| 34.0 | 2.8 | 3.6 | 453 | 2.1 | 2.3 |
| 40.2 | 3.3 | 1.8 | 536 | RESERVED | RESERVED |
| 47.5 | 3.3 | 2.5 | 634 | RESERVED | RESERVED |
| 56.2 | 3.3 | 2.8 | 768 | RESERVED | RESERVED |
| Short | 3.3 | 3.6 | 909/OPEN | RESERVED | RESERVED |

## Table 2. $R_{SEL2}$ Selection Table

| $R_{SEL2}$ (kΩ) | DVS | PROTECTION | $I_{LIM}$ (mA) | STARTUP VOLTAGE |
|---|---|---|---|---|
| 226 | Disabled | Hiccup/ Auto-Restart | 1050 | OUT2 |
| 267 | Disabled | Hiccup/ Auto-Restart | 400 | OUT2 |
| 324 | | | 1050 | OUT1 |
| 383 | | Latch Off | 400 | OUT1 |
| 453 | | | 1050 | OUT1 |
| 536 | Enabled | Hiccup/ Auto-Restart | 400 | OUT1 |
| 634 | | | 1050 | OUT1 |
| 768 | | Latch Off | 400 | OUT1 |
| 909 | | | 1050 | OUT1 |

# Applications Information

### Inductor Selection

Select an inductor with a saturation current rating ($I_{SAT}$) greater than or equal to the maximum high-side switching current limit threshold ($I_{LIM}$) setting. In general, inductors with lower saturation current and higher DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the RMS current rating ($I_{RMS}$) of the inductor (the current at which the temperature rises appreciably) based on the expected load current.

The chosen inductor value should ensure that the peak-inductor ripple current ($I_{PEAK}$) is below the $I_{LIM}$ setting so that the converter can maintain regulation. A 2.2µH inductor is recommended throughout the operating range of the converter. See *Table 3* for recommended inductors.

## Table 3. Inductor Recommendations

| VENDOR | PART NUMBER | NOMINAL INDUCTOR (µH) | TYPICAL DCR (mΩ) | $I_{SAT}$ (A) | $I_{RMS}$ (A) | DIMENSIONS L x W x H (mm) | $I_{LIM}$ (mA) |
|---|---|---|---|---|---|---|---|
| Samsung | CIGT201610EH2R2MNE | 2.2 | 87 | 2.9 | 2.5 | 2 x 1.6 x 1 | 1050 |
| Murata | DFE21CCN2R2MELL | 2.2 | 138 | 2.1 | 1.8 | 2 x 1.2 x 0.8 | 1050 |
| Taiyo Yuden | MCHK1608T2R2MKN | 2.2 | 237 | 1.8 | 1.2 | 1.6 x 0.8 x 0.8 | 400 |

### Input Capacitor Selection

For most applications, bypass IN pin with a 10V 10µF nominal ceramic input capacitor ($C_{IN}$) that maintains 3.75µF or higher effective capacitance at its working voltage. Effective $C_{IN}$ is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter but increase inrush current from the voltage supply when connected. $C_{IN}$ reduces the current peaks drawn from the input power source and reduces switching noise in the system. The ESR/ESL of $C_{IN}$ and its series PCB trace should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to the converter's switching frequency.

When selecting $C_{IN}$, pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance decreases as DC bias increases). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

## Output Capacitor Selection

Sufficient output capacitance ($C_{OUT}$) is required for the stable operation of the converter. Choose effective $C_{OUT}$ to be 2.2µF minimum. Effective $C_{OUT}$ is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase input surge currents during soft start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full load to no-load conditions. For most applications, a 10V 22µF capacitor is recommended for $C_{OUT}$.

When selecting $C_{OUT}$, to pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance decreases as DC bias increases). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

## Other Required Component Selection

The resistor between SEL pins (SEL1 and SEL2) and GND should have a tolerance of ±1% for the internal ADC to read the value accurately.

## PCB Layout Guidelines

The careful circuit board layout is critical to achieve low switching power loss and clean, stable operation.

When designing the PCB, follow these guidelines:

- Place the input capacitors ($C_{IN}$) and output capacitors ($C_{OUT}$) immediately next to the IN pin and OUT pin of the IC, respectively. Since the IC operates at a high switching frequency with a fast LX edges, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
- Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer, make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to reduce trace impedance further. Furthermore, do not make LX traces take up excessive area. The voltage on this node switches very quickly, and additional area creates more radiated emissions.
- Connect the inner GND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create GND islands, as GND islands risk interrupting the hot loops.
- Keep the power traces and load connections short and wide which is essential for high converter efficiency.
- Pay attention to ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

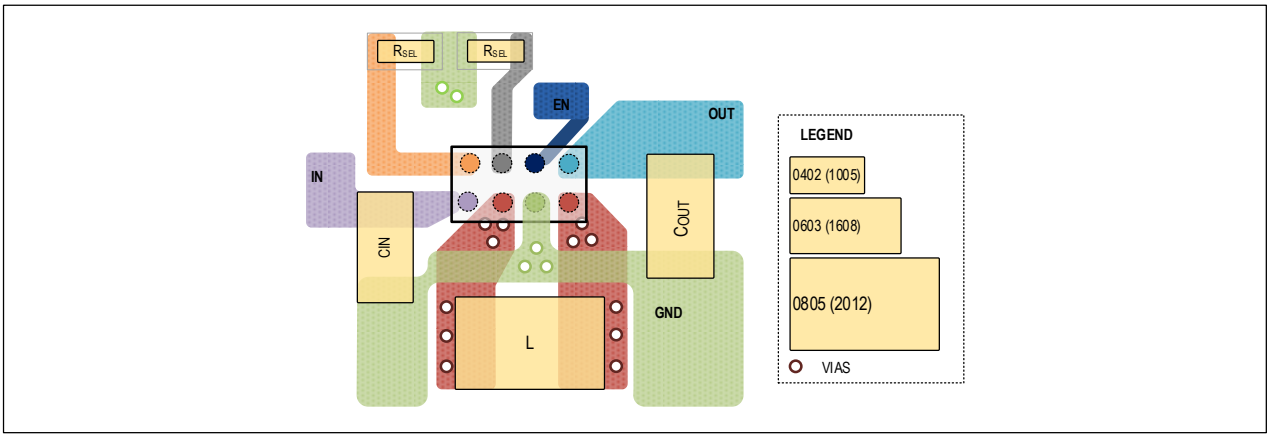


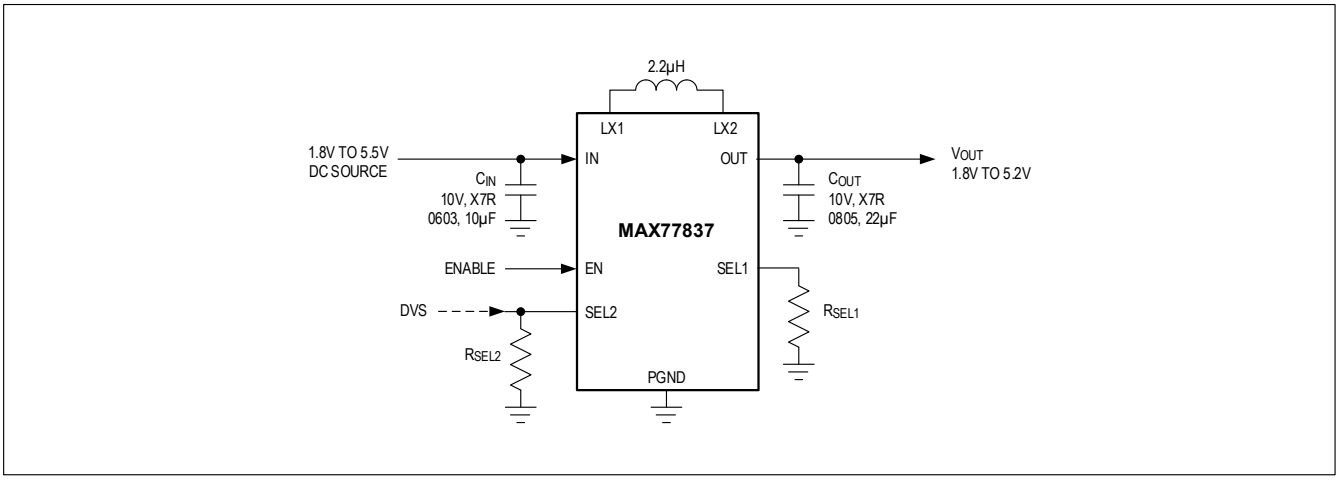

*Figure 8. PCB Layout Recommendation for WLP Package*

### Things to Avoid

Avoid using the following use cases when operating the part.

- When doing a line transient between $V_{IN}$ > $V_{OUT}$ to $V_{IN}$ < $V_{OUT}$ - 0.7V, the slew should be less than 1V/20µs (typical). For a faster transient, there is a risk of the part entering a state where it switches, even if there is no load. If the part enters this state, toggle the EN pin or power cycle $V_{IN}$ to remove this behavior. Note that this behavior does not induce any reliability issues for the part. The slew rate at the input is to be kept at less than 1V/20µs by increasing the input capacitance as required by the application.

## Typical Application Diagram




## Ordering Information

| PART NUMBER | PIN PACKAGE |
|---|---|
| MAX77837EWA+T | 8 WLP |
| MAX77837EFA+T* | 8 FC2QFN |

*+Denotes a lead (Pb)-free/RoHS-compliant package*

*T = Tape and reel*

**Future product- Contact factory for availability*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 09/21 | Initial release | — |