Click here to ask an associate for production status of specific part numbers.

MAX77720

Wide Output-Voltage Range, Dual-Polarity PMIC

General Description

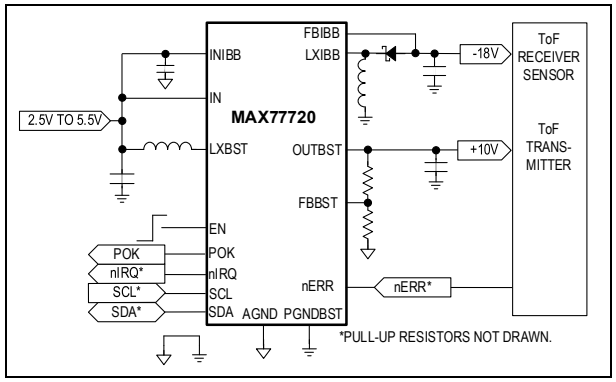
The MAX77720 dual-output DC-DC converter generates two independently regulating positive and negative supply voltages. The positive output delivers up to 4W of power at the output while the negative output delivers up to 4.8W of power. The MAX77720 is ideal for powering time of flight (ToF) imaging sensors and OLED displays in smart internet of things (IoT) devices.

The MAX77720 generates an adjustable negative output down to -24V and a positive output voltage up to +20V. The negative output operates at a fixed 1.5MHz frequency while the positive output operates at a fixed 1MHz frequency to ease noise filtering in sensitive applications and to reduce external component size.

The nERR pin, when connected to an external device's output pin, is used to disable the regulators to signal an external error. This error can be cleared through I²C from a host processor to re-enable the regulators. While in the error on state, there is an option for the active discharge to be enabled or disabled (for example, to set the regulator outputs to a high-Z floating).

A bidirectional I²C serial interface allows for configuring and checking the status of the devices. Numerous factory-programmable options allow the device to be tailored for many applications, enabling faster time to market.

Simplified Application Diagram



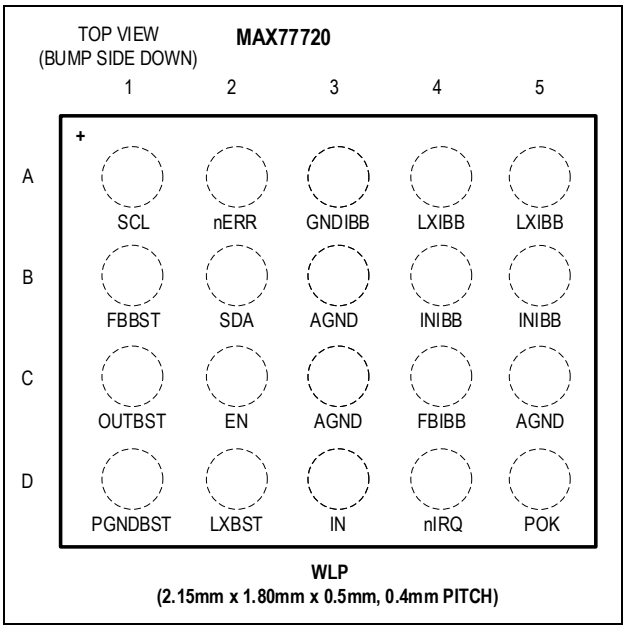
Key Applications

- ToF Sensors
- OLED Displays
- Bipolar Amplifiers

Benefits and Features

- 2.5V to 5.5V Input Voltage Range
- Programmable Output-Voltage Range (Up to +20V and Down to -24V)
- Flexible and Configurable
  - I²C Interface
  - Factory OTP Settings Available
  - Programmable Turn-On and -Off Delay Between Rails
- 1.2V to 3.6V V_{IO}-Compatible
- True Shutdown™ for Boost
- Programmable Peak Current Limit for Boost (Up to 1A and Down to 0.5A)
- Thermal-Shutdown Protection
- Fault-Condition Flag
- Error Pin for External Sensor Fault Condition
- Controlled Inrush Current During Soft-Start
- -40°C to +125°C Operating Temperature Range
- Small Size
  - 3.86mm² Wafer-Level Package (WLP)
  - 20-Bump, 0.4mm-Pitch, 5 x 4 Array

Pin Configuration



WLP
(2.15mm x 1.80mm x 0.4mm PITCH)

True Shutdown is a trademark of Maxim Integrated Products, Inc.

***Ordering Information* appears at end of data sheet.**

19-101733; Rev 0; 9/23

Click here to ask an associate for production status of specific part numbers.

MAX77720

Wide Output-Voltage Range, Dual-Polarity PMIC

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19-101733; Rev 0; 9/23

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

EN, nIRQ, nERR, POK to AGND ..... -0.3V to IN + 0.3V
SDA, SCL to AGND ..... -0.3V to IN + 0.3V
nIRQ, SDA Continuous Current ..... ±20mA
IN to AGND ..... -0.3V to +6.0V
INIBB to GNDIBB ..... -0.3V to +6V
IN to PGNDBST ..... -0.3V to +6V
V_{OUTBST} to AGND ..... -0.3V to +22V
LXBST to PGNDBST ..... -0.3V to +24V
LXIBB to GNDIBB ..... -30V to INIBB + 0.3V
PGNDBST, GNDIBB to AGND ..... -0.3V to +0.3V
FBIBB to AGND ..... -30V to +0.3V
FBBST to AGND ..... -0.3V to +6V
LXBST Continuous Current ..... $-1.6A_{RMS}$ to $+1.6A_{RMS}$
LXIBB Continuous Current ..... $-1.6A_{RMS}$ to $+1.6A_{RMS}$
Continuous Power Dissipation for WLP package (T_A = +70°C derate 20.4mW/°C above +70°C (Note 1)) 840mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

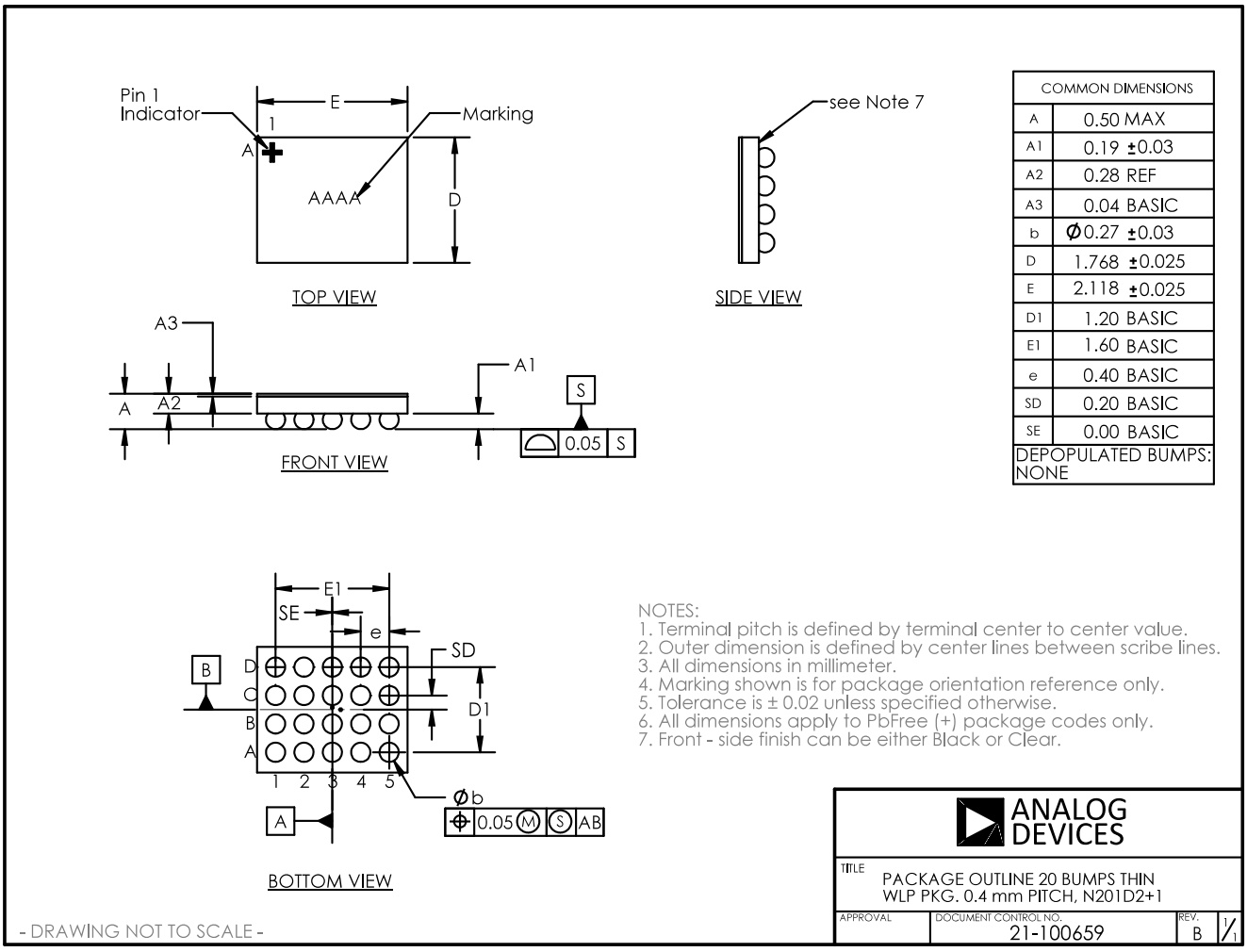
Operating Junction Temperature ..... -40°C to +125°C
Operating Ambient Temperature ..... -40°C to +125°C
Input Voltage Range ..... 2.5V to 5.5V
V_{IO} Voltage Range ..... 1.2V to 3.6V

Package Information

Package Code	N201D2+1
Outline Number	*21-100659*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	55.49°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com*.



COMMON DIMENSIONS	
A	0.50 MAX
A1	0.19 ±0.03
A2	0.28 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	1.768 ±0.025
E	2.118 ±0.025
D1	1.20 BASIC
E1	1.60 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 20 BUMPS THIN WLP PKG. 0.4 mm PITCH, N201D2+1

APPROVAL | DOCUMENT CONTROL NO. 21-100659 | REV. B | 1/1

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Supply Current	I_{SHDN}	Main bias is off (CNFG_DCDC0.ADE_IBB = 0x0)		3		µA
		Main bias is off (CNFG_DCDC0.ADE_IBB = 0x1)		20		
Quiescent Current	I_Q	Main bias is on		235		µA
		Main bias is on and BST regulator on (device not switching)		252		
		Main bias is on and IBB regulator on (device not switching)		742		
		Main bias is on and both regulators are on (device not switching)		757		

Electrical Characteristics—Global Resources

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Main Bias Enable Time	t_{SBIAS_EN}			60		µs
VOLTAGE MONITORS/POWER-ON RESET (POR)						
POR Threshold	V_{POR}	V_{IN} falling		1.5		V
POR Threshold Hysteresis	V_{POR_HYS}			100		mV
VOLTAGE MONITORS/UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold	V_{UVLO}	V_{IN} falling	2.3	2.4	2.5	V
UVLO Threshold Hysteresis	V_{UVLO_HYS}			100		mV
VOLTAGE MONITORS/OVERVOLTAGE LOCKOUT (OVLO)						
OVLO Threshold	V_{OVLO}	V_{IN} rising	5.70	5.85	6.00	V
VOLTAGE MONITORS/THERMAL MONITORS						
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising		+165		˚C
Overtemperature Lockout Hysteresis	T_{OTLO_HYS}			15		˚C
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)						
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Leakage Current	I_{nIRQ_LKG}	V_{IN} = 5.5V, nIRQ is high impedance (no interrupts), V_{nIRQ} = 5.5V, T_J = +25˚C	-1	±0.001	+1	µA
		V_{IN} = 5.5V, nIRQ is high impedance (no interrupts), V_{nIRQ}= 5.5V, T_J = +125˚C		±0.01		
OPEN-DRAIN POK OUTPUT (POK)						
POK Output Voltage Low	V_{POK_L}	I_{POK} = 2mA			0.4	V
POK Leakage Current	I_{POK_LK}	V_{IN} = 5.5V, V_{POK} = 5.5V, T_J = +25˚C	-1	±0.001	+1	µA
		V_{IN} = 5.5V, V_{POK} = 5.5V, T_J = +125˚C		±0.01		
ENABLE INPUT (EN)						
Enable Voltage Falling Threshold	V_{EN_IL}	V_{IN} = 2.5V to 5.5V, EN falling			0.36	V
Enable Voltage Rising Threshold	V_{EN_IH}	V_{IN} = 2.5V to 5.5V, EN rising	0.84			V
Enable Input Leakage	I_{EN_LK}	V_{EN} = 0 to 5.5V, T_J = +25°C	-1	±0.001	+1	µA
		V_{EN} = 0 to 5.5V, T_J = +125°C		±0.01		
ERROR PIN (nERR)						
Error Voltage Falling Threshold	V_{nERR_IL}	V_{IN} = 2.5V to 5.5V, nERR falling			0.36	V

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error Voltage Rising Threshold	V_{nERR_IH}	V_{IN} = 2.5V to 5.5V, nERR rising	0.84			V
Error Input Leakage	I_{nERR_LK}	V_{nERR} = 0 to 5.5V, T_J = +25°C	-1	±0.001	+1	µA
		V_{nERR} = 0 to 5.5V, T_J = +125°C		±0.01		
POWER-UP/POWER-DOWN DELAY (T_{DELAY})						
Power-Up Delay for Inverting Buck-Boost	$t_{D\_IBB\_UP}$	Programmable between 0.2ms and 3.2ms		0.2		ms
Power-Down Delay for Inverting Buck-Boost	$t_{D\_IBB\_DN}$	Programmable between 0.2ms and 3.2ms		0.2		ms
Power-Up Delay for Boost	$t_{D\_BST\_UP}$	Programmable between 0.2ms and 3.2ms		0.2		ms
Power-Down Delay for Boost	$t_{D\_BST\_DN}$	Programmable between 0.2ms and 3.2ms		0.2		ms

Electrical Characteristics—Boost Regulator

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BOOST REGULATOR						
Boost Output-Voltage Range	V_{OUTBST}	V_{IN} + 0.5V < V_{OUT_TARGET}	V_{IN} + 0.5V		20	V
Boost Feedback (FB) Accuracy	ACC_{CCM}	V_{FBBST} falling when LX switching frequency = 1MHz (*Note 2*)	-1.5		+1.5	%
	ACC_{DCM}	V_{FBBST} falling when LX switching frequency < 1MHz (*Note 2*)	1.239	1.258	1.277	V
Boost Output Load Regulation	ACC_{LDREG}	10mA < I_{OUTBST} < 160mA		2.0		%
LXBST Leakage Current	I_{LXP_LK}	V_{LX} = 5.5V, V_{EN} = V_{OUT} = 0V, T_J = +25°C		10	500	nA
LXBST Inductor Peak Current Limit (*Note 3*)	I_{BST_ILIM}	CNFG_IBB0.IPK_BST[2:1] = 0b00	0.8	1.0	1.2	A
		CNFG_IBB0.IPK_BST[2:1] = 0b01		0.781		
		CNFG_IBB0.IPK_BST[2:1] = 0b10		0.563		
		DCM only; CNFG_IBB0.IPK_BST[2:1] = 0b11		0.5		
Boost Soft-Start Ramp Rate	$\Delta V_{OUTBST}/\Delta t$	C_{OUT_BST} = 20µF, 35V, nominal		7		mV/µs
LXBST Maximum Duty Cycle	DC_{BST}	V_{IN} = 2.5V (*Note 4*)		90		%
LXBST Maximum On-Time	t_{ON_MAX}		1.9	3.4	6.1	µs
LXBST On-Time	t_{BST_ON}	V_{IN} = 5.5V (*Note 4*)		450		ns
LXBST Off-Time (Note 4)	t_{BST_OFF}	V_{IN} = 3.6V, V_{OUT} = 12.0V, T_J = +25°C	230	255	280	ns
		V_{IN} = 5.5V, V_{OUT} = 12.0V		350		
		V_{IN} = 5.0V, V_{OUT} = 7.0V		530		

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		V_{IN} = 3.0V, V_{OUT} = 18V		147		
LXBST Switching Frequency	f_{BST_SW}	V_{IN} = 3.6V, V_{OUT} = 12V		1.0		MHz
		V_{IN} = 5.0V, V_{OUT} = 7.0V		1.0		
		V_{IN} = 3.0V, V_{OUT} = 18V		1.0		
Boost n-Channel On-Resistance	R_{BST_RDSON}	V_{IN} = 3.6V		320	650	mΩ
Boost p-Channel On-Resistance	R_{BST_RDSON}	V_{IN} = 3.6V		320	650	mΩ
Boost Diode Forward Voltage	V_F	V_{IN} = 3.6V, I_{LX} = 100mA		0.4		V
Boost FB Leakage	$I_{FB\_BST\_LK}$	V_{FBBST} = 1.25V	-100	0.5	+100	nA
Boost Active Discharge Resistance	R_{BST_AD}	V_{IN} = 3.6V		320		Ω
BOOST POK						
Boost POK Rising Threshold	$V_{POK\_BST\_R}$	V_{OUT} when POK switches, V_{OUT_BST} rising		92		%
Boost POK Falling Threshold	$V_{POK\_BST\_F}$	V_{OUT} when POK switches, V_{OUT_BST} falling		89.5		%
BST Short-Circuit Fault Rising Threshold	V_{SC_BST}	Rising, 10µs timer, enabled at 2800µs after the rail is turned on		IN		V

Electrical Characteristics—Inverting Buck-Boost

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INVERTING BUCK-BOOST REGULATOR						
IBB Programmable Output-Voltage Range	V_{IBB_RNG}	Low range	-24.00	-18.00	-17.01	V
		High range	-17.00	-11.00	-10.01	
IBB Output-Voltage Step	V_{IBB_STEP}	9-bit (2 bytes) configuration		15		mV
IBB Output-Voltage Accuracy	V_{IBB_ACC}	T_A = -40°C to +125°C	-2.0		+2.0	%
FBN Input Current	I_{IBB_FBN}	At -15V, FBN sense input current		-50		µA
LXN Switching Frequency	f_{IBB_SW}		1275	1500	1725	kHz
IBB Maximum Duty Cycle	D_{IBB_MAX}		91	95	98	%
LXN On-Resistance	R_{IBB_ON}			0.25	0.5	Ω
LXN Leakage Current	I_{IBB_LK}	Block disabled, V_{LXN} = -24V			20	µA
LXN Current Limit	I_{IBB_ILIM}	V_{IN} = 3.6V, FBIBB = -18V		1.5		A
IBB Soft-Start Ramp Rate	$\Delta V_{IBB}/\Delta t$	V_{IN} = 2.5V, FBIBB = -24V, C_{OUT_IBB} = 20µF 50V, nominal, I_{IBB_SS} = 600mA		-4		mV/µs
		V_{IN} = 5.5V, FBIBB = -17V, C_{OUT_IBB} = 20µF, 50V, nominal, I_{IBB_SS} = 600mA		-8		

(V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J= +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IBB Soft-Start Current Limit	I_{IBB_SS}	CNFG_DCDC0.SS_IBB = 0x0, V_{IN} = 3.6V		400		mA
		CNFG_DCDC0.SS_IBB = 0x1, V_{IN} = 3.6V		600		
IBB Active Discharge Resistance	R_{IBB_AD}	V_{IN} = 3.6V		320		Ω
INVERTING BUCK-BOOST POK						
IBB POK Rising Threshold	$V_{POK\_IBB\_R}$	V_{OUT_IBB} when POK switches, V_{OUT_IBB} rising		90		%
IBB POK Falling Threshold	$V_{POK\_IBB\_F}$	V_{OUT_IBB} when POK switches, V_{OUT_IBB} falling (V_{OUT_IBB} = -18V)		81.7		%
		V_{OUT_IBB} when POK switches, V_{OUT_IBB} falling (V_{OUT_IBB} = -11V)		76.5		
IBB Short-Circuit Fault Rising Threshold	V_{SC_IBB}	Rising, 10µs timer, enabled at 2800µs after the rail is turned on		40		%

Electrical Characteristics—I²C Serial Interface

(V_{IN} = 3.6V , V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}		0.84			V
SCL, SDA Input Low Voltage	V_{IL}				0.36	V
SDA Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.4	V
SCL, SDA Input Capacitance	C_I			6		pF
SCL, SDA Input Leakage Current	I_{LK}		-10	0.001	+10	µA
I²C-COMPATIBLE INTERFACE TIMING (STANDARD) (*Note 5*)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs
Hold Time (REPEATED) START Condition	t_{HD_START}	(*Note 6*)	0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.3			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.26			µs
DATA Hold Time	t_{HD_DATA}	(*Note 7* and *Note 8*)	0			µs
Setup Time for STOP condition	t_{SU_STO}		0.26			µs
Pulse Width of Suppressed Spikes	t_{SP}			50		ns

Note 2: Output accuracy does not include load, line, or ripple.

Note 3: This is a static measurement. The actual peak current limit depends upon V_{IN} and the inductor due to propagation delays.

Note 4: Measured opened loop. Propagation delays not included.

Note 5: Design guidance only. Not production tested.

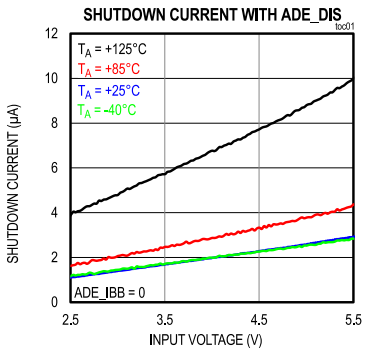
Note 6: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

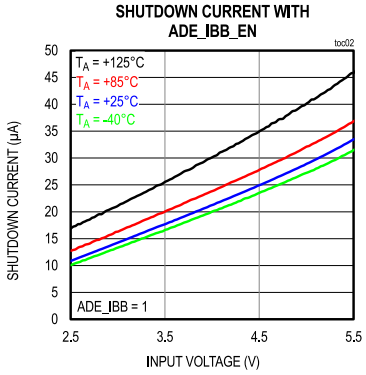
Note 7: The maximum t_{HD_DATA} has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

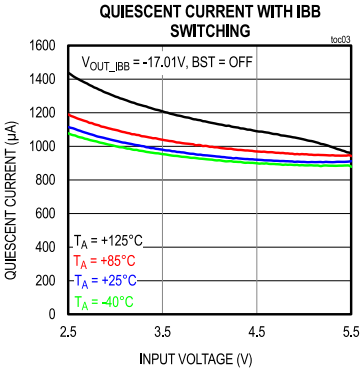
Note 8: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

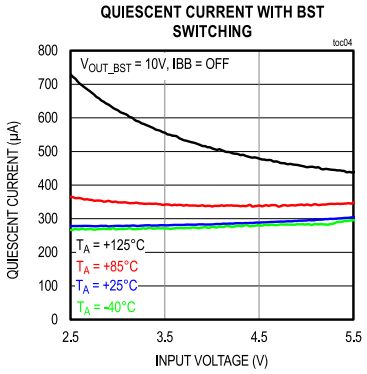
Typical Operating Characteristics

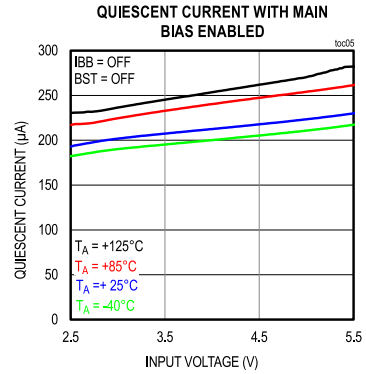
V_{IN} = 3.6V, V_{OUTIBB} = -18V, V_{OUTBST} = 10V, limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.

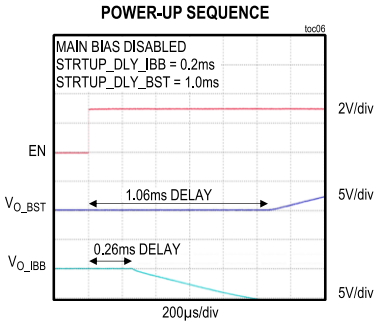




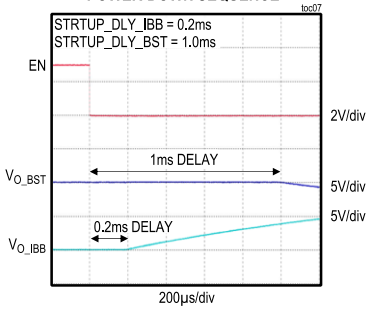




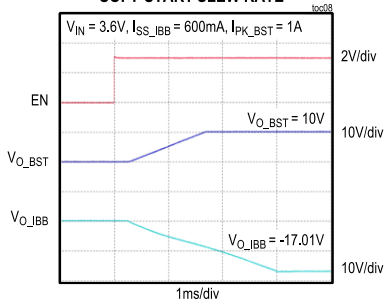




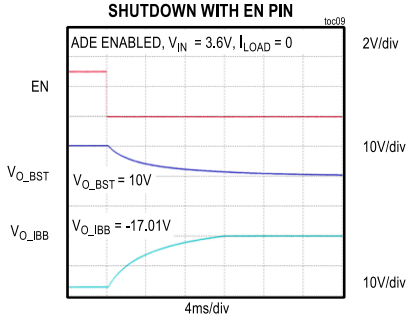
POWER-DOWN SEQUENCE



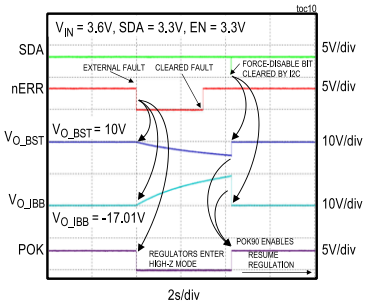
SOFT-START SLEW RATE



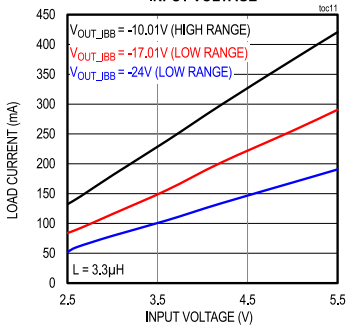
SHUTDOWN WITH EN PIN



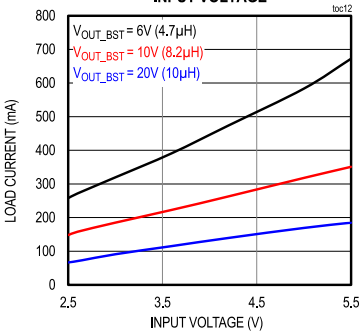
nERR PIN FUNCTIONALITY



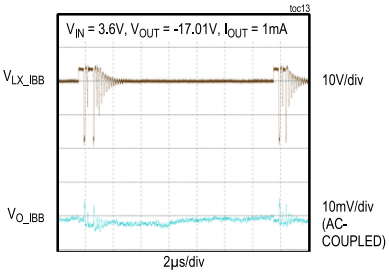
MAXIMUM IBB LOAD CURRENT vs. INPUT VOLTAGE



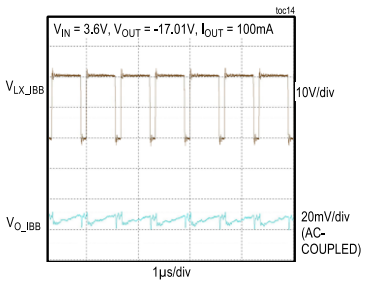
MAXIMUM BST LOAD CURRENT vs. INPUT VOLTAGE



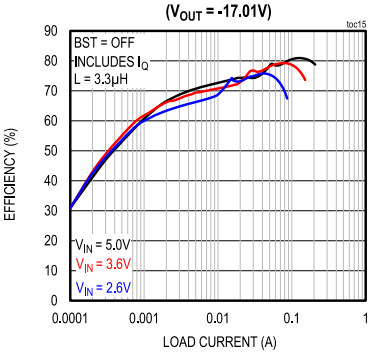
IBB SWITCHING IN LIGHT LOAD



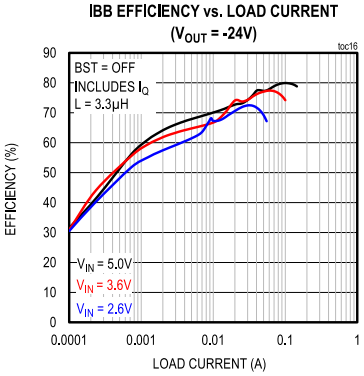
IBB SWITCHING IN CCM



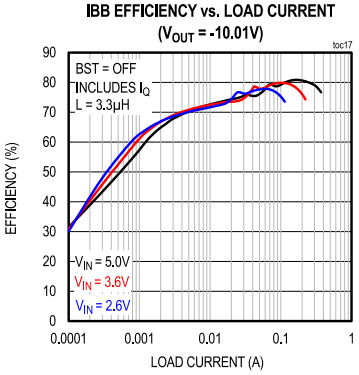
IBB EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -17.01V)



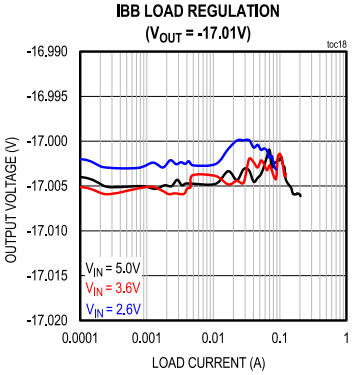
IBB EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -24V)



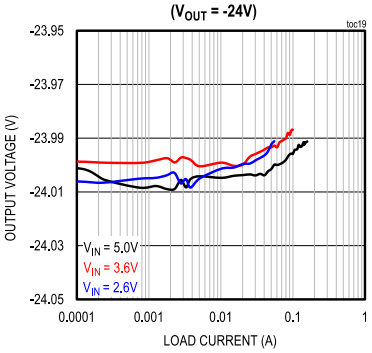
IBB EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -10.01V)



IBB LOAD REGULATION (V_{OUT} = -17.01V)



IBB LOAD REGULATION (V_{OUT} = -24V)



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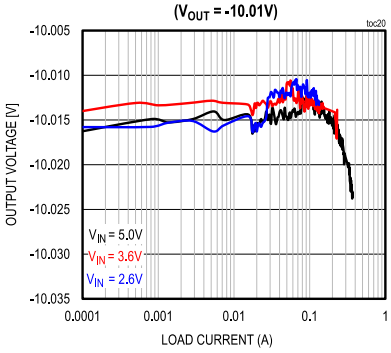

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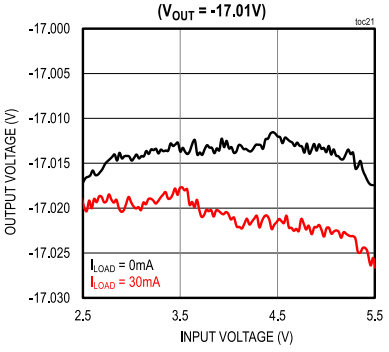

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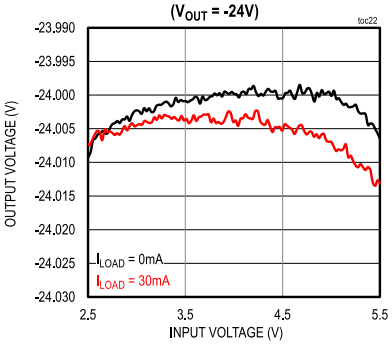

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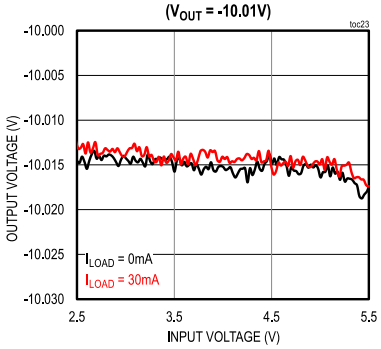

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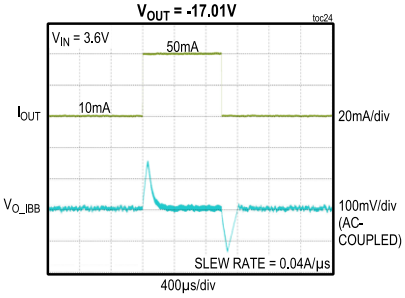

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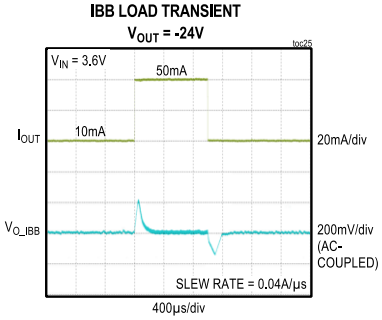
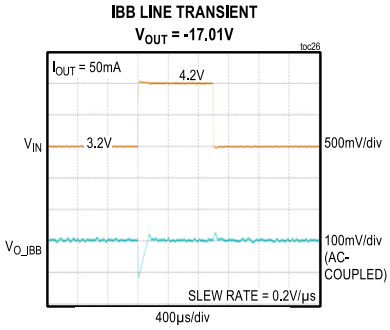


IBB LINE TRANSIENT V_{OUT} = -17.01V



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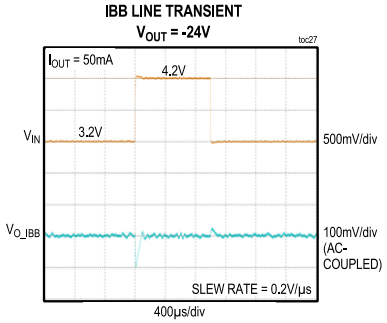
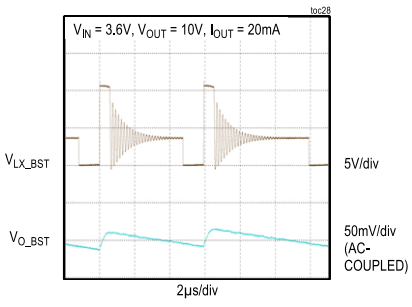
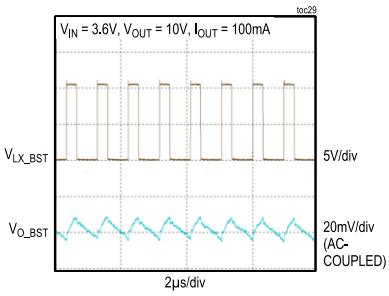


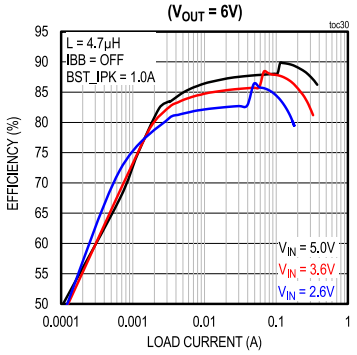
BST SWITCHING IN LIGHT LOAD



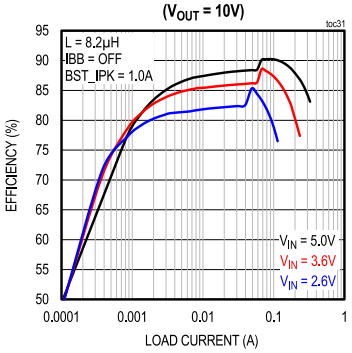
BST SWITCHING IN CCM



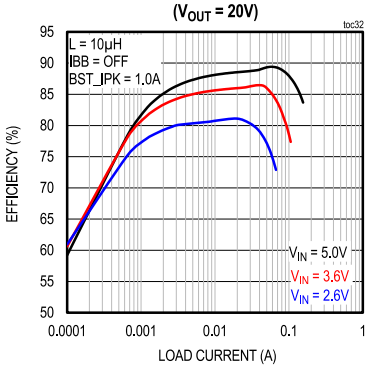
BST EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 6V)



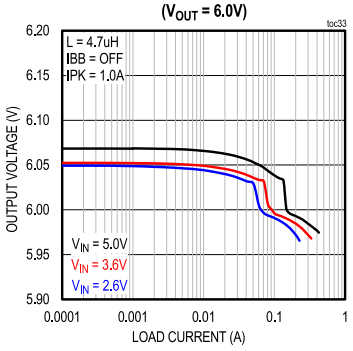
BST EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 10V)



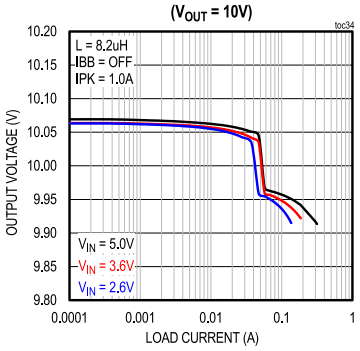
BST EFFICIENCY vs. LOAD CURRENT
(V_{OUT} = 20V)



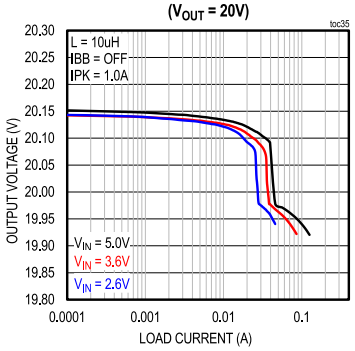
BST LOAD REGULATION
(V_{OUT} = 6.0V)



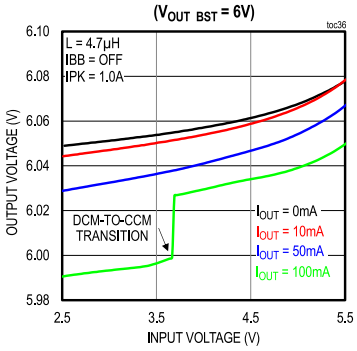
BST LOAD REGULATION
(V_{OUT} = 10V)



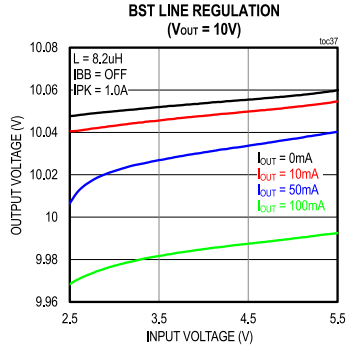
BST LOAD REGULATION
(V_{OUT} = 20V)



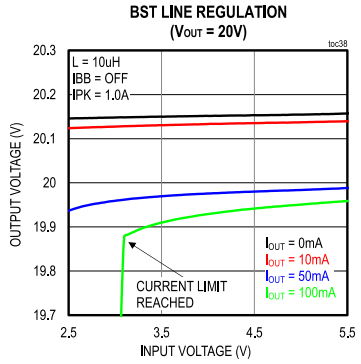
BST LINE REGULATION
($V_{OUT\ BST}$ = 6V)



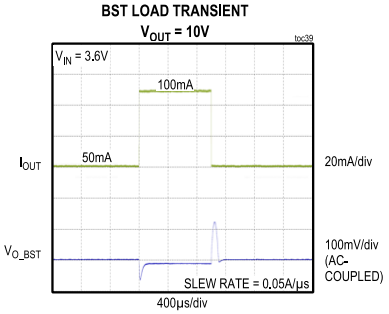
BST LINE REGULATION
(V_{OUT} = 10V)



BST LINE REGULATION
(V_{OUT} = 20V)



BST LOAD TRANSIENT
V_{OUT} = 10V



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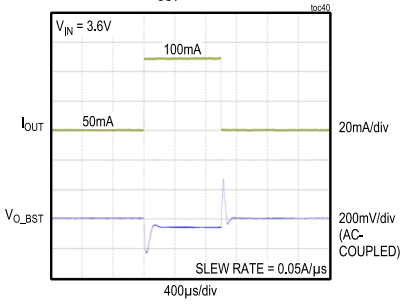
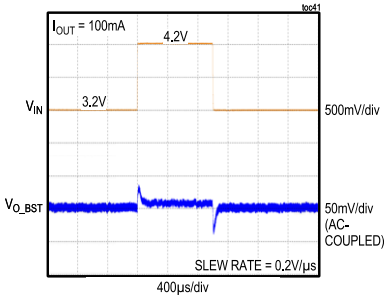
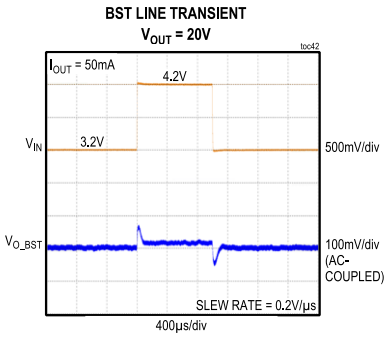
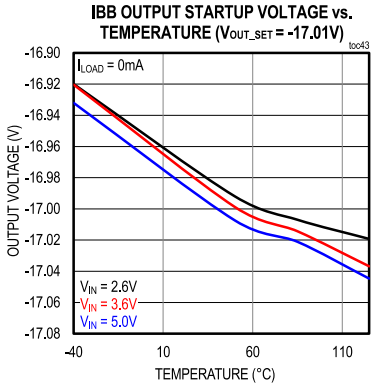
V_{OUT} = 20V



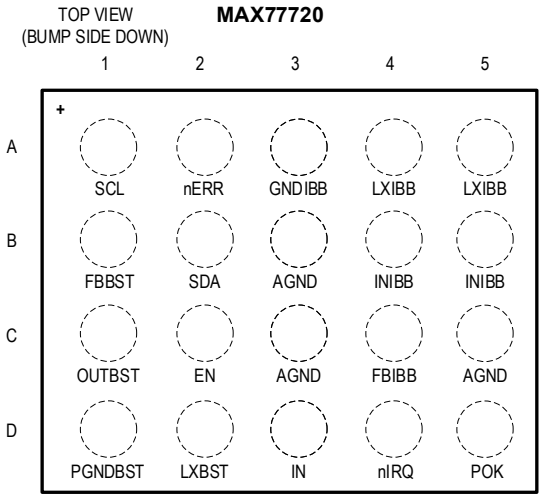
BST LINE TRANSIENT
V_{OUT} = 10V







Pin Configuration



WLP
(2.15mm x 1.80mm x 0.5mm, 0.4mm PITCH)

Pin Description

PIN	NAME	FUNCTION	Type
C2	EN	Active-High Enable Input	Digital Input
D4	nIRQ	Active-Low, Open-Drain Interrupt. Connect a 100kΩ pull-up resistor from nIRQ to external logic rail.	Digital Output
A1	SCL	I²C Clock	Digital Input
B2	SDA	I²C Data	Digital I/O
D3	IN	Input Voltage Connection. Bypass to AGND with a 1µF ceramic capacitor.	Power Input
B3, C3, C5	AGND	Quiet Ground	Ground
D5	POK	Open-Drain, Power-OK Output. Connect a 100kΩ pull-up resistor from POK to external logic rail.	Digital Output

A2	nERR	Active-Low Error Input. Connect a 100kΩ pull-up resistor from nERR to external logic rail.	Digital Input
B4, B5	INIBB	Inverting Buck-Boost Power Input. Bypass to GNDIBB with a 22µF ceramic capacitor.	Power Input
C4	FBIBB	Inverting Buck-Boost Output-Voltage Sense Input. Connect to the output at the point-of-load (close to the output capacitor).	Power Input
A4, A5	LXIBB	Switching Node for Inverting Buck-Boost. Connect LXIBB to an external Schottky diode.	Power Output
A3	GNDIBB	Ground for Inverting Buck-Boost	Ground
C1	OUTBST	Boost Output-Voltage	Power Output
B1	FBBST	Boost Output-Voltage Feedback Input. Connect to the center tap of an external resistor-divider from the output to AGND to set the output voltage. See the *Configuring the Boost Output Voltage* section for more details.	Power Input
D2	LXBST	Switching Node Pin of Boost. Connect the inductor from IN to LXBST.	Power Output
D1	PGNDBST	Power Ground for Boost	Ground

Block Diagram

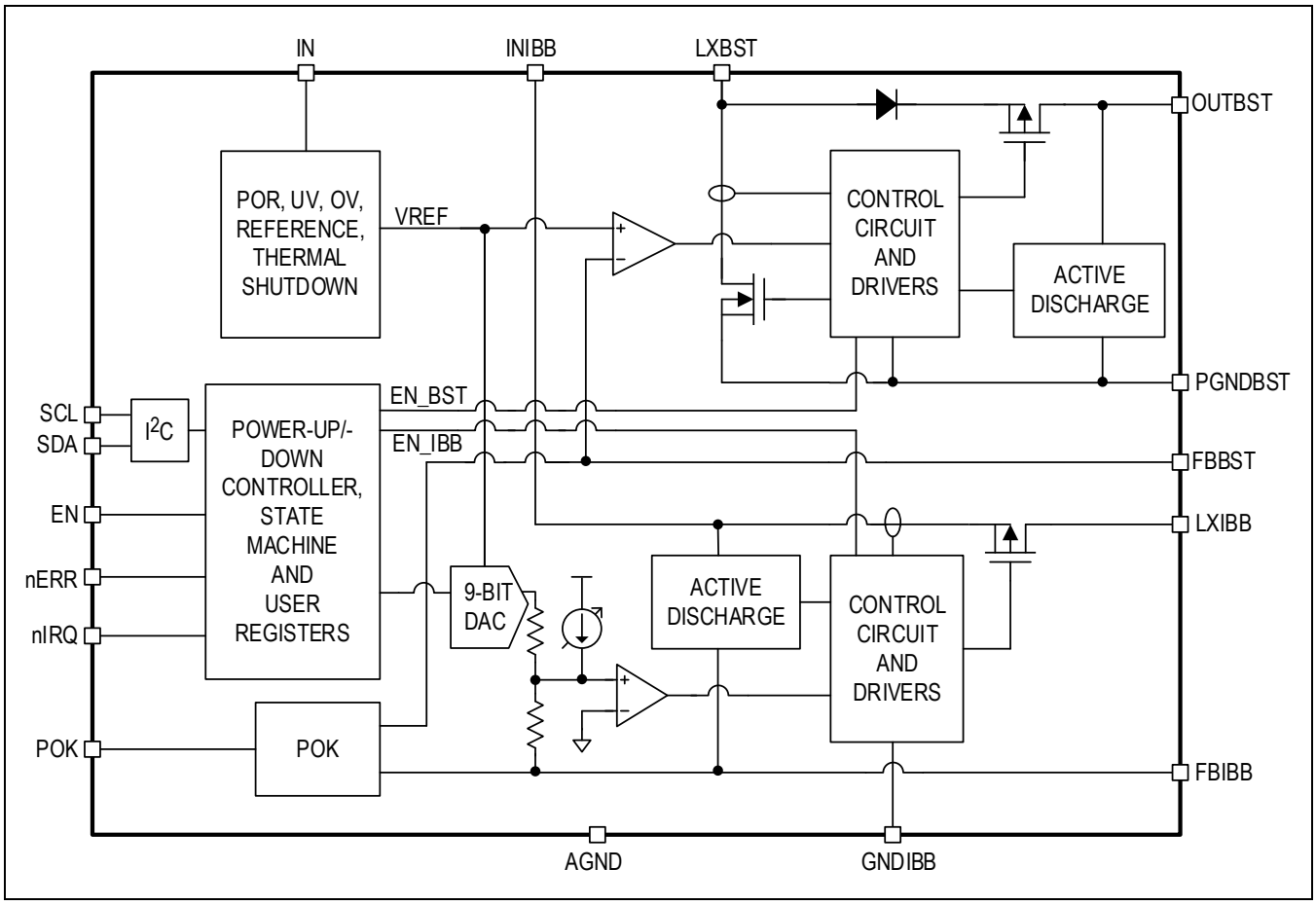


Figure 1. MAX77720 Detailed Functional Diagram

Detailed Description

The MAX77720 is a wide-range, dual-polarity integrated circuit that generates both a positive and negative output voltage by combining both a step-up boost converter and an asynchronous inverting buck-boost converter. The boost converter has True Shutdown, which disconnects the output from the input with no forward or reverse current.

Each regulator is independently regulated and separately controlled by a pulse-width-modulated (PWM) controller. Additionally, the boost converter allows for programmability of changing the peak current limit thresholds. The different peak current limit thresholds for the boost converter allow the use of lower profile and smaller external components optimized for a particular application. The use of external feedback resistors for the boost converter allows for wider output-voltage range and customizable output voltages at startup.

The inverting buck-boost converter allows for programmable voltages from a host processor through I2C.

An optional I2C serial interface allows dynamic control of the following:

- Output voltage for the inverting regulator (using internal reference voltage)
- Programmable peak current limit for the positive regulator (using I2C)
- Turn on and shutdown delay for the positive and negative regulator
- POK status and fault interrupts
- Enabling and disabling active discharge for the positive and negative regulator

Part Number Decoding

The MAX77720 has different one-time programming (OTP) options and variants to support a variety of applications. Variants are versions of the MAX77720 with different features. See *Figure 2* for an explanation of the MAX77720 part number decoding. The MAX77720 offers various settings such as settings for default output voltages or power-on delay. These OTP variants are identified by the register name, which can be read in the OTP_REV register. *Table 1* lists all available OTP options. Refer to *Key Package Information* for more details.

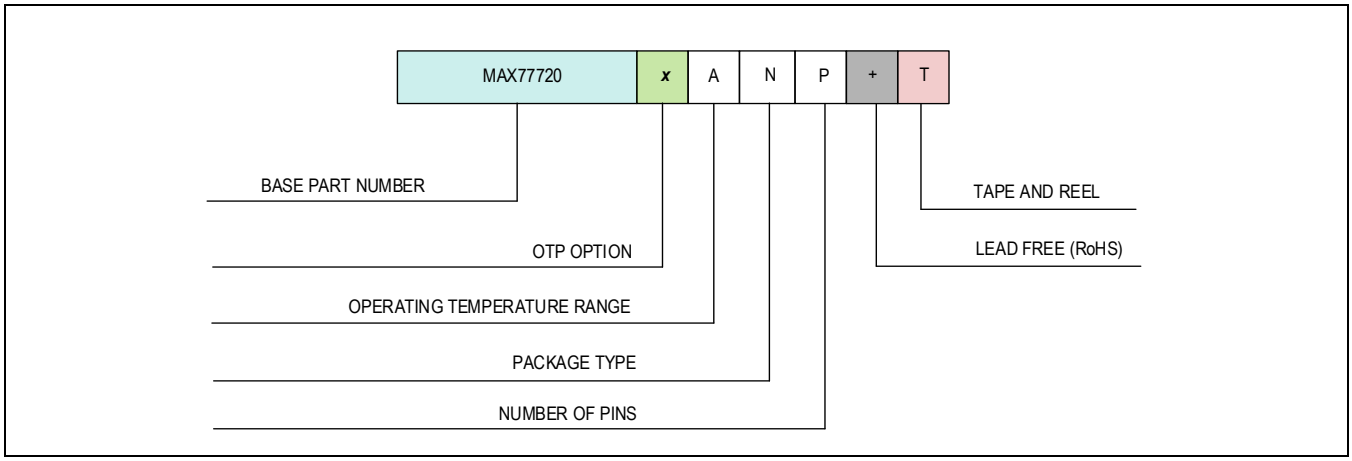


Figure 2. Part Number Decode

Table 1. OTP Options Table

			OTP LETTER AND SETTINGS
BLOCK	**BITFIELD NAME**	**SETTING NAME**	**S**
Global	ADDR	I^2C Address (7-Bit)	0x41
	OTP_REV[5:0]	OTP Revision	0x21
IBB	VOUT_IBB[9:0]	Inverting Buck-Boost V_{OUT}	-17.01V
	RNG_IBB	Inverting Buck-Boost Output-Voltage Range	Low Range
	SS_IBB	Inverting Buck-Boost Soft-Start Current Limit	600mA
	ADE_IBB	Inverting Buck-Boost Active Discharge Enable	Enabled
	STRTUP_DLY_IBB[7:4]	Inverting Buck-Boost Startup Delay	0.2ms
	PWRDN_DLY_IBB[3:0]	Inverting Buck-Boost Power-Down Delay	0.2ms
BST	IPK_BST	Boost Peak Current Limit	1.0A
	ADE_BST	Boost Active Discharge Enable	Enabled
	STRTUP_DLY_BST[7:4]	Boost Startup Delay	0.2ms
	PWRDN_DLY_BST[3:0]	Boost Power-Down Delay	0.2ms

Power-Up/Power-Down Sequence

The MAX77720 integrates a timer delay that controls the power-up/power-down timing of the regulators. The functionality of the power-up and power-down is described as follows:

- The power-up delays start from the time the EN pin goes from low to high.
- The power-down delays start from the time the EN pin goes from high to low.
- The 16 programmable power-up and power-down delays range from 0.2ms to 3.2ms in 0.2ms increments.
- The soft-start feature limits the slew rate of the output voltage during startup (each regulator has their own soft-start feature).
- The power-down ramp rate depends on the output load current and active discharge circuit.

Figure 3 shows an example of the power-up/power-down sequence with respect to the EN pin.

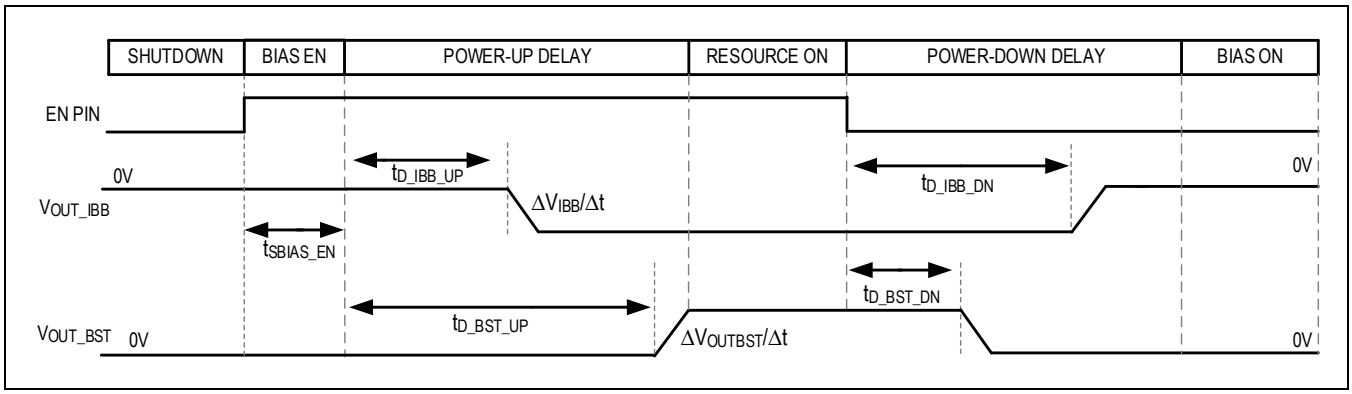


Figure 3. Start-Up Programmable Timing Diagram (Includes EN_Bias Timing with CNFG_GLBL.EN_BIAS = 0)

Soft-Start

The soft-start feature of the device limits inrush current during startup, which is achieved by limiting the slew rate of the output voltage during startup (d_V/d_{TSS}). The MAX77720 soft-start begins when the EN pin is pulled high above V_{IH} and after the programmed delay for each individual regulator.

The output-voltage ramp rate for the boost regulator is a fixed 7mV/µs. The output-voltage ramp rate for the inverting buck-boost regulator is dependent on the soft-start current limit setting, input voltage, and output voltage. See the *Electrical Characteristics* for typical soft-start ramp rates for the selected settings. The two selectable soft-start current limits allow for trading power-up time for minimum battery transient impact and should be changed for certain applications.

Shutdown

When the EN pin is pulled low ($V_{EN} < V_{EN\_IL}$), the MAX77720 goes into the shutdown state. While in the shutdown state, both regulators are not switching but are still programmable through I²C. See *Figure 7* and *Table 4* for details. The current consumed in this mode is 235µA if the main bias is on with no regulators enabled.

nERR Error Pin

The error pin (nERR) is an active-low, digital input. When this pin receives a falling edge, the STAT_GLBL.ERR_PIN_S asserts high and both the boost and the inverting buck-boost converters stop regulating. If the active discharge is disabled, both regulators remain in a high-Z state, and the rate of discharge depends on the output load condition. To re-enable the regulators, write a 0 to the CNFG_GLBL.FORCE_DIS bitfield through I²C. Once I²C clears it, both the boost and the inverting buck-boost converters resume regulation again after the programmed timing startup delay with the programmed soft-start enabled at any voltage.

Table 2 gives a summary of certain states while *Figure 4* displays the output voltages with respect to the nERR pin if the active discharge is disabled.

Table 2. Error Pin Summary

nERR PIN	ERROR PIN STATUS (STAT_GLBL.ERR_PIN_S)	FORCE DISABLE BIT (CFNG_GLBL.FORCE_DIS)	INVERTING BUCK-BOOST	BOOST
High to Low	1	1	High-Z	High-Z
Low to High	0	Keep 1 until I²C clears the error by writing to a 0	Keep high-Z until I²C clears the error	Keep high-Z until I²C clears the error

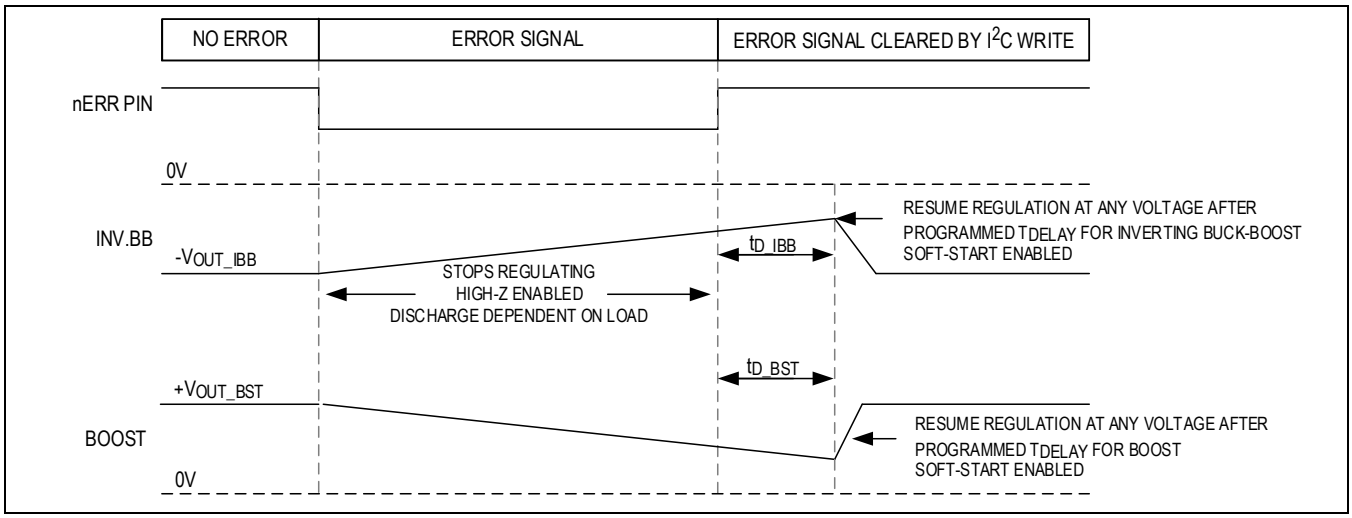


Figure 4. Error Pin Functional Diagram

There are multiple ways to re-enable the regulators during the error-on state. Each scenario assumes that an error signal has already been received by the nERR pin going from high to low:

1. After the nERR pin returns high, regulation for both the inverting buck-boost and boost converters resumes with the programmed timing delays and soft-start after writing a 0 to the CNFG_GLBL.FORCE_DIS bitfield.

Note: This method only works when the EN pin is still held high. Otherwise, CNFG_GLBL.FORCE_DIS does not re-enable the regulators. *Figure 5* shows the requirements to resume regulation using this method.

2. After the nERR pin returns high, regulation for both the inverting buck-boost and boost converter can be enabled individually through I2C by writing to registers CNFG_GLBL.FORCE_IBB_ON = 1 or CNFG_GLBL.FORCE_BST_ON = 1 and by writing CNFG_GLBL.FORCE_DIS = 0. If CNFG_GLBL.FORCE_XXX_ON = 1, no timing delay is implemented for the regulator to resume regulation. If the EN pin is still held high, while only one CNFG_GLBL.FORCE_XXX_ON = 1, the other regulator resumes regulation after its programmed timing delay. *Figure 6* shows this behavior with the CNFG_GLBL.FORCE_IBB_ON = 1 scenario. *Figure 7* and *Table 4* show the top-level system flow to resume regulation.

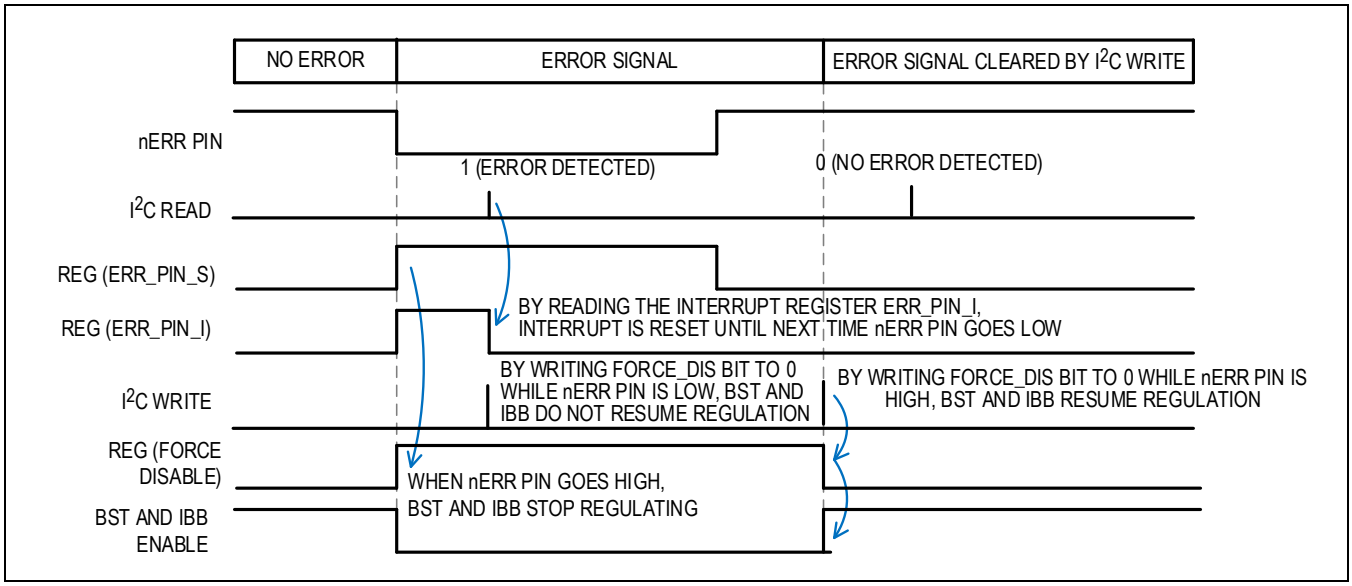


Figure 5. Error-State Timing Diagram

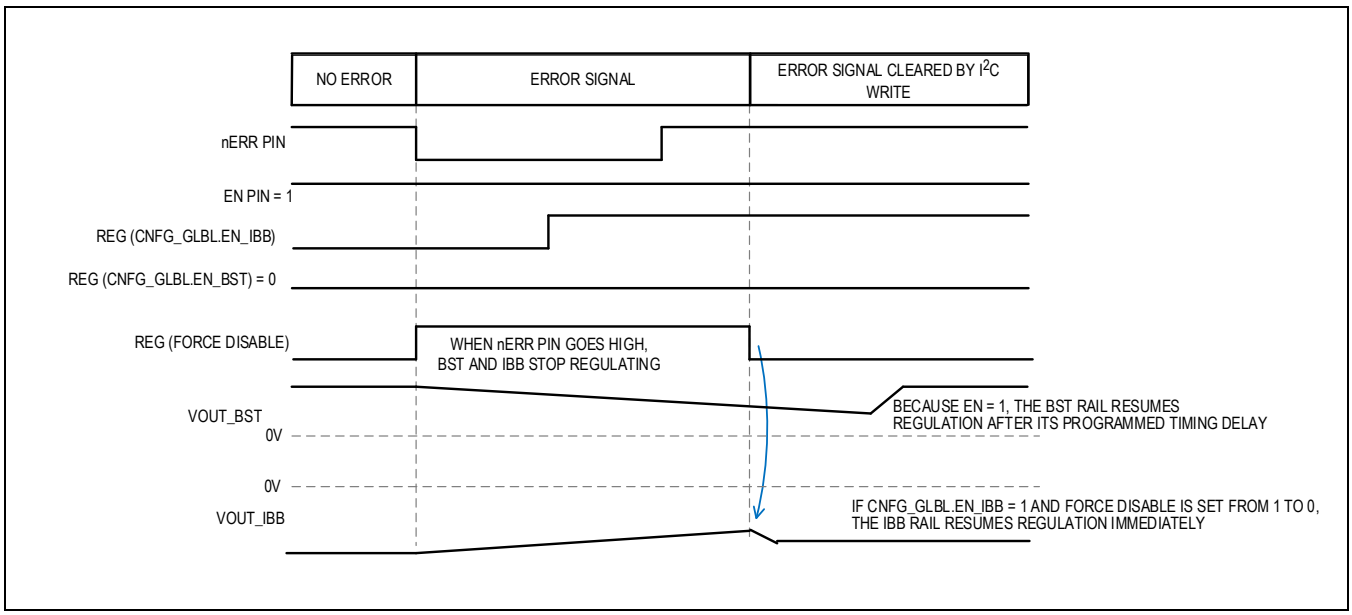


Figure 6. Re-Enabling Regulator Using the CNFG_GLBL.EN_IBB Bit

Output Active-Discharge

Each regulator has an active-discharge resistor (R_{AD_BST} and R_{AD_IBB}). The active-discharge feature may be enabled (CNFG_DCDC0.ADE_BST or CNFG_DCDC0.ADE_IBB = 1) or disabled (CNFG_DCDC0.ADE_BST or CNFG_DCDC0.ADE_IBB = 0) independently for each individual regulator. Enabling the active discharge feature ensures a complete and timely power-down of all system peripherals.

Note: The R_{AD_IBB} turns off once the output voltage of the inverting buck-boost reaches 0V.

Power-OK Monitor

The IC features power-OK (POK) status bits (STAT_GLBL.POK_IBB_S and STAT_GLBL.POK_BST_S) and interrupt flags (INT_GLBL0.POK_IBB_I and INT_GLBL0.POK_BST_I).

In addition, the open-drain POK digital output pin reflects the logical AND of all POK flags of enabled regulators. If either regulators are disabled, the POK pin is pulled low. See *Table 3* for the truth table. Connect the POK pin with a pull-up resistor to an external logic rail.

While in the error-on state (see *Table 2*), both regulators are disabled. Therefore, the POK pin is pulled low.

Table 3. POK Pin Truth Table

IBB ENABLE	POK_IBB_S	BST ENABLE	POK_BST_S	POK PIN STATE
Disabled	Don't Care	Disabled	Don't Care	0
Disabled	Don't Care	Enabled	0	0
			1	0
Enabled	0	Disabled	Don't Care	0
	1			0
Enabled	0	Enabled	0	0
	0		1	0
	1		0	0
	1		1	High-Z

If the target output voltage of the inverting buck-boost is changed to a higher absolute value (e.g., -17.01V to -24V), STAT_GLBL.POK_IBB_S can be 0 during the voltage transition. To avoid false flags, ignore STAT_GLBL.POK_IBB_S during a voltage transition and clear the interrupt flag (INT_GLBL0.POK_IBB_I) after the regulator output settles.

Interrupt (nIRQ)

The nIRQ pin is an active-low, open-drain output typically routed to a controller interrupt input for triggering off interrupt events. Several status, interrupt, and interrupt mask registers monitor key information and update when an interrupt event has occurred. See the Register Map for a comprehensive list of all interrupt bits and status registers. Depending on the OTP, some or all interrupts are masked by default. Initialization software unmasks interrupts of interest.

When any unmasked interrupt occurs, this pin is asserted low. A 100kΩ pull-up resistor is required for this signal and is typically found inside the controller. If one is unavailable, a board-mounted 100kΩ pull-up resistor to a logic rail is required.

System State Flow

Figure 7 and *Table 4* describe from a top level the different conditions to enable or disable resources (e.g., switching regulators) in the MAX77720. *Figure 7* organizes the device's behavior as a set of states (shown in bubbles). For example, the shutdown state is a state in which all regulators and the bias are disabled and the device draws the lowest current from the input. *Table 4* details the conditions to trigger transitions between two states. For example, to wake up the device and start the power-up sequence (transition 3 to 4 and transition 4 to 5), apply a high signal to the EN pin.

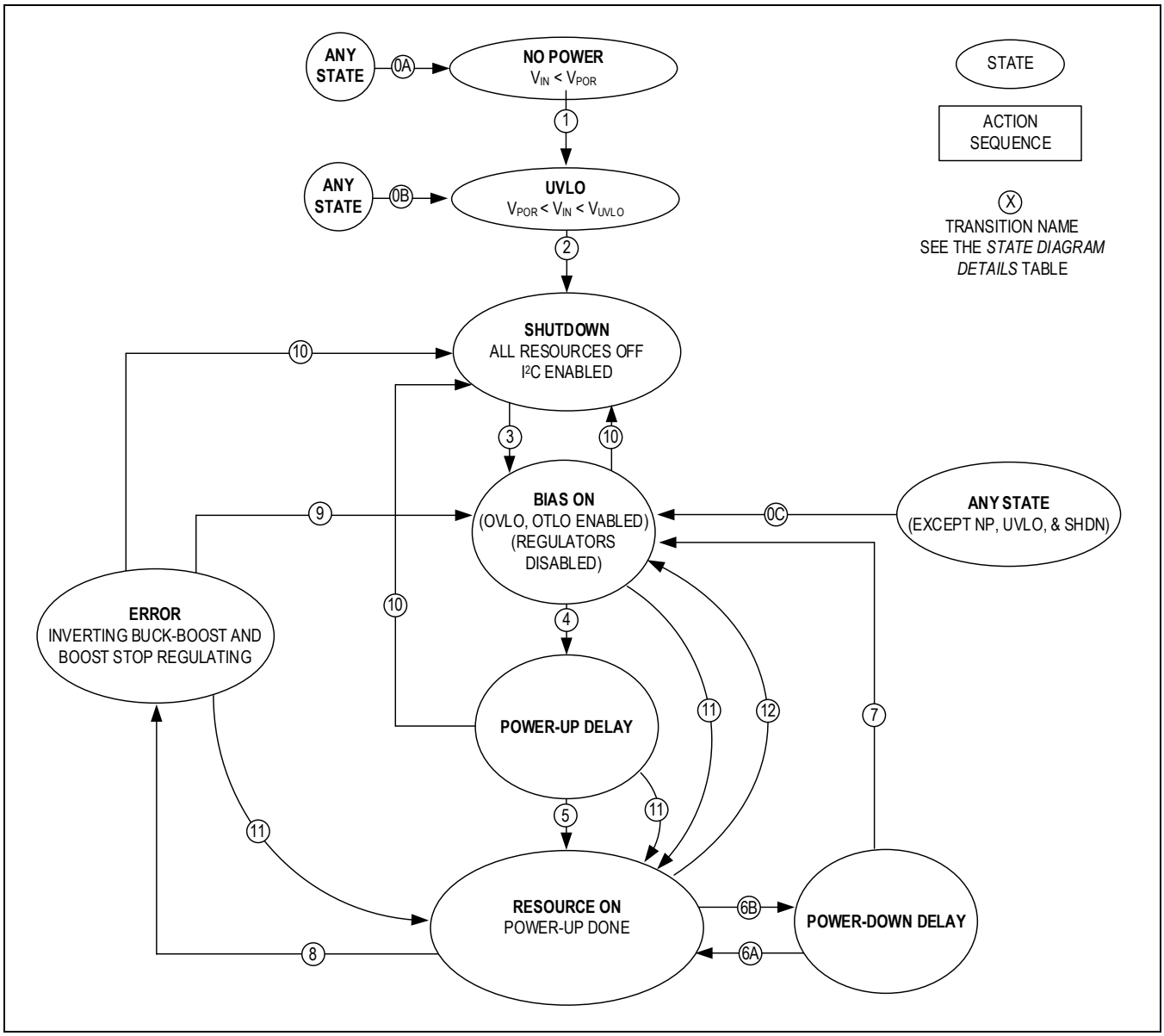


Figure 7. Top-Level State Diagram

Table 4. State Diagram Details

TRANSITION/STATE	CONDITION
0A	IN voltage is below the POR threshold ($V_{IN} < V_{POR}$).
0B	IN voltage is above the POR threshold but is below the UVLO threshold ($V_{POR} < V_{IN} < V_{UVLO}$).
0C	Fault detected: • System overtemperature lockout ($T_J > T_{OTLO}$) or • System overvoltage lockout ($V_{IN} > V_{OVLO}$) or • Bias circuits are not OK Both regulators are immediately shut down to protect the IC.
No Power	All registers are reset. I2C disabled.
1	IN voltage is above the POR threshold ($V_{IN} > V_{POR}$).

UVLO	IN voltage is above the POR threshold but is below the UVLO threshold (V_{POR} < V_{IN}< V_{UVLO}). All registers are reset in this state except for the fault registers. *State of ERCFLAG.UVLO, ERCFLAG.OVLO, and ERCFLAG.OTLO is preserved.
2	IN voltage is above the UVLO threshold (V_{IN} > V_{UVLO} + V_{INUVLO_HYS}).
Shutdown	The device is waiting for a wake-up signal to power up the regulators. I^2C is enabled. When EN = 0, active discharge immediately turns on and pulls all output voltages down to 0V. *This is the lowest current state of the device (I_{SHDN}).
3	A wake-up signal has been received. Wake-up signals include: ● EN = 1 or ● Setting CNFG_GLBL.FRC_IBB_ON or CNFG_GLBL.FRC_BST_ON or CNFG_GLBL.EN_BIAS register bit to 1
Bias On	Bias circuits (REF, I_{BIAS}, OSC) and fault detection circuits (OVLO and OTLO) are enabled. Inverting buck-boost and boost regulators are disabled.
4	Bias circuits are OK. No faults detected: UVLO = 0, OVLO = 0, and OTLO = 0. CNFG_GLBL.FRC_IBB_ON and CNFG_GLBL.FRC_BST_ON register bits are both 0.
Power-Up Delay	Start power-up counter
5	Inverting buck-boost and boost regulator programmed power-up t_{DELAY} reached. Set PU_BST_DONE = 1 and PU_IBB_DONE = 1.
Resource On	Buck-boost and boost regulator are enabled.
6A	Request to power down received. Software power-down enabled. (EN = 0) and {(PU_DONE_BST = 1 and CNFG_GLBL.FRC_BST_ON = 0) or (PU_IBB_DONE = 1 and CNFG_GLBL.FRC_IBB_ON = 0)} Boost powers down after t_{D_BST}. This is from when power-down request is received to programmed t_{D_BST} time. Inverting buck-boost powers down after t_{D_IBB}. This is from when power down request is received to programmed t_{D_IBB} time.
6B	Not transition 6A. (EN = 1) and {(PU_DONE_BST = 0 and CNFG_GLBL.FRC_BST_ON = 1) or (PU_IBB_DONE = 0 and CNFG_GLBL.FRC_IBB_ON = 1)} This transition happens if CNFG_GLBL.FRC_BST_ON = 1 or CNFG_GLBL.FRC_IBB_ON = 1 and EN = 1 signal is received during the power-down delay time. If the transition occurs, the power-down delay counter is terminated and regulators remain on.
Power-Down Delay	Start power-down counter. **Note:** Only resource that is on is powered down.
7	Buck-boost and boost regulator programmed power-down t_{DELAY} reached. Set PU_BST_DONE = 0 and PU_IBB_DONE = 0.
8	nERR pin has been flagged. (From 1 to 0) while EN = 1 and both regulators are on.
ERROR	Regulators are disabled. Depending on the OTP, if the active discharge is disabled (CNFG_DCDC0.ADE_IBB and CNFG_DCDC0.ADE_BST = 0 default), output regulators are in high-Z mode. Depending on the OTP, if the active discharge is enabled, (CNFG_DCDC0.ADE_IBB and CNFG_DCDC0.ADE_BST = 1), output regulators discharge back to 0V.
9	nERR pin output has been reset to 1 AND an I^2C signal has been sent to reenable the negative buck-boost and boost regulators (CNFG_GLBL.FORCE_DIS bit = 0).
10	Not transition 3. The wake-up signal is no longer enabled, which causes the regulators to power down. Neither the EN pin nor the following register bits (CNFG_GLBL.FRC_IBB_ON, CNFG_GLBL.FRC_BST_ON, and CNFG_GLBL.EN_BIAS) are set to 1.

11	The boost or inverting buck-boost is forced on and no power-up delay is implemented. CNFG_GLBL.FRC_IBB_ON = 1 or CNFG_GLBL.FRC_BST_ON = 1. Bias circuits are OK No faults detected: UVLO = 0, OVLO = 0, and OTLO = 0. **Note:** CNFG_GLBL.FRC_IBB_ON = 1 clears PU_DONE_IBB. CNFG_GLBL.FRC_BST_ON = 1 clears PU_DONE_BST.
12	The boost or inverting buck-boost is forced off and no power-down delay is implemented. (CNFG_GLBL.FRC_IBB_ON = 0 and PU_DONE_IBB = 0) and (CNFG_GLBL.FRC_IB_ON = 0 and PU_DONE_BST = 0)

Protection Features

IN Overvoltage Lockout (OVLO)

The overvoltage protection feature ensures that the input voltage V_{IN} never exceeds the overvoltage limit threshold (V_{OVLO}). When V_{IN} rises up to V_{OVLO}, the device detects the overvoltage, sets the ERCFLAG.OVLO bit, and activates the overvoltage lockout by disabling all the regulators.

IN Undervoltage Lockout (UVLO)

The undervoltage lockout feature prevents operation in abnormal input conditions when the input voltage V_{IN} falls below the UVLO falling voltage (V_{UVLO_F}). Regardless of the EN pin status, the device is disabled, and all registers are reset until V_{IN} rises above the UVLO rising threshold (V_{UVLO_R}).

Overtemperature Lockout (OTLO)

The MAX77720 has a on-chip thermal sensor to monitor overtemperature conditions. The thermal overtemperature lockout alarm generates an ERCFLAG.OTLO signal when the junction temperature exceeds the overtemperature lockout specification (see T_{OTLO} in. *Electrical Characteristics—Global Resources*. When OTLO is asserted, the system resets which disables all functions of the MAX77720. Once all functions are disabled, a wake-up event is required to turn the MAX77720 on again. To wake up the MAX77720 after a overtemperature lockout condition, the junction temperature must be below T_{OTLO} - T_{OTLO_HYS}. If a wake-up event turns the MAX77720 on when the junction temperature is still above T_{OTLO} - T_{OTLO_HYS}, the MAX77720 promptly forces system reset which disables all functions again. The host can check if a overtemperature lockout condition occurred by reading the ERCFLAG.OTLO flag.

Overcurrent Protection (OCP)

The MAX77720 limits the inductor peak current limit for both the inverting buck-boost and boost converter. The MAX77720 allows an inductor current limit of I_{BB_ILIM} (1.5A typical) on the inverting buck-boost converter.

For the boost converter, there are four inductor peak current limit options (see I_{BST_ILIM} in *Electrical Characteristics—Boost Regulator* section). The boost inductor peak current limit is programmable at the bitfield CNFG_IBB0.IPK_BST. This allows for flexibility in designing for higher load-current applications or for more compact designs when less power is needed. Note that the currents listed above are peak inductor currents and not output load currents.

If the lowest boost inductor peak current limit is used (CNFG_DCDC0.IPK_BST = 0x3), the regulator operates in discontinuous mode (DCM) only, and OCP sets if the output voltage is below target when the inductor current reaches 0A. *Figure 8* shows a diagram of when the OCP sets for this condition.

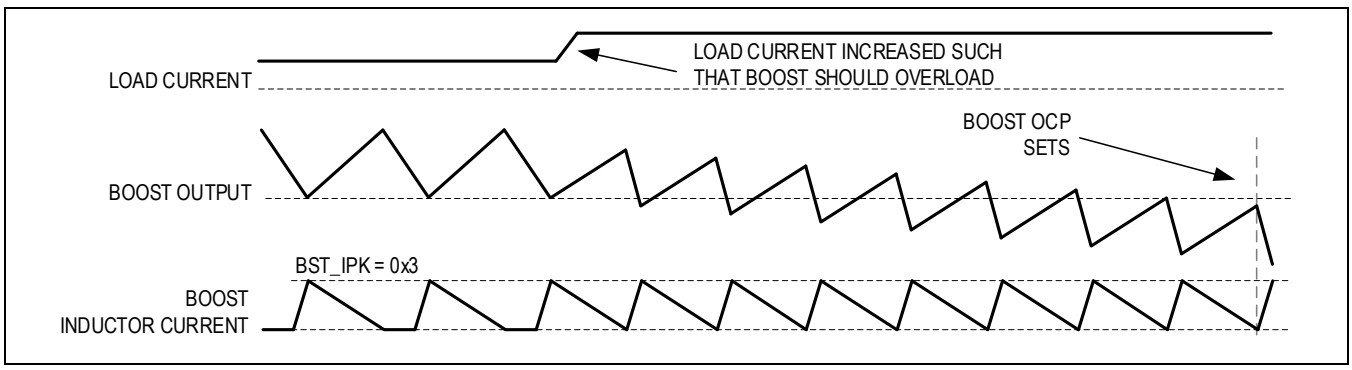


Figure 8. OCP Conditions for the Boost Converter when IPK_BST = 0x3

Additionally, the MAX77720 includes dedicated status, interrupt, and mask register bits. This is used to monitor overcurrent conditions and to notify application processors or microcontroller units of whether an overcurrent condition occurred (interrupt flag) and is still occurring (status flag). These bits can be found in the Register Map section under INT_GLBL0, INTM_GLBL0, and STAT_GLBL.

Output Short-Circuit Protection (SCP)

The MAX77720 has a short-circuit protection for the inverting buck-boost converter and boost converter.

For the inverting buck-boost converter, the output voltage is considered short-circuited if it is 40% of the target output voltage. If a short circuit is detected, the regulator disables after 10µs along with the status and interrupt bits reflecting the short circuit on the inverting buck-boost converter (INT_GLBL0.IBB_SCP = 1 and STAT_GLBL.IBB_SCP = 1). *Figure 9* shows the timing of the short-circuit protection implementation for the inverting buck-boost regulator.

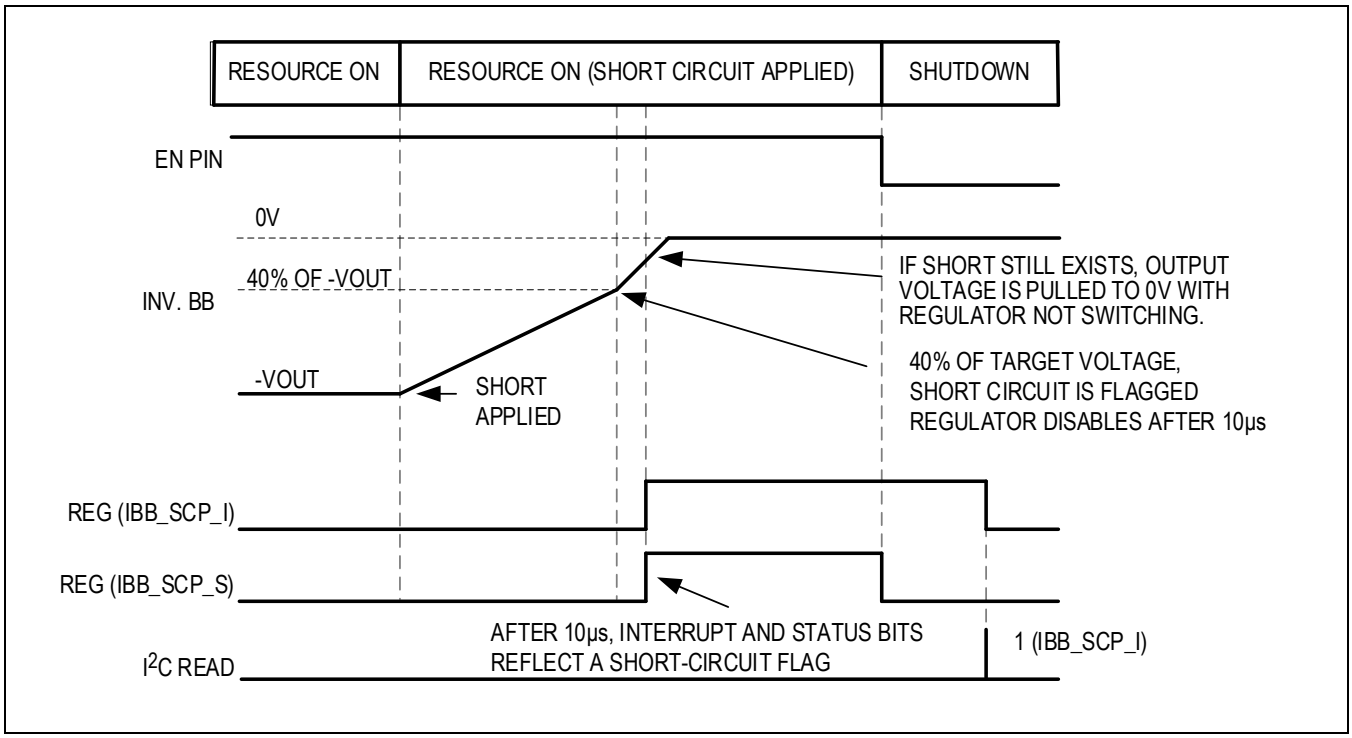


Figure 9. IBB Short-Circuit Protection Timing Diagram

For the boost converter, the output voltage is considered short-circuited if $V_{OUTBST} < V_{IN}$. If a short-circuit is detected, the regulator disables after 10µs along with the status and interrupt bits reflecting the short circuit on the boost converter (INT_GLBL0.BST_SCP = 1 and STAT_GLBL.BST_SCP = 1). *Figure 10* shows the timing of the short-circuit protection implementation for the boost regulator.

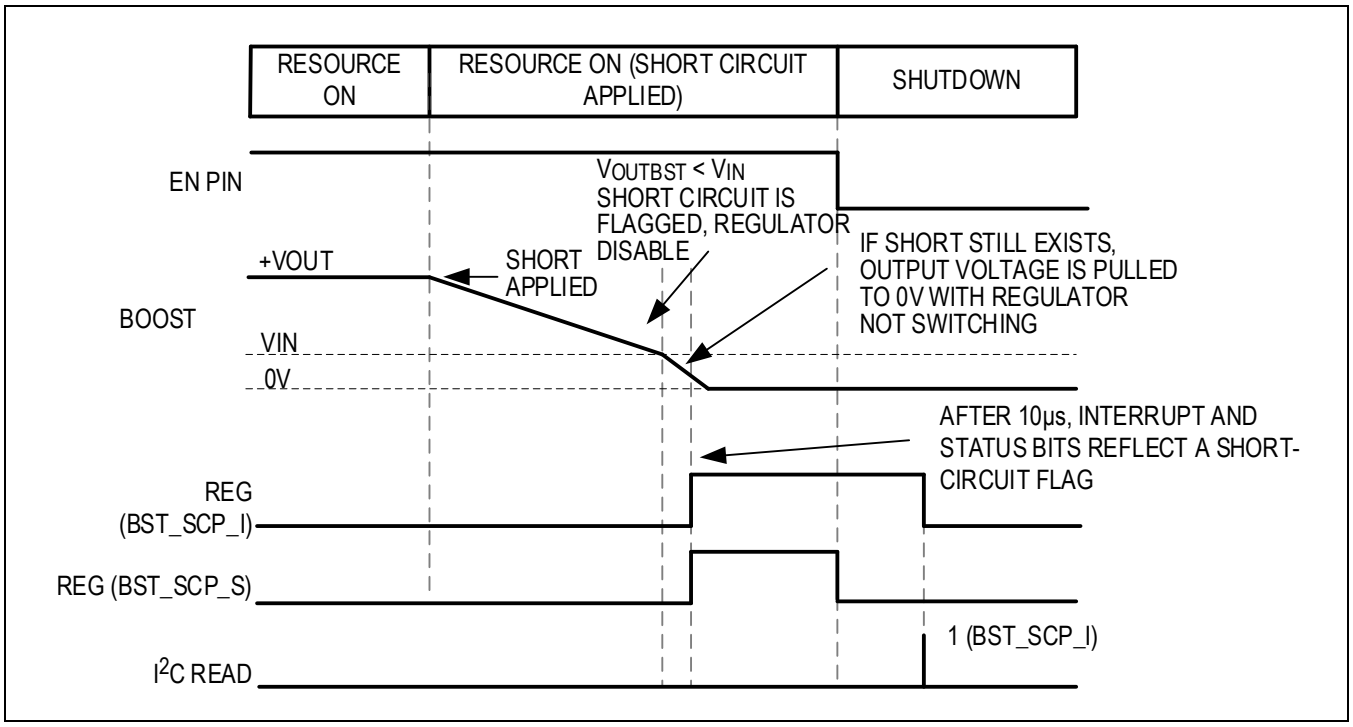


Figure 10. BST Short-Circuit Protection Timing Diagram

Additionally, the MAX77720 includes a dedicated status, interrupt, and mask register bits for monitoring the short-circuit conditions for each individual regulator. This is used to help monitor short-circuit conditions and to notify application processors or microcontroller units of whether a short-circuit condition occurred (interrupt flag) and is still occurring (status flag). These bits can be found in the Register Map section under INT_GLBL0, INTM_GLBL0, and STAT_GLBL.

To re-enable the regulators after a short-circuit condition, set the EN pin low, wait for the power-down delay time (see the *Power-Up/Power-Down* section), then set the EN pin high again. *Figure 11* shows how to re-enable the regulators as described above if a short circuit occurs on the inverting buck-boost regulator. Note that if CNFG_GLBL.FRC_IBB_ON = 1 or CNFG_GLBL.FRC_BST_ON = 1, a regulator can be enabled without waiting for the power-down delay time after a short-circuit event occurs.

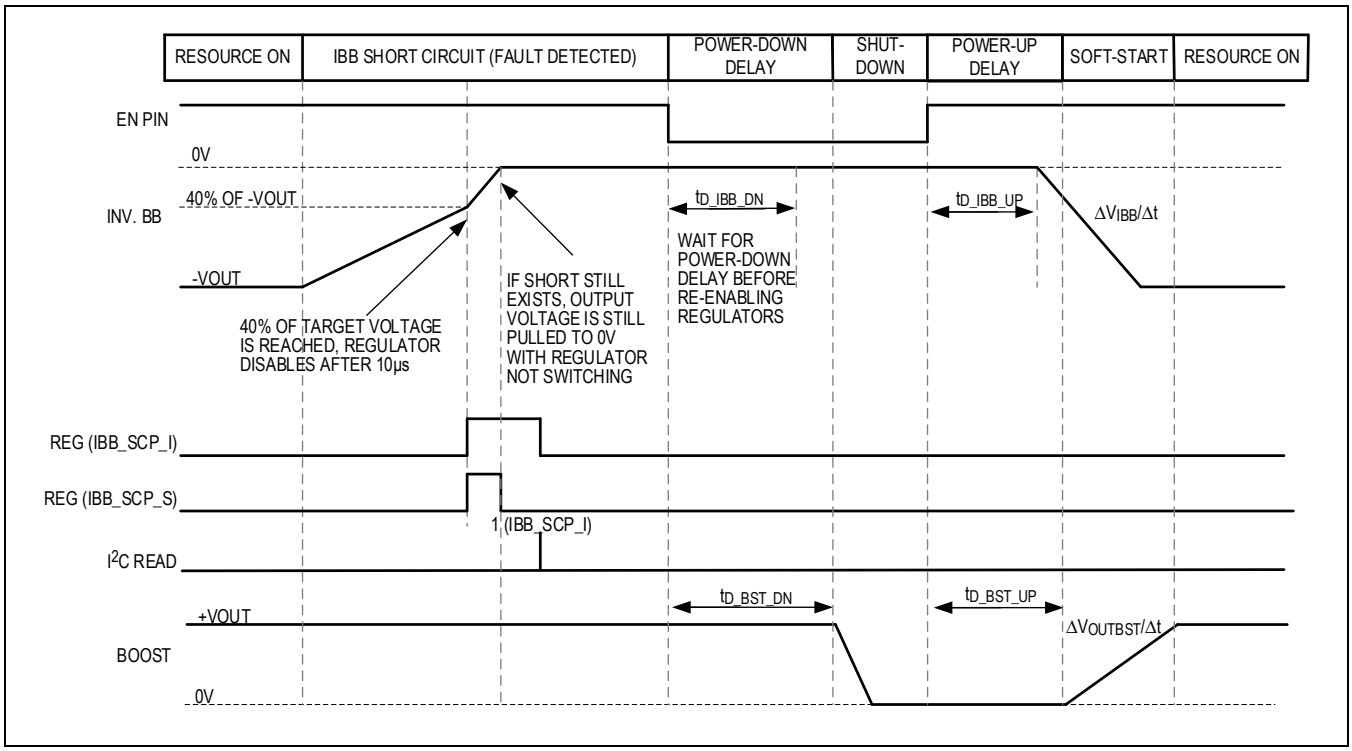


Figure 11. IBB Short-Circuit Protection Re-Enabling Timing Diagram

Detailed Description—Inverting Buck-Boost Converter

The asynchronous, inverting buck-boost converter generates a negative output voltage in two output voltage ranges: from -17.01V to -24.00V and from -17.00V to -10.01V, programmable through I²C. It is recommended that the inverting buck-boost converter is disabled before changing between output voltage ranges.

Inverting Buck-Boost Functional Modes

The MAX77720 inverting buck-boost converter operates in two functional modes: skip mode and PWM mode.

Skip Mode

The MAX77720 inverting buck-boost converter automatically enters skip mode at no load or light load conditions to improve efficiency. During this mode, the high-side MOSFET skips on pulses when the error amplifier output voltage is less than the target skip threshold. The target skip threshold determines the peak inductor current (400mA typ).

PWM Mode

The MAX77720 inverting buck-boost converter uses a peak current-mode control architecture with internal loop compensation at a 1.5MHz switching frequency pulse-width modulation. At the rising edge of each clock, the high-side MOSFET turns on and the inductor current ramps up. An internal error amplifier integrates the error between a fraction of the output voltage at the FBIBB pin and an internal reference. To program the duty cycle of the regulator, the output of the error amplifier sets the peak current in the inductor at which the high-side MOSFET turns off. Once the MOSFET turns off, the current in the inductor discharges the negative voltage rail (V_{OUT_IBB}) through the external Schottky diode. The inductor current continues to discharge V_{OUT_IBB} until the inductor current reaches zero or when the next rising clock edge is received.

Programming the Inverting Buck-Boost Output Voltage

The MAX77720 configures the inverting buck-boost output voltage through I²C. The target output voltage is between -10.01V and -17.00V in 15mV steps, while the range bit is high (CNFG_DCDC0.RNGIBB = 1). See *Table 5* for a summary of programmable voltage ranges and step sizes.

Table 5. Inverting Buck-Boost Output-Voltage Range

RANGE BIT	VIBB_RNG PROGRAMMABLE VOLTAGE RANGE (V)	VOLTAGE STEP PER LSB (mV)
Low Range (CNFG_DCDC0.RNGIBB = 0)	-17.01 to -24.00	15
High Range (CNFG_DCDC0.RNGIBB = 1)	-10.01 to -17.00	15

The CNFG_DCDC1.VOUTIBB and CNFG_DCDC2.VOUTIBB bitfields set the inverting buck-boost output voltage through a 9-bit (2-byte) configuration, to account for the wide programmable output range and voltage step size. The higher byte (CNFG_DCDC1.VOUTIBB) is latched to the lower byte (CNFG_DCDC2.VOUTIBB) so that the write command to change the output voltage is written together once the lower byte (CNFG_DCDC2.VOUTIBB) is written to. All 9 bits for V_{OUTIBB} are updated at the same time when the CNFG_DCDC1.VOUTIBB register is written to.

Only change the range of the inverting buck-boost while the converter is not switching. If the user decides to change the target output voltage of the inverting buck-boost from a higher absolute value to a lower absolute value (e.g., -24V to -17.01V), the rate at which it decreases highly depends on the output load condition and capacitance.

Detailed Description—Boost Converter

The step-up converter is a boost converter that generates a positive output voltage range from V_{IN} + 0.5V to 20V. The output voltage is programmable through external feedback resistors, see the *Configuring the Boost Output Voltage* section for more details. An internal power switching and internal catch diode allow for conversion efficiencies as high as 90%.

Boost-Converter Functional Modes

The MAX77720 boost converter operates in two functional modes: skip mode and PWM mode.

Skip Mode

The MAX77720 boost converter automatically enters skip mode through pulse frequency-modulation (PFM) to improve efficiency at light loads. In this mode, the on-time is determined by a peak inductor current limit of 500mA. Once the inductor current hits this limit, the on-time is terminated, and the power diode is forward-biased. During the off time, charge is transferred to the output capacitor causing the output voltage to rise. The off time gets terminated once the inductor current ramps down to zero. The load is supplied by the output capacitor and thus the output voltage declines.

When the FB voltage falls below the PFM reference voltage, the device initiates the on time again to bring the output voltage back up. In skip mode, the MAX77720 boost converter regulates the output voltage to 1% above the nominal output target. (**Note:** This threshold change does not apply to CNFG_IBB0.IPK_BST[1:0] = 0b11 as this mode only operates in DCM.)

PWM Mode

The MAX77720 boost converter uses a quasi-constant 1.0MHz switching frequency pulse-width modulation (PWM) at load current levels in CCM. (**Note:** This mode does not apply to CNFG_IBB0.IPK_BST[1:0] = 0b11 as this mode only operates in DCM.) Based on the input voltage to output voltage ratio, the circuit predicts the required off time. At the beginning of the switching cycle, the low-side MOSFET is turned on. In this phase, the input voltage is applied across the inductor and the inductor current ramps up while the output capacitor is discharged by the load current. When the inductor hits the current threshold that is set by the output error amplifier, the low-side MOSFET is turned off, and the power diode is forward-biased. In this phase, the inductor transfers its stored energy to the output capacitor to replenish the charge and supply the load current. When the off time expires, the next switching cycle starts again.

In PWM mode, the error amplifier compares the FBBST pin voltage with an internal reference voltage and the output of the error amplifier determines the inductor peak current. The MAX77720 boost converter has an internal compensation circuit that can accommodate a wide range of input voltage, output voltage, inductance, and output capacitance for stable operation.

Configuring the Boost Output Voltage

The MAX77720 configures the boost output voltage using an external resistor-divider. By selecting the external resistor-divider R_{TOP} and R_{BOT}, the output voltage is configured to the desired value. When the output voltage is regulated, the typical voltage at the FBBST pin is 1.25V.

Calculate the value of R_{TOP} (from V_{FBBST} to V_{OUTBST}) for a desired V_{OUTBST} at startup with the following equation:

$$R_{TOP} = R_{BOT}\ x\ \left(\frac{V_{OUTBST}}{V_{FBBST}} - 1\right)$$

Where:

- V_{OUTBST} is the desired positive output voltage
- V_{FBBST} is the default internal reference voltage at the FBBST pin, 1.25V (typ)

For best accuracy, set R_{BOT} to a value smaller than 475kΩ to ensure that the current flowing through it is significantly larger than the FBBST pin bias current. The advantage of using a higher value for R_{BOT} is the reduction of quiescent current for achieving the highest efficiency at light load currents. However, using R_{BOT} values that are lower increases immunity against noise injection. Additionally, using one percent tolerance resistors (or better) are recommended to maintain high output-voltage accuracy.

Figure 12 shows a small circuit diagram of the feedback network.

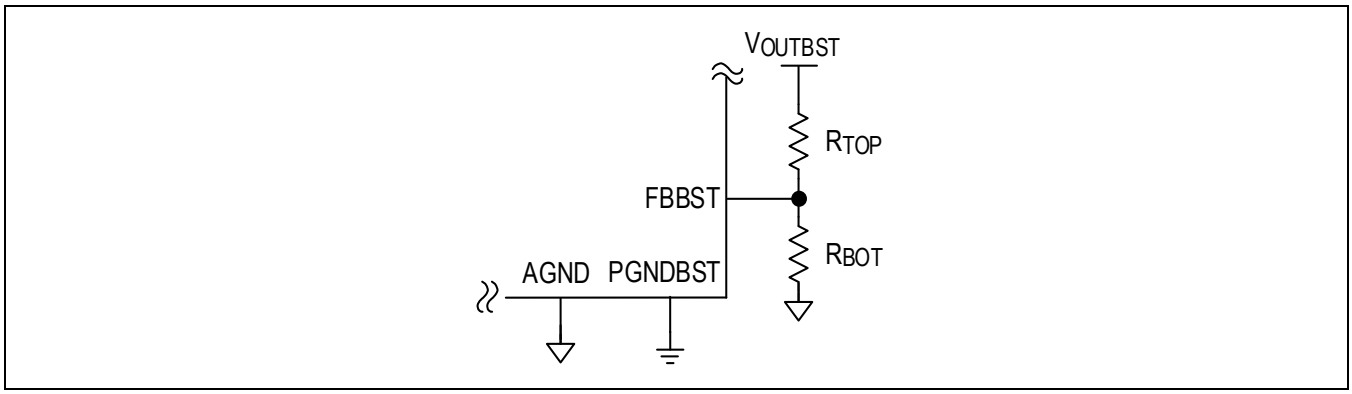


Figure 12. Connecting External Feedback Network

Detailed Description—Two-Wire Communication

General Description

The MAX77720 uses a 2-wire bus system to communicate by standard I2C protocol. The target address used by the host to access the IC determines what memory locations are available to read or write.

System Configuration

The 2-wire bus system supporter operation as a target-only device in a single or multitarget, and single or multicontroller system. Using a 7-bit target address, the system can support up to 128 target addresses. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the IC and a controller device at speeds up to 1MHz.

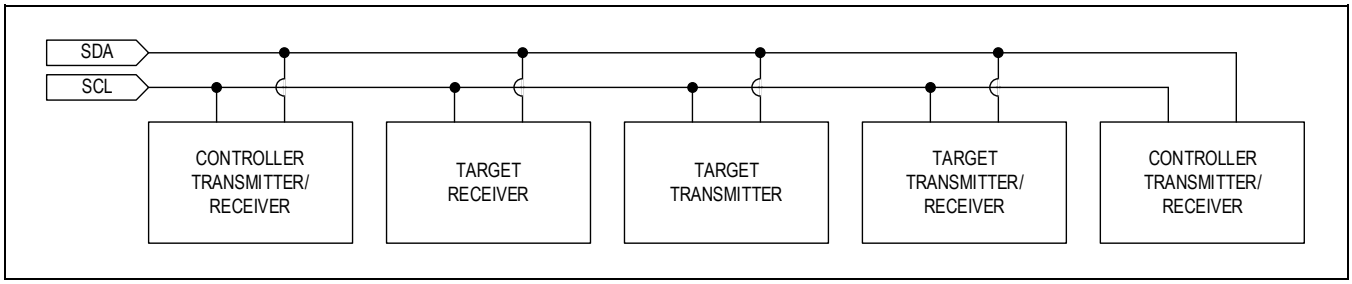


Figure 13. Functional Logic Diagram for the Communications Controller

Figure 13 shows an example of a typical I2C bus system. A device on the I2C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. A device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a controller. Any device being addressed by the controller is called a target. The MAX77720 is a target on the I2C bus. The IC's SDA pin operates bidirectionally. When the IC receives data, the SDA operates as an input. When the IC returns data, the SDA operates as an open-drain output with the host system providing a resistive pull-up. The IC always operates as a target device, receiving and transmitting data under the control of a controller device. The controller initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits which begin and end each transaction.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on the SDA must remain stable during the high portion of the SCL clock pulse. Changes in the SDA while the SCL is high are control signals (START and STOP conditions). See Figure 14 for an example.

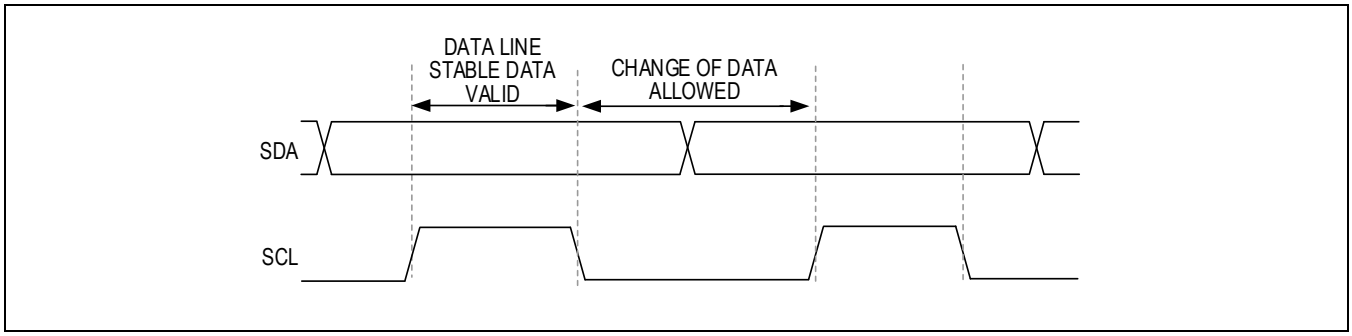


Figure 14. I²C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, the SDA and SCL idle high. A controller device initiates communication by issuing a START condition (S). A START condition (S) is a high-to-low transition on the SDA while the SCL is high. A STOP condition (P) is a low-to-high transition on the SDA while the SCL is high. Figure 15 demonstrates the START and STOP conditions.

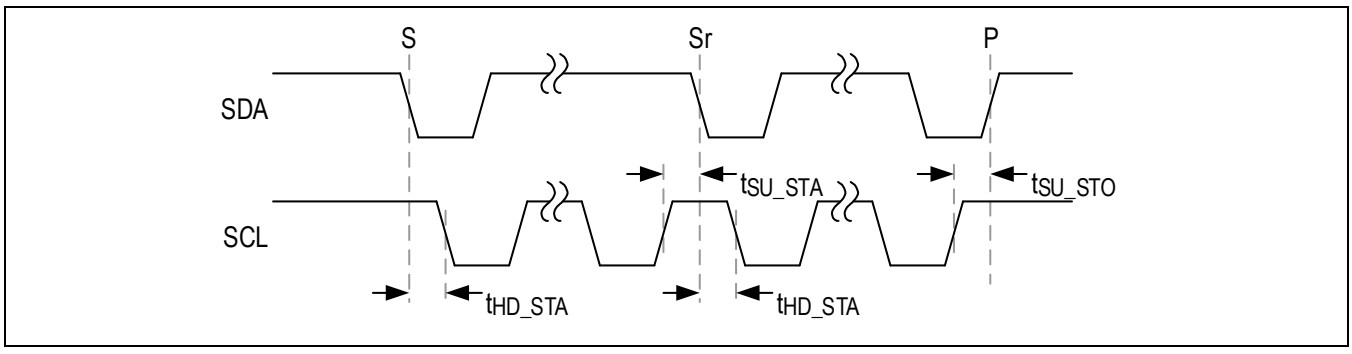


Figure 15. START and STOP Conditions

A START condition (S) from the controller device signals the beginning of a transmission. The controller terminates transmission by issuing a NOT ACKNOWLEDGE (NACK) followed by a STOP condition (P). A STOP condition (P) frees the bus. To issue a series of commands to the target, the controller can issue REPEATED START (Sr) commands instead of a STOP condition (P) to maintain control of the bus. In general, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S). When a STOP condition (P) or incorrect address is detected, the MAX77720

internally disconnects the SCL from the I2C serial interface until the next START condition (S), minimizing digital noise and feedthrough.

Acknowledge Bit

Both I2C bus controller device and target devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an ACKNOWLEDGE (ACK), the receiving device must pull the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high portion of the clock pulse. To generate a NOT ACKNOWLEDGE (NACK), the receiving device allows the SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high portion of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller should reattempt communication at later time. *Figure 16* shows the timing for when the device has an ACKNOWLEDGE and NOT-ACKNOWLEDGE condition.

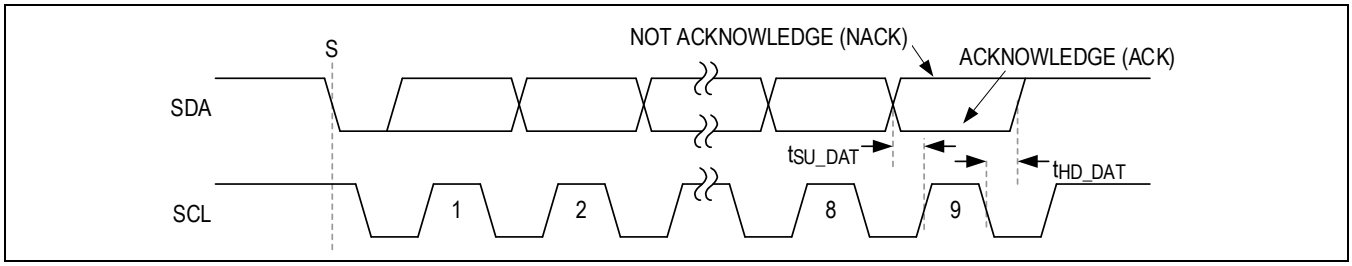


Figure 16. Acknowledge Bit

Data Order

With 2-wire communication, a byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSB) of each byte is followed by the ACKNOWLEDGE bit. IC registers composed of multibyte values are ordered least significant byte (LSB) first.

Target Address

The I2C controller implements 7-bit target addressing. An I2C bus controller initiates communication with the target by issuing a START condition followed by the target address. See *Figure 17*. The OTP address is factory programmable for one of four options (see *Table 6*). All target addresses not mentioned in *Table 6* are not acknowledged.

Table 6. I2C Target Addresses

ADDRESS	7-BIT TARGET ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR[1:0]= 0x0)*	0x41, 0b 100 0001	0x82, 0b 1000 0010	0x83, 0b 1000 0011
Main Address (ADDR[1:0] = 0x1)*	0x42, 0b 100 0010	0x84, 0b 1000 0100	0x85, 0b 1000 0101
Main Address (ADDR[1:0] = 0x2)*	0x6A, 0b 110 1010	0xD4, 0b 1101 0100	0xD5, 0b 1101 0101
Main Address (ADDR[1:0] = 0x3)*	0x6B, 0b 110 1011	0xD6, 0b 1101 0110	0xD7, 0b 1101 0111
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

**Perform all reads and writes on the main address. The ADDR is a factory one-time programmable (OTP) option allowing for address changes in the event of a bus conflict. Contact* Analog Devices *for more information.*

***When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rate even when debugging needs to be performed in cooperation with Analog Devices.*

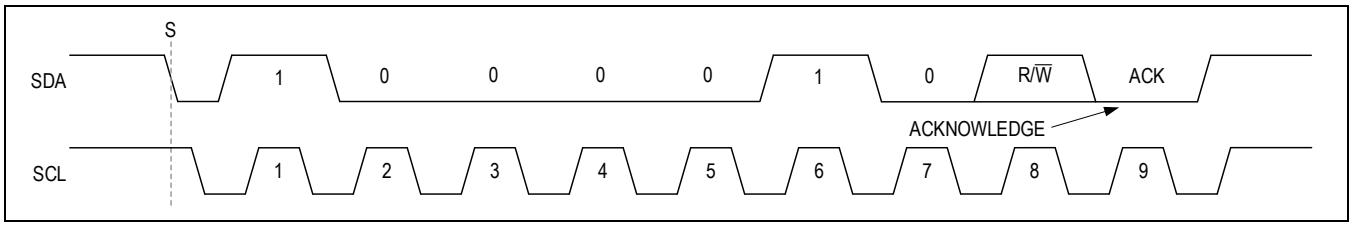


Figure 17. Target Address Byte Example—SDA Shows the 7-Bit Target Address at 0x42

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the controller device. The I2C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The MAX77720 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77720 does not implement the general call address from the I2C specification and does not issue an acknowledge for a general call address (0b0000 0000).

Communication Speed

The MAX77720 supports the following communication speeds outlined in the I2C Rev. 7.0 specification:

- 0Hz to 100kHz (Standard-mode)
- 0Hz to 400kHz (Fast-mode)
- 0Hz to 1MHz (Fast-mode Plus)

Operating in Standard-mode, Fast-mode, and Fast-mode Plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pull-up resistors. Higher time constants created by the bus capacitance and pull-up resistance (C x R) slow the bus operation. Therefore, when increasing bus speed, the pull-up resistance must be decreased to maintain a reasonable time constant. See the pull-up resistor sizing section of the I2C Rev. 7.0 specification for detailed guidance on the pull-up resistor selection. In general, for a bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pull-up resistors and a 400kHz bus needs approximately 1.5kΩ pull-up resistors, and a 1MHz bus needs 680Ω pull-up resistors. Note that the pull-up resistor dissipates power when the open-drain bus is low. The lower the value of the pull-up resistor, the higher the power dissipation (V^2/R). Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I2C Rev. 7.0 specification. The major considerations with respect to the MAX77720 are as follows:

- Controller device uses current source pull-ups to shorten the signal rise times
- Target device must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed
- Communication protocols need to utilize the high-speed controller code

At power-up and after each STOP condition (P), the MAX77720 inputs filters that are set for Standard-mode, Fast-mode, and/or Fast-mode Plus (i.e., 0Hz to 1MHz).

Communication Protocols

The MAX77720 supports both writing to and reading from its registers as described in the following subsections.

Writing to a Single Register

Figure 18 shows the protocol for writing to a single register. This protocol is the same as the write byte protocol in the SMBus specification.

The write byte protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling the SDA low.

4. The controller sends an 8-bit register pointer.

5. The target acknowledges the register pointer.

6. The controller sends a data byte.

7. The target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.

8. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

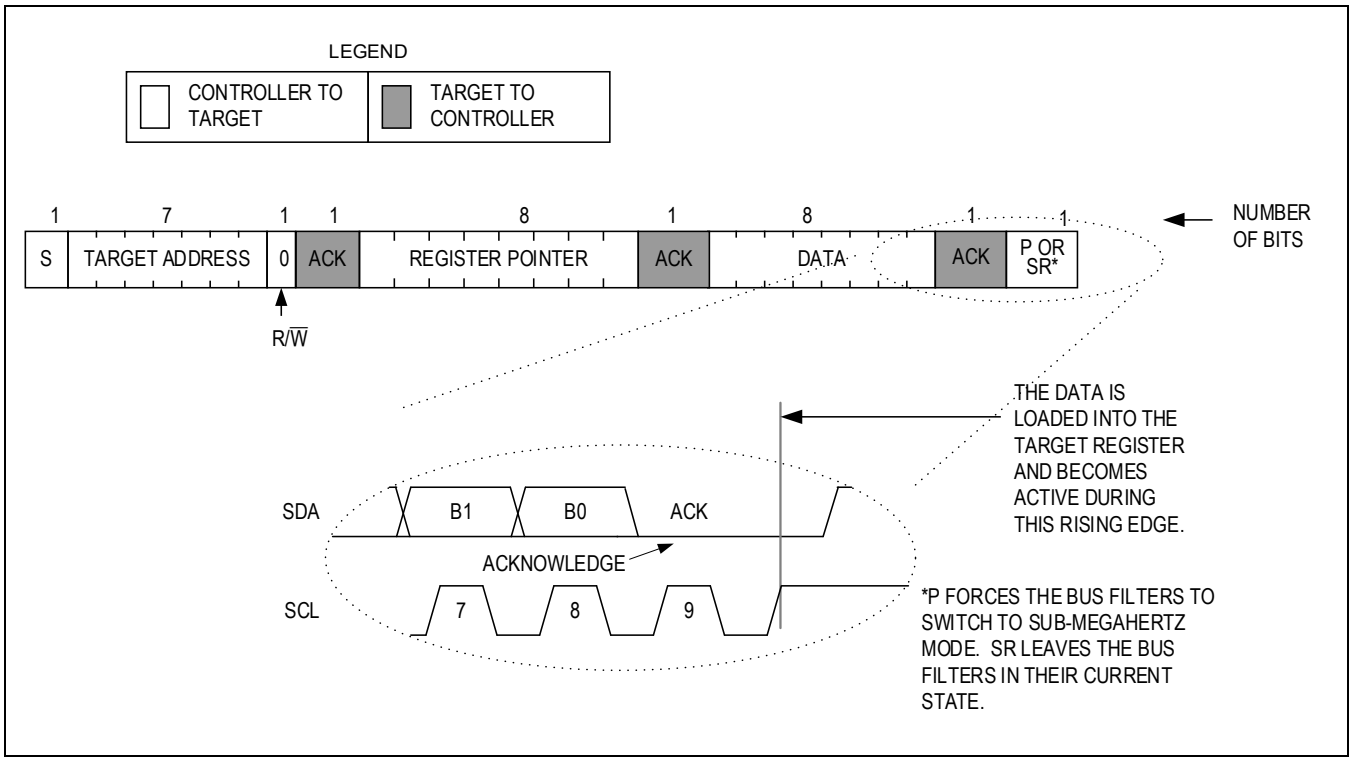


Figure 18. Writing to a Single Register

Writing to Sequential Registers

Figure 19 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol, except the controller device continues to write after the target device receives the first byte of data. When the controller is done writing data, it issues a STOP condition (P) or REPEATED START condition (Sr).

The writing to sequential registers protocol is as follows:

1. The controller sends a START condition (S).

2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).

3. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling the SDA LOW.

4. The controller sends an 8-bit register pointer.

5. The target acknowledges the register pointer.

6. The controller sends a data byte.

7. The target acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.

8. Step 6 to step 7 are repeated as many times as the controller requires.

9. During the last acknowledge-related clock pulse, the target issues an ACKNOWLEDGE (ACK).

10. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

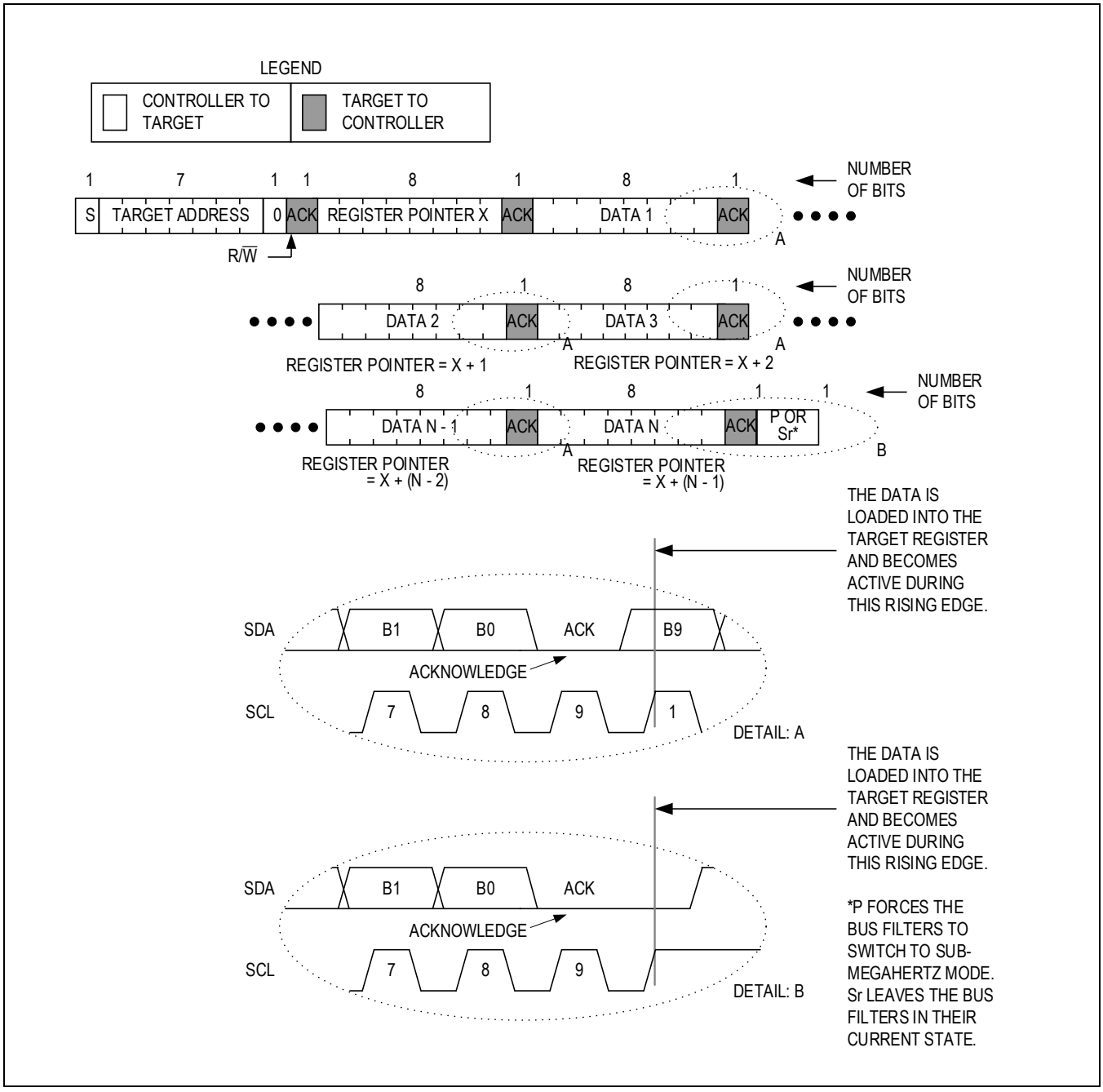


Figure 19. Writing to Sequential Registers

Reading from a Single Register

Figure 20 shows the protocol for reading from a single register. This protocol is the same as the read byte protocol in the SMBus specification.

The read byte protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling the SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling SDA low.
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.
10. The controller issues a NOT ACKNOWLEDGE (NACK).
11. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

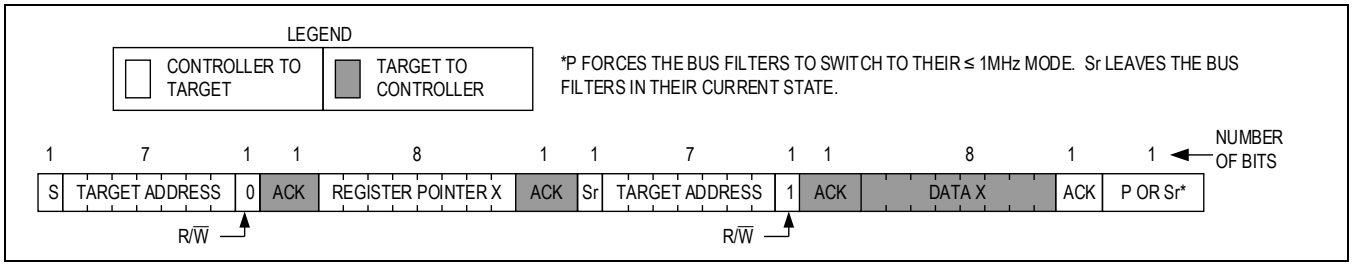


Figure 20. Reading to a Single Register

Reading from Sequential Registers

Figure 21 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol, except the controller device issues an ACKNOWLEDGE (ACK) to signal the target device that it wants more data. When the controller device has all the data it requires, it issues a NOT ACKNOWLEDGE (NACK) and a STOP condition (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The controller sends a START condition (S).
2. The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling the SDA LOW.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a REPEATED START command (Sr).
7. The controller sends the 7-bit target address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed target asserts an ACKNOWLEDGE (ACK) by pulling the SDA LOW.
9. The addressed target places 8 bits of data from the location specified by the register pointer on the bus.

10. The controller issues an ACKNOWLEDGE (ACK) signaling the target that it wishes to receive more data.

11. Step 9 to step 10 are repeated as many times as the controller requires. Following the last byte of data, the controller must issue a NOT ACKNOWLEDGE (NACK) to signal that it wishes to stop receiving data.

12. The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

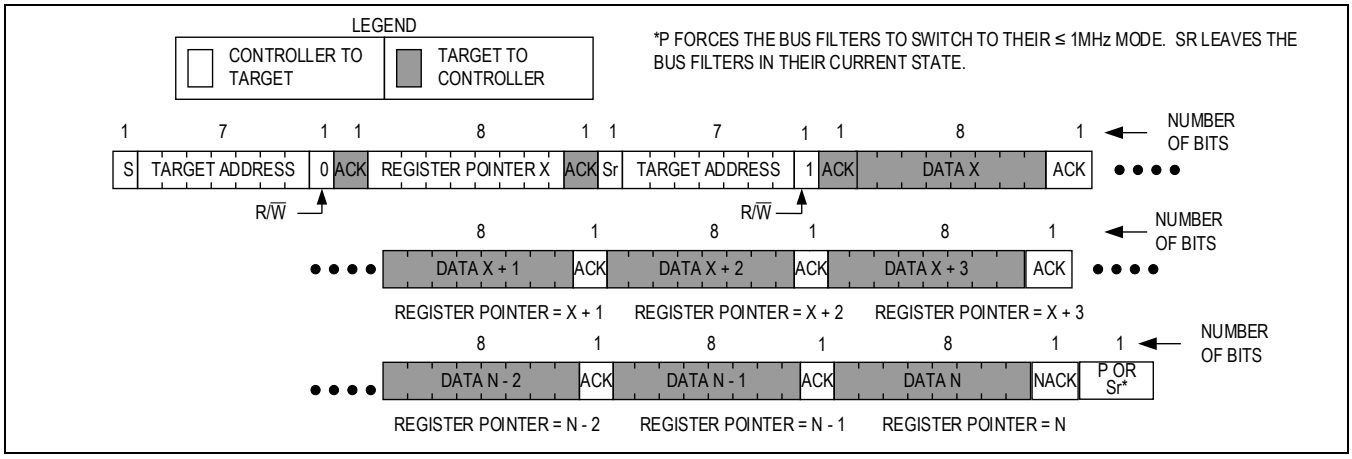


Figure 21. Reading from Sequential Registers

Applications Information

Inverting Buck-Boost and Boost Enable Options

The MAX77720 offers a high degree of control flexibility. The EN pin can be used to enable both the boost and inverting buck-boost with its respective programmed delays (CNFG_DLY0.STRTUP_DLY_BST and CNFG_DLY1_STRTUP_DLY_IBB). The boost converter can be forced on with no delay by I^2C by setting CNFG_GLBL.FRC_BST_ON = 1. Similarly, the inverting buck-boost converter can also be forced on with no delay through I^2C by setting CNFG_GLBL.FRC_IBB_ON = 1.

Input-Capacitor Selection

Input capacitors reduce current peaks drawn from the battery or input power source and reduce switching noise in the system. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low, ESR, and small temperature coefficients. Other capacitor types can be used as well, but at a tradeoff of higher ESR.

It is recommended to have a minimum 12µF effective capacitance between the INIBB pin and PGND and a minimum 12µF effective capacitance between the boost inductor and PGND. Both of these capacitors should be placed as close to the IC as possible.

Additionally, it is recommended to have a 1µF bypass capacitor between the IN pin and AGND. This is to ensure stable operation of the MAX77720 and to reduce any noise injections that might affect the performance of the IC.

To fully utilize the available input-voltage range of the device (5.5V max), use a input capacitor voltage rating of at least 6.3V).

Inverting Buck-Boost Inductor Selection

The MAX77720 inverting buck-boost converter is optimized for a 3.3µH inductor.

Choose an inductor with a saturation current that is greater than or equal to the maximum peak current limit setting (I_{IBB_ILIM}).

Consider the DC resistance (DCR), AC resistance (ACR), and package size of the inductor. Typically, smaller sized inductors have larger DCR and ACR, which reduce efficiency. Refer to the manufacturer data sheet to balance the trade-offs between DCR, ACR (i.e., core losses), variation with temperature, and component cost.

Inverting Buck-Boost Diode Selection

The MAX77720 inverting buck-boost converter is an asynchronous converter which requires an external diode. A Schottky diode is recommended for best performance with a low forward-voltage drop and a fast-switching action.

For the low range (-17.01V to -24V), choose a Schottky diode with a reverse voltage (V_R) below -40V and a minimum forward current (I_{FW}) of 1.5A.

For the high-range (-10.01V to -17V), choose a Schottky diode with a (V_R) reverse voltage below -30V and a minimum forward current (I_{FW}) of 1.5A.

These recommendations provide high robustness and best efficiency for small form factor diodes.

Inverting Buck-Boost Output Capacitor Selection

Sufficient output capacitance (C_{OUT_IBB}) is required for stable operation of the inverting buck-boost. Choose the effective C_{OUT_IBB} to be 4.7µF minimum.

Effective C_{OUT_IBB} is the actual capacitance value seen by the DC-DC converter during operation. Choose effective C_{OUT_IBB} carefully by considering the capacitor's initial tolerances, variation with temperature, and derating with DC bias.

Larger values of C_{OUT_IBB} (above the required effective minimum capacitance) improve load transient performance and ripple performance but increase the input surge currents during soft-start. The output filter capacitor must have low enough ESR to meet the output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case-size capacitors derate heavily compared to larger case sizes (0805 case size performs better than 0603).

Additionally, ceramic capacitor absolute maximum-voltage ratings must be considered due to the high absolute output voltage (down to -24V). For applications that use the inverting buck-boost low range (-17.01V to -24V), it is recommended to use 50V rating capacitors for better reliability. For applications that are using the inverting buck-boost high range (-10.01V to -17V), it is recommended to use 35V rating capacitors for better reliability. Refer to the manufacturer data sheet for proper DC bias, AC ripple, and temperature capacitance derating.

Boost-Inductor Selection

Because the selection of the inductor affects steady-state operation, transient behavior, and loop stability, the inductor is the most important component in a boost power-converter design. The three major specifications to consider are: inductance value, saturation current, and DC resistance. The MAX77720 boost converter is designed to work with inductor values between 4.7µH and 15µH. Additionally, choose an inductor with a saturation current that is greater than or equal to the programmed peak current-limit setting (I_{BST_ILIM}) depending on the application.

Use the following equations to calculate the inductor's peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with -30% tolerance and a low-power conversion efficiency for the calculation.

The inductor's DC current ($I_{IL(DC)}$) in amperes can be calculated using the following formula:

$$I_{L(DC)} = (V_{OUT\_BST} \times I_{OUT\_BST})/(V_{IN} \times \eta)$$

Where:

V_{OUT_BST} = Boost output voltage.

I_{OUT_BST} = Boost output current.

V_{IN} = Input voltage.

η = Power conversion efficiency; use 80% for most applications.

The inductor ripple current ($\Delta I_{L(PK-PK)}$) in amperes is calculated with the following equation for an asynchronous boost converter in CCM.

$\Delta I_{L(PK-PK)} = (V_{IN} \times (V_{OUT\_BST} + 0.4V - V_{IN}))/((L \times f_{SW} \times (V_{OUT} + 0.4V))$

Where:

$\Delta I_{L(PK-PK)}$ = peak-to-peak inductor ripple current in amperes.

L = Inductance value.

f_{SW} = Switching frequency, 1MHz (typ).

V_{OUT_IBB} = Output voltage.

V_{IN} = Input voltage.

0.4V = Typical diode drop voltage.

Therefore, the inductor peak current ($I_{L(PK)}$) in amperes is calculated with this equation:

$I_{L(PK)} = I_{L(DC)} + (\Delta I_{L(PK-PK)}/2)$

Normally, if the power supply is expected to operate in CCM, it is advisable to work with an inductor peak-to-peak current ripple of less than 40% of the average inductor current. Smaller ripple from a larger valued inductor reduces EMI and the magnetic losses in the inductor. However, load-transient response time is increased. Because the MAX77720 is used for relatively small output-current applications, the inductor peak-to-peak current ripple can be higher, in which case the MAX77720 operates mostly in the discontinuous current mode (DCM) of operation.

For a general recommendation for the application, choose an inductor value based on the V_{OUT_BST} setting (see *Table 7*).

Table 7. Boost Inductor-Value Recommendation

V_{OUT_BST} (V)	L (µH)
5.5 to 7	4.7
7 to 9	6.8
9 to 11	8.2
11 to 17	10
17 to 20	15

Boost Output-Capacitor Selection

Sufficient output capacitance (C_{OUT_BST}) is required for stable operation of the boost. For output voltages at 8V and below, choose 12µF effective capacitance minimum. For output voltages above 8V, choose 6µF effective capacitance minimum.

Like the inverting buck-boost converter, the effective C_{OUT_BST} is the actual capacitance value seen by the DC-DC converter during operation. Choose the effective C_{OUT_BST} carefully by considering the capacitor's initial tolerances, variation with temperature, and derating with DC bias.

Additionally, ceramic capacitor absolute maximum voltage ratings must be considered due to the high absolute output voltage (up to +20V). For applications that use the output voltage range at 14V and higher, it is recommended to use 35V or 50V rating capacitors. For applications that use the output voltage range below 14V, it is recommended to use 20V rating capacitors (or higher) for better reliability. Refer to the manufacturer data sheet for proper DC bias, AC ripple, and temperature capacitance derating.

The boost output capacitor affects the small-signal control loop stability of the boost converter. If the output capacitor is below the range, the boost converter can potentially become unstable. Increasing the output capacitor makes the output voltage rippler smaller. In applications where V_{IN} is approaching V_{OUT_BST}, more output capacitance is required to minimize the output-voltage ripple.

General PCB Layout Guidelines

Careful printed circuit board layout is critical to achieve low-switching power losses, and a clean stable operation by increasing noise immunity.

When laying out the PCB, follow these general guidelines:

- Place the inductors and output capacitors of the DC-DC converters close to the MAX77720 and keep the power loop small.
- When routing the current path of the DC-DC converters, short and wide traces should be used to reduce any EMI issues radiated from the fast switching. The trace between LX pin and the inductor is the most critical for this.
- The ground loop for the input and output capacitor should be as small as possible.
- For multilayer PCBs, analog ground (AGND) should be its own plane and power ground (PGND) should be its own separate plane. AGND should be directly connected to the ground plane separately, to ensure a quiet ground plane for AGND and to avoid common impedance grounding.
- The feedback pins should be routed away from the LX switching node to increase noise immunity. This pin is a high-impedance input which is highly noise sensitive.
- When possible, ground planes and traces should be used to help shield the feedback signal and minimize noise and magnetic interference. For multilayer PCBs, a ground plane should be in between the high current paths and any analog or digital paths.

Example PCB Layout

Figure 22 shows an example layout of the top layer with additional digital signals shown beneath the top layer. For component details and EV kit recommendations, refer to the MAX77720EVKIT# data sheet.

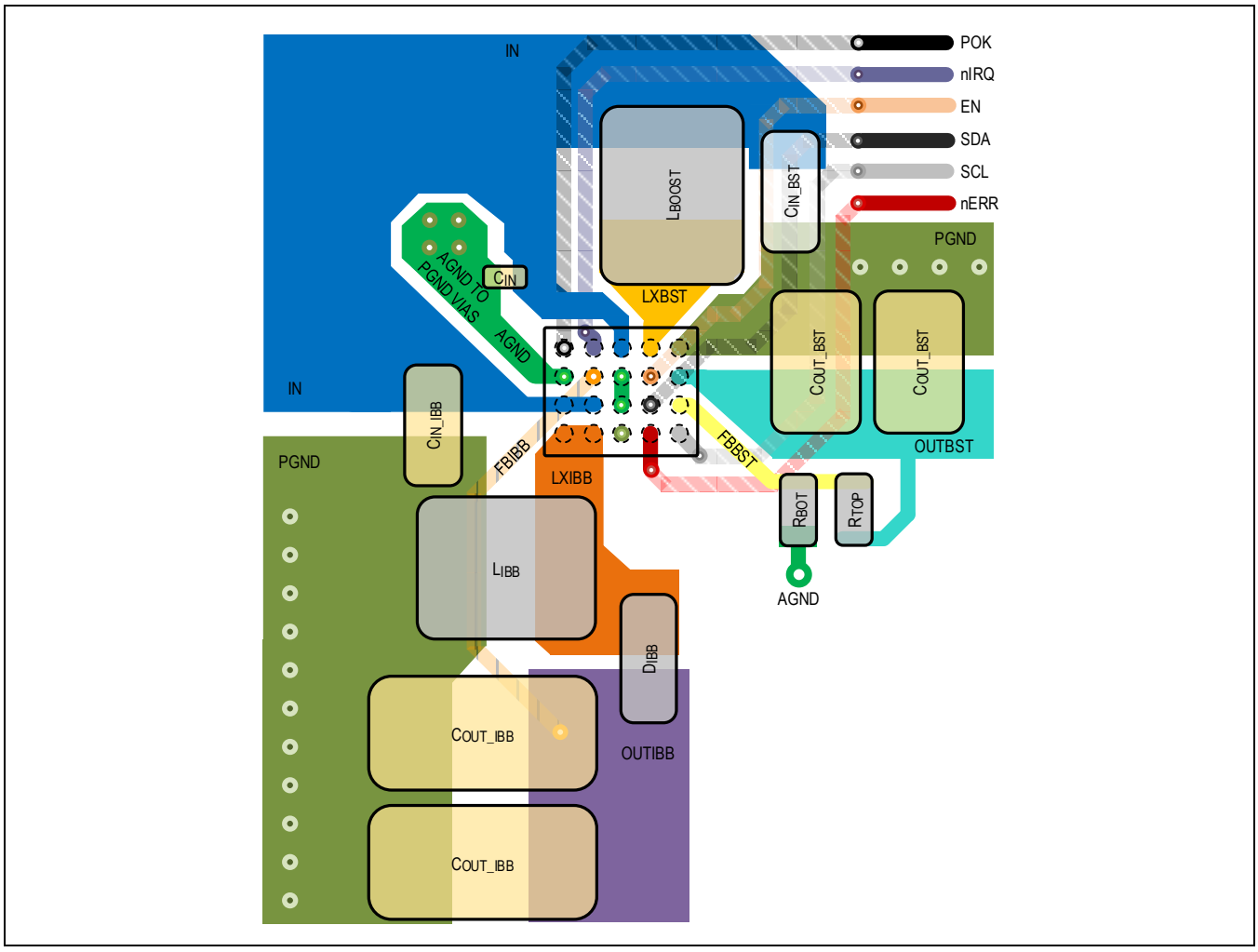


Figure 22. PCB Top Layer and Component Placement Example

Typical Application Circuits

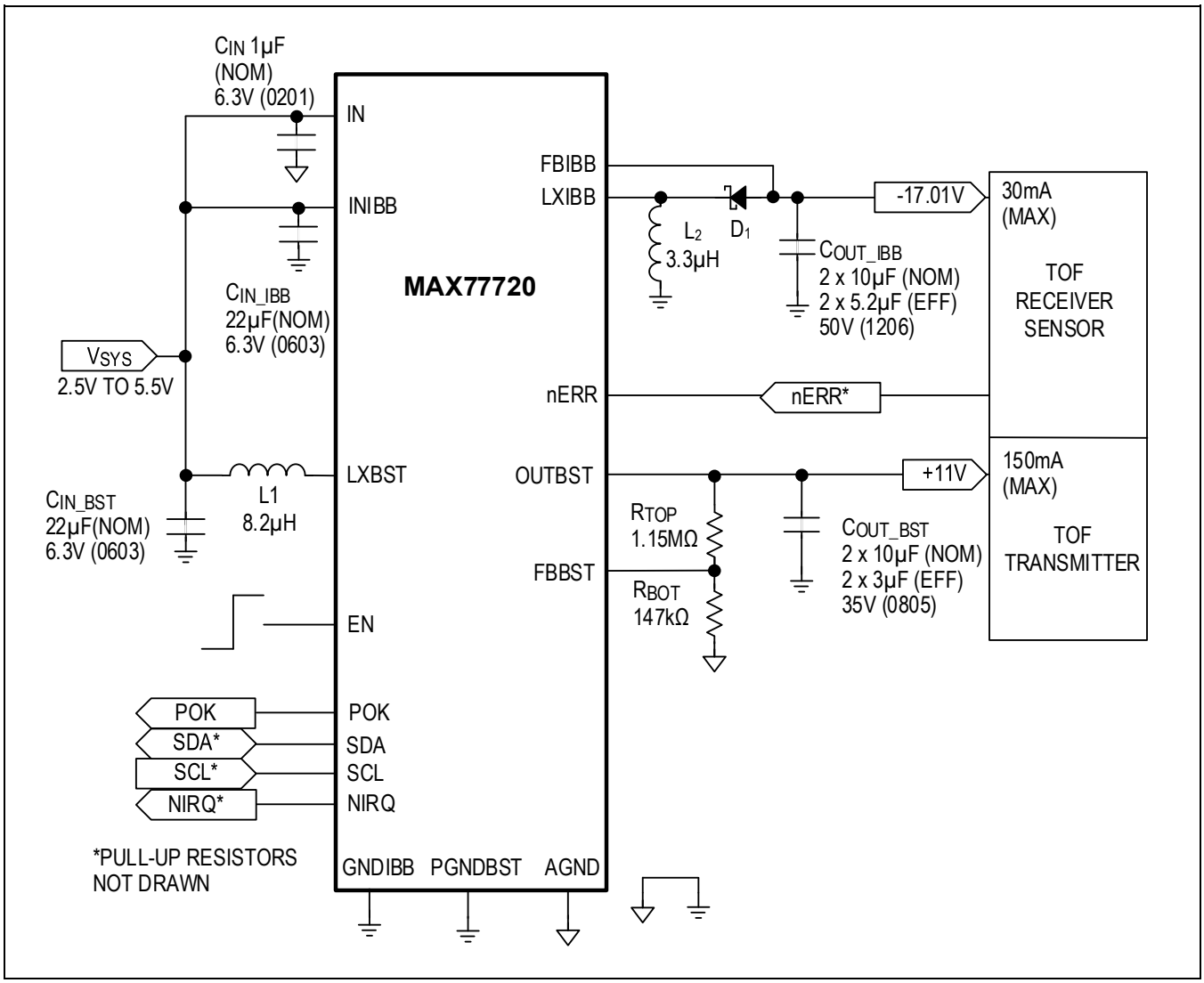


Figure 23. Typical Application Circuit

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x01	INT_GLBL0[7:0]	RSVD	POK_IBB_I	POK_BST_I	IBB_SCP_I	BST_SCP_I	IBB_OCP_I	BST_OCP_I	ERR_PIN_I
0x02	INTM_GLBL0[7:0]	RSVD	POK_IBB_M	POK_BST_M	IBB_SCP_M	BST_SCP_M	IBB_OCP_M	BST_OCP_M	ERR_PIN_M
0x03	STAT_GLBL[7:0]	RSVD	POK_IBB_S	POK_BST_S	IBB_SCP_S	BST_SCP_S	IBB_OCP_S	BST_OCP_S	ERR_PIN_S
0x04	ERCFLAG[7:0]	–	–	–	–	OVLO	UVLO	OTLO	RSVD
0x05	CNFG_GLBL[7:0]	–	–	–	–	EN_BIAS	FRC_IBB_ON	FRC_BST_ON	FORCE_DIS
User Registers									
0x30	CNFG_DCDC0[7:0]	–	RNG_IBB	SS_IBB	ADE_IBB	RSVD	IPK_BST[1:0]		ADE_BST
0x31	CNFG_DCDC1[7:0]	–	–	–	–	RSVD	RSVD	RSVD	VOUT_IBB
0x32	CNFG_DCDC2[7:0]	VOUT_IBB[7:0]							
0x40	CNFG_DLY0[7:0]	STRTUP_DLY_IBB[3:0]				PWRDN_DLY_IBB[3:0]			
0x41	CNFG_DLY1[7:0]	STRTUP_DLY_BST[3:0]				PWRDN_DLY_BST[3:0]			

Register Details

INT_GLBL0 (0x1)

POK and Interrupt Source Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	POK_IBB_I	POK_BST_I	IBB_SCP_I	BST_SCP_I	IBB_OCP_I	BST_OCP_I	ERR_PIN_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	
POK_IBB_I	6	Power-OK Inverting Buck-Boost Interrupt	0x0: Buck-boost output voltage is above POK threshold 0x1: Buck-boost output voltage is below POK threshold
POK_BST_I	5	Power-OK Positive Boost Interrupt	0x0: Boost output voltage is below POK threshold 0x1: Boost output voltage is above POK threshold
IBB_SCP_I	4	Inverting Buck-Boost Short-Circuit Protection Interrupt	0x0: Buck-boost output short clrcuit is not detected 0x1: Buck-boost output short circuit is detected
BST_SCP_I	3	Boost Short-Circuit Protection Interrupt	0x0: Boost output short clrcuit is not detected 0x1: Boost output short circuit is detected
IBB_OCP_I	2	Inverting Buck-Boost Overcurrent Protection Interrupt	0x0: Inverting buck-boost output was not overloaded since the last time this bit was read 0x1: Inverting buck-boost output was overloaded since the last time this bit was read
BST_OCP_I	1	Boost Overcircuit Protection Interrupt	0x0: Boost output was not overloaded since the last time this bit was read 0x1: Boost output was overloaded since the last time this bit was read
ERR_PIN_I	0	Error Pin Interrupt	0x0: Sensor error has not been detected 0x1: Sensor error has been detected

INTM_GLBL0 (0x2)

POK and Interrupt Mask Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	POK_IBB_M	POK_BST_M	IBB_SCP_M	BST_SCP_M	IBB_OCP_M	BST_OCP_M	ERR_PIN_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	
POK_IBB_M	6	Power-OK Interrupt Mask	0x0: Power-OK for buck-boost status is not masked 0x1: Power-OK for buck-boost status is masked (default)
POK_BST_M	5	Power-OK Interrupt Mask	0x0: Power-OK for boost status is not masked 0x1: Power-OK for boost status is masked (default)
IBB_SCP_M	4	Inverting Buck-Boost Short-Circuit Protection Interrupt Mask	0x0: Inverting buck-boost output short-circuit interrupt is not masked 0x1: Inverting buck-boost output short-circuit interrupt is masked (default)
BST_SCP_M	3	Boost Short-Circuit Protection Interrupt Mask	0x0: Boost output short-circuit interrupt is not masked 0x1: Boost output short-circuit interrupt is masked (default)
IBB_OCP_M	2	Inverting Buck-Boost Overload Protection Interrupt Mask	0x0: Inverting buck-boost output overcurrent interrupt is not masked 0x1: Inverting buck-boost output overcurrent interrupt is masked (default)

BITFIELD	BITS	DESCRIPTION	DECODE
BST_OCP_M	1	Boost Short-Circuit Protection Mask	0x0: Boost output overcurrent interrupt is not masked 0x1: Boost output overcurrent interrupt is masked (default)
ERR_PIN_M	0	Error Pin Interrupt Mask	0x0: Error-pin interrupt is not masked 0x1: Error-pin interrupt is masked (default)

STAT_GLBL (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	POK_IBB_S	POK_BST_S	IBB_SCP_S	BST_SCP_S	IBB_OCP_S	BST_OCP_S	ERR_PIN_S
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	
POK_IBB_S	6	Power-OK Negative Buck-Boost Status	0x0: Buck-boost output voltage is above POK threshold 0x1: Buck-boost output voltage is below POK threshold
POK_BST_S	5	Power-OK Positive Boost Status	0x0: Boost output voltage is below POK threshold 0x1: Boost output voltage is above POK threshold
IBB_SCP_S	4	Inverting Buck-Boost Short-Circuit Status	0x0: Inverting buck-boost output is not short-circuited 0x1: Inverting buck-boost output is short-circuited
BST_SCP_S	3	Boost Short-Circuit Status	0x0: Boost output is not short-circuited 0x1: Boost output is short-circuited
IBB_OCP_S	2	Inverting Buck-Boost Overcurrent Protection Status	0x0: Inverting buck-boost output is not overloaded 0x1: Inverting buck-boost output is overloaded
BST_OCP_S	1	Boost Overcurrent Protection Status	0x0: Boost output is not overloaded 0x1: Boost output is overloaded
ERR_PIN_S	0	Error Pin Status	0x0: Sensor error has not been detected 0x1: Sensor error has been detected

ERCFLAG (0x4)

POK and Interrupt Source Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OVLO	UVLO	OTLO	RSVD
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
OVLO	3	Overvoltage Lockout	0x0: The overvoltage lockout has not occurred since this last read of this register 0x1: The overvoltage lockout has occurred since the last

BITFIELD	BITS	DESCRIPTION	DECODE
			read of this register. This indicates that the V_{IN} voltage rose above OVLO (~5.85V).
UVLO	2	Undervoltage Lockout	0x0: The undervoltage lockout has not occurred since this last read of this register 0x1: The undervoltage lockout has occurred since the last read of this register. This indicates that the V_{IN} voltage fell below UVLO (~2.4V).
OTLO	1	Overtemperature Lockout	0x0: The overtemperature lockout has not occurred since the last read of this register 0x1: The overtemperature lockout has occurred since the last read of this register. This indicates that the junction temperature exceeded +165ºC.
RSVD	0	Reserved	

CNFG_GLBL (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_BIAS	FRC_IBB_ON	FRC_BST_ON	FORCE_DIS
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_BIAS	3	Bias Enable	0x0: Determined by EN pin 0x1: Enable
FRC_IBB_ON	2	Inverting Buck-Boost (IBB) Regulator Enable Allows the IBB regulator to be forced on regardless of which state it is in.	0x0: Determined by EN pin, nERR pin, and FORCE_DIS 0x1: Force enable
FRC_BST_ON	1	Boost Regulator Enable Allows the BST regulator to be forced on regardless of which state it is in	0x0: Determined by EN pin, nERR pin, and FORCE_DIS 0x1: Force enable
FORCE_DIS	0	Force Disable Bit While the nERR pin is low, this bit is set to 1 and both the inverting buck boost and boost remain disabled. To allow the regulators to be re-enabled, write this bit to 0 while the nERR pin is high.	0x0: Sensor error has not been detected 0x1: Sensor error has been detected

CNFG_DCDC0 (0x30)

BIT	7	6	5	4	3	2	1	0

Field	–	RNG_IBB	SS_IBB	ADE_IBB	RSVD	IPK_BST[1:0]	ADE_BST
Reset	–	OTP	OTP	OTP	0x0	OTP	OTP
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RNG_IBB	6	Inverting Buck-Boost Output-Voltage Range	0x0: Low range: -24.00V < V_{OUT_IBB} < -17.01V 0x1: High range: -17.00V < V_{OUT_IBB} < -10.01V
SS_IBB	5	Inverting Buck-Boost Soft-Start Current Limit	0x0: 400mA 0x1: 600mA
ADE_IBB	4	Inverting Buck-Boost Active-Discharge Enable	0x0: The active discharge function is disabled. When the inverting buck boost is disabled, its discharge rate is a function of the output capacitance and the external load (default). 0x1: The active discharge function is enabled. When the inverting buck boost is disabled, an internal resistor (R_{AD_NBB}) is activated from V_{NBB} to GNDIBB to help the output voltage discharge. The output-voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_NBB} load.
RSVD	3	Reserved	
IPK_BST	2:1	Inductor Peak Current Limit for the Boost Regulator	0x0: 1.0A 0x1: 0.781A 0x2: 0.563A 0x3: 0.5A (DCM only)
ADE_BST	0	Positive Boost Active-Discharge Enable	0x0: The active discharge function is disabled. When the positive boost is disabled, its discharge rate is a function of the output capacitance and the external load (default). 0x1: The active discharge function is enabled. When the positive boost is disabled, an internal resistor (R_{AD_BOOST}) is activated from V_{BOOST} to PGNDBST to help the output voltage discharge. The output-voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_BOOST} load.

CNFG_DCDC1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RSVD	RSVD	RSVD	VOUT_IBB
Reset	–	–	–	–	0x0	0x0	0x0	OTP
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	3	Reserved	
RSVD	2	Reserved	
RSVD	1	Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_IBB	0	This bit acts as the MSB of the 9-bit configuration for the inverting buck-boost target output voltage and works alongside address CNFG_DCDC2.VOUT_IBB. **Note:** This bit is latched to CNFG_DCDC2.VOUT_IBB. For the user to write using 9 bits, the user must write first to the CNFG_DCDC1.VOUT_IBB bitfield before writing to the CNFG_DCDC2.VOUT_IBB address. All 9 bits for VOUT_IBB are updated at the same time when VOUT_IBB[7:0] is written.	0x0: See CNFG_DCDC2.VOUT_IBB for target voltage settings

CNFG_DCDC2 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	VOUT_IBB[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_IBB	7:0	Inverting Buck-Boost Target Output Voltage This is a 9-bit configuration with 15mV increments. This register address works alongside bit 0 of 0x31 register address (CNFG_DCDC1.VOUT_IBB). **Note:** For the user to write using 9 bits, the user must write first to the CNFG_DCDC1.VOUT_IBB bitfield before writing this register address. All 9 bits for VOUT_IBB are updated at the same time when VOUT_IBB[7:0] is written. Low range: -24.00V to -17.01V High range: -17.00V to -10.01V	0x000: -17.010V/-10.010V 0x001: -17.010V/-10.010V ... 0x02D: -17.010V/-10.010V 0x02E: -17.025V/-10.025V ... 0x06F: -18.000V/-11.000V ... 0x1FE: -23.985V/-16.985V 0x1FF: -24.000V/-17.000V

CNFG_DLY0 (0x40)

BIT	7	6	5	4	3	2	1	0

Field	STRTUP_DLY_IBB[3:0]	PWRDN_DLY_IBB[3:0]
Reset	0xOTP	OTP
Access Type	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
STRTUP_DLY_IBB	7:4	Startup Delay for the Inverting Buck-Boost From Time when EN is Received	0x0: 0.2ms 0x1: 0.4ms 0x2: 0.6ms 0x3: 0.8ms 0x4: 1.0ms 0x5: 1.2ms 0x6: 1.4ms 0x7: 1.6ms 0x8: 1.8ms 0x9: 2.0ms 0xA: 2.2ms 0xB: 2.4ms 0xC: 2.6ms 0xD: 2.8ms 0xE: 3.0ms 0xF: 3.2ms
PWRDN_DLY_IBB	3:0	Power-Down Delay for the Inverting Buck-Boost From Time when EN is Received	0x0: 0.2ms 0x1: 0.4ms 0x2: 0.6ms 0x3: 0.8ms 0x4: 1.0ms 0x5: 1.2ms 0x6: 1.4ms 0x7: 1.6ms 0x8: 1.8ms 0x9: 2.0ms 0xA: 2.2ms 0xB: 2.4ms 0xC: 2.6ms 0xD: 2.8ms 0xE: 3.0ms 0xF: 3.2ms

CNFG_DLY1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	STRTUP_DLY_BST[3:0]				PWRDN_DLY_BST[3:0]			
Reset	0xOTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
STRTUP_DLY_BST	7:4	Start-Up Delay for the Boost From Time when EN is Received	0x0: 0.2ms 0x1: 0.4ms 0x2: 0.6ms 0x3: 0.8ms 0x4: 1.0ms 0x5: 1.2ms 0x6: 1.4ms 0x7: 1.6ms

BITFIELD	BITS	DESCRIPTION	DECODE
			0x8: 1.8ms 0x9: 2.0ms 0xA: 2.2ms 0xB: 2.4ms 0xC: 2.6ms 0xD: 2.8ms 0xE: 3.0ms 0xF: 3.2ms
PWRDN_DLY_BST	3:0	Power-Down Delay for the Boost From Time when EN is Received	0x0: 0.2ms 0x1: 0.4ms 0x2: 0.6ms 0x3: 0.8ms 0x4: 1.0ms 0x5: 1.2ms 0x6: 1.4ms 0x7: 1.6ms 0x8: 1.8ms 0x9: 2.0ms 0xA: 2.2ms 0xB: 2.4ms 0xC: 2.6ms 0xD: 2.8ms 0xE: 3.0ms 0xF: 3.2ms

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	OPTIONS
MAX77720SANP+T	-40°C to +125°C	20 WLP	See *Table 1*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/23	Initial release	—