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### Evaluates: MAX77542 in WLP Package

### MAX77542 Evaluation Kit

### **General Description**

The MAX77542 evaluation kit (EV kit) is a fully assembled and tested printed circuit board (PCB) that demonstrates the MAX77542 four-phase configurable step-down regulator. The board is equipped with test points and jumpers for testing all pins on the device. Six potentiometers allow for adjusting the SEL1/2/3/4 and CFG1/2 configuration pins at will. There are also probe sockets on critical nodes (VOUTx, LXx) for precise measurements. The board also comes with some spare inductors (L5-L12) for testing out efficiency/performance tradeoffs. The PCB is designed with Analog Devices, Inc.'s, recommended layout of the IC and external components. The IC sets default output voltages by way of R15, R17, R19, and R21 but can be changed with the potentiometers or through I<sup>2</sup>C communication. Analog Devices' GUI can be used by connecting a Windows®-based PC to J1 through a USB Type-A to Micro-USB cable.

### **Features**

- Probe Sockets for High-Accuracy Measurements
- Test Points for All Features (MFIO, CE, IRQB)
  - Default Output Voltage Adjustable Via SEL1/2/3/4
  - Default MFIO Function and I<sup>2</sup>C Slave ID Set Via CFG1
  - Default Peak Current Limit and FSW Set Via CFG2
- Connector for Custom I<sup>2</sup>C Host

### **EV Kit Contents**

- The MAX77542 EV kit
- USB Type-A to Micro-USB Cable
- Windows-based GUI software is available for use with the EV kit and can be downloaded from Analog Devices website at <u>www.analog.com/max77542evkit</u> (under the **Design Resources** tab). Windows 7 or newer is required to use with the EV kit GUI software.



Figure 1. MAX77542 Evaluation Board

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#### Ordering Information appears at end of data sheet.

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### **EV Kit Specifications and Default** Configuration

The MAX77542 EV kit comes with the following default settings:

- V<sub>OUT1</sub> = 1.0V
- V<sub>OUT2</sub> = 1.8V
- V<sub>OUT3</sub> = 3.3V
- V<sub>OUT4</sub> = 5.0V
- F<sub>SW</sub> = 1.0MHz
- Skip Mode
- Soft-Start and DVS Ramp-Up Rate = 5.0mV/µs
- Soft-Stop and DVS Ramp-Down Rate = -0.15mV/µs
- 100 $\Omega$  Active Discharge Enabled (1 $\Omega$  is Disabled)
  - Peak Current Limit = 5.5A
  - MFIO1-8 set to EN inputs and POK outputs
  - MFIO1: EN1
  - MFIO2: POK1
  - MFIO3: EN2
  - MFIO4: POK2
  - MFIO5: EN3
  - MFIO6: POK3
  - MFIO7: EN4
  - MFIO8: POK4
  - MAX77542AAWU+ Installed

### Table 1. EV Kit Default Specifications

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage		2.8		16.0	V
Output Voltage	Configurable by SEL or through I <sup>2</sup> C	0.3		5.2	V
Output Current	Per Phase	0		4	A
Switching Frequency			1		MHz
Peak Current Limit			5.5		A

### **Quick Start**

#### **Required Equipment**

- Adjustable DC Power Supply or Applicable Battery
- Multimeter
- USB Type-A to Micro-USB Cable (optional)
- Windows-based PC with MAX77542 EV kit GUI

#### **Setup Overview**

Figure 2 depicts a simplified block diagram of a typical EV kit setup. Attach more meters and scope probes as necessary. Figure 3 depicts a typical application circuit of the MAX77542.





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Figure 3. Typical Application Circuit

#### Procedure

Follow this procedure for first time evaluation:

- Install GUI software. Visit the product webpage at <u>https://www.analog.com/max77542evkit</u> and navigate to Design Resources to download the latest version of the EV kit software. Save the EV kit software installation file to a temporary folder and decompress the ZIP file. Run the .EXE file and follow the on-screen instructions to complete installation.
- 2) Ensure that the jumpers are configured as per Table 2.
- Apply a valid voltage (like 7.6V) from a power supply to the SYS and PGND terminals of the EV Kit. Do not enable the power supply yet.

- 4) **Important:** Make sure that the phase configuration is correct. See the *Phase Configuration* section.
- 5) Connect a USB cable between your PC and J1 USB port on the EV kit.
- 6) Turn on the input power supply.
- 7) Open the GUI and click Device in the menu bar. Click Connect in the Device drop-down list. Wait for the device to respond, and in the Synchronize window, press Connect. The GUI takes a few seconds to read the device registers after pressing Connect.
- Navigate to the Buck 1 Configuration tab. Drag the slide bar in Buck Normal Output Voltage section to change the output voltage and click Write.

	Write Read Once					Start Auto Read E	very 600	) _ ms
niguration 2	Interrupt			Interrupt Mask				
ation	Buck Master1 Short Circuit Fault Interrupt	0 = Not Occurred	Read	Buck Master1 Short-Circuit Fault Interrupt Mask	🚺 1 = Masked			Read
ion	Buck Master1 Power-OK Fault Interrupt	0 = Not Occurred		Buck Master1 Power-OK Fault Interrupt Mask	1 = Masked			Write
ration	Status							
n	Buck Master1 Short-Circuit Fault Status	0 = Buck Master1 Output Voltage is High	er than its Short-Circuit Thresh	old, or Buck Master1 is Disabled				Read
on	Buck Master1 Power-OK Fault Status	0 = Buck Master1 Output Voltage is Low	er than its POK Threshold, or Bi	ick Master1 is Disabled				
	Buck Normal Output Voltage							
	Buck Master1 Output Voltage	0x64 = 0.800V		<u></u>				Read
								Write

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- Navigate to the Global Configuration 2 tab. Toggle Buck Master1 Enable Control to Enable and press Write.
- 10) Measure OUT1 with a voltmeter. It should read the voltage set in the GUI in Step 8.
- 11) Use the GUI to exercise the various features of the MAX77542.

This concludes the Quick Start procedure. Users are now encouraged to further explore the device and its register settings with the GUI software. For more information on the GUI, see *Detailed Description of Software* section.

JUMPER	NODE OR FUNCTION	SHUNT POSITION	FUNCTION
J1	USB Connector (GUI)	N/A	GUI USB Connector
J2	ALT_IN	1-2*	Connects ALT_IN to GND. Leave disconnected if ALT_IN functionality is used.
12	CE	1-2*	Connects CE to SYS (Enables internal bias)
13	CE	2-3	Connects CE to GND (Disables internal bias)
14		1-2*	Connects SEL1 to fixed 1.87k $\Omega$ resistor (1.0V <sub>OUT</sub> default)
J4	SELI	2-3	Connects SEL1 to the potentiometer for adjustable default $\mathrm{V}_{_{\mathrm{OUT}}}$
		2-4*	Connects SEL2 to fixed $30.9k\Omega$ resistor (1.8V <sub>OUT</sub> default)
J5	SEL2	3-4	Connects SEL2 to GND (enables multiphase operation)
		4-6	Connects SEL2 to the potentiometer for adjustable default $\mathrm{V}_{_{\mathrm{OUT}}}$
		2-4*	Connects SEL3 to fixed $64.9k\Omega$ resistor ( $3.3V_{OUT}$ default)
J6	SEL3	3-4	Connects SEL3 to GND (enables multiphase operation)
		4-6	Connects SEL3 to the potentiometer for adjustable default $V_{\mbox{OUT}}$
		2-4*	Connects SEL4 to fixed 100k $\Omega$ resistor (5V <sub>OUT</sub> default)
J7	SEL4	3-4	Connects SEL4 to GND (enables multiphase operation)
		4-6	Connects SEL4 to the potentiometer for adjustable default $V_{OUT}$
J8	CFG1	1-2*	Connects CFG1 to fixed $0\Omega$ resistor (Sets MFIO default functions. Refer to the device data sheet for more information.)
		2-3	Connects CFG1 to the potentiometer for adjustable MFIO functions
J9	CFG2	1-2*	Connects CFG2 to fixed 0Ω resistor (Sets default Mx_ILIM and Mx_FREQ values. Refer to the device data sheet for more information.)
		2-3	Connects CFG2 to the potentiometer for adjustable Mx_ILIM and Mx_FREQ
		1-2	MFIO1 pulled up to VIO through $10k\Omega$ resistor
J10	MFIO1	2-3*	MFIO1 tied to GND
		N/A	MFIO1 left disconnected (Hi-Z)
		1-2*	MFIO2 pulled up to VIO through $10k\Omega$ resistor
J11	MFIO2	2-3	MFIO2 tied to GND
		N/A	MFIO2 left disconnected (Hi-Z)
		1-2	MFIO3 pulled up to VIO through $10k\Omega$ resistor
J12	MFIO3	2-3*	MFIO3 tied to GND
		N/A	MFIO3 left disconnected (Hi-Z)

### **Table 2. Default Shunt Positions and Jumper Descriptions**

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JUMPER	NODE OR FUNCTION	SHUNT POSITION	FUNCTION
		1-2*	MFIO4 pulled up to VIO through $10k\Omega$ resistor
J13	MFIO4	2-3	MFIO4 tied to GND
		N/A	MFIO4 left disconnected (Hi-Z)
		1-2	MFIO5 pulled up to VIO through $10k\Omega$ resistor
J14	MFIO5	2-3*	MFIO5 tied to GND
		N/A	MFIO5 left disconnected (Hi-Z)
		1-2*	MFIO6 pulled up to VIO through $10k\Omega$ resistor
J15	MFIO6	2-3	MFIO6 tied to GND
		N/A	MFIO6 left disconnected (Hi-Z)
		1-2	MFIO7 pulled up to VIO through $10k\Omega$ resistor
J16	MFIO7	2-3*	MFIO7 tied to GND
		N/A	MFIO7 left disconnected (Hi-Z)
		1-2*	MFIO8 pulled up to VIO through $10k\Omega$ resistor
J17	MFIO8	2-3	MFIO8 tied to GND
		N/A	MFIO8 left disconnected (Hi-Z)
J18	I <sup>2</sup> C Header for External I <sup>2</sup> C Bus	N/A	Test points for I <sup>2</sup> C signals to be connected to an external I <sup>2</sup> C Bus
14.0		1-2*	VIO LDO powered from VUSB
J.18		2-3	VIO LDO powered from VIO_PI (External I <sup>2</sup> C Bus)
120		1-2	VIO is set to 1.2V
JZU	VIO Level	2-3*	VIO is set to 1.8V

### Table 2. Default Shunt Positions and Jumper Descriptions (continued)

\*Default position.

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### **EV Kit Hardware**

#### **GUI Interface**

The MAX77542EVKIT# can be connected to the GUI by connecting a USB cable to J1 on the EV kit.

#### External I<sup>2</sup>C Bus

To use a different I<sup>2</sup>C host, disconnect the USB cable and attach I<sup>2</sup>C wires to J18 on the EV kit. Move the jumper on J19 to position 2-3. The J19 jumper sets the input of the LDO that provides VIO to either the USB input voltage or the voltage applied to VIO on J18. Jumper J18 is the input to a level shifter rather than an input to the actual pins on the IC.

#### **Phase Configuration**

The SEL2, SEL3, and SEL4 are used to set the phase configuration of the MAX77542. R48, R49, R50, and R57 are used to connect the outputs together for multiphase configuration. The default configuration is four outputs ( $1\phi + 1\phi + 1\phi + 1\phi$ ). See <u>Table 3</u> to configure the MAX77542 according to the correct phase configuration.

#### **Buck Feedback Configuration**

Buck feedback configuration is specific to the selected phase configuration. Each of the four bucks have their own feedback inputs (SNSxP and SNSxN for Buck 1 and Buck 3; SNSxP alone for Buck 2 and Buck 4). Only the master feedback pins need to connect to the output voltage to ensure regulation (see <u>Table 4</u>). Unused or slave feedback pins can connect to the output voltage during evaluation at no consequence.

For example, a  $2\phi + 2\phi$  configuration creates Buck 1 (using L1 and L2) and Buck 3 (using L3 and L4). Buck 1's feedback is SNS1P and SNS1N. Buck 3's feedback is SNS3P and SNS3N. In this example, Buck 2 and Buck 4 are not configured as stand-alone channels. Therefore, SNS2P and SNS4P are do not care but can connect to their corresponding multiphase outputs with no consequence.

Each inductor under a single buck's control must be the same value. Refer to the device data sheet for recommendations on which inductor to use for each output voltage range.

#### Table 3. Phase Configuration Truth Table for Local Sensing

PHASE CONFIGURATION	SEL2	SEL3	SEL4	R48	R49	R50	R57
4 Outputs (1ϕ + 1ϕ + 1ϕ + 1ϕ)	>200Ω	>200Ω	>200Ω	Open	Open	Open	Open
3 Outputs (2φ + 1φ + 1φ)	0Ω	>200Ω	>200Ω	0Ω	Open	Open	Open
2 Outputs (2φ + 2φ)	0Ω	>200Ω	0Ω	0Ω	Open	0Ω	Open
2 Outputs (3ϕ + 1ϕ)	0Ω	0Ω	>200Ω	0Ω	Open	Open	0Ω
1 Output (4¢)	0Ω	0Ω	0Ω	0Ω	0Ω	0Ω	0Ω

#### Table 4. Buck Output Naming Convention and Feedback

PHASE CONFIGURATION	NAMING CONVENTION AND PHASES USED	FEEDBACK INPUTS
	Buck 1 (1¢) uses L1	SNS1P, SNS1N
	Buck 2 (1¢) uses L2	SNS2P
4 Outputs $(1\phi + 1\phi + 1\phi + 1\phi)$	Buck 3 (1¢) uses L3	SNS3P, SNS3N
	Buck 4 (1¢) uses L4	SNS4P
	Buck 1 (2φ) uses L1, L2	SNS1P, SNS1N
3 Outputs (2φ + 1φ + 1φ)	Buck 3 (1¢) uses L3	SNS3P, SNS3N
	Buck 4 (1¢) uses L4	SNS4P
	Buck 1 (2¢) uses L1, L2	SNS1P, SNS1N
$2 \text{ Outputs}(2\phi + 2\phi)$	Buck 3 (2¢) uses L3, L4	SNS3P, SNS3N
	Buck 1 (3ø) uses L1, L2, L3	SNS1P, SNS1N
$2 \text{ Outputs} (3\phi + 1\phi)$	Buck 3 (1¢) uses L3	SNS4P
1 Output (4¢)	Buck 1 (4) uses ALL (L1, L2, L3, L4)	SNS1P, SNS1N

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#### **Buck Feedback Sense Location**

The EV kit uses additional  $0\Omega$  resistors to modify the feedback routing between the IC and the output voltage sense location. In general, single-phase configurations should take feedback close to the corresponding output capacitor as close to the IC as possible (this is the default EV kit configuration). However, the MAX77542 supports remote sensing in addition to local sensing. The EV kit includes a LOAD plane for testing remote sensing on the EV kit. Table 5 describes which resistors to install depending on whether local or remote sensing is being evaluated.

Buck 1, Buck 2, Buck 3, and Buck 4 can be connected to the remote LOAD plane by installing R45, R44, R46, and R47, respectively. These resistors are for the high current connections.

#### Change Default Setup with RSEL1/RSEL2/ RSEL3/RSEL4/CFG1/CFG2

Note that the MAX77542 EV kit is default configured for four output, single-phase operation, with VOUT1 set to 1.0V, VOUT2 set to 1.8V, VOUT3 set to 3.3V, and VOUT4 set to 5.0V (by way of R15, R17, R19, and R21). The CFG1 sets MFIO1-8 to EN\_M1, POK\_M1, EN\_M2, POK\_M2, EN\_M3, POK\_M3, EN\_M4, and POK\_M4 through R23. CFG2 sets Mx\_ILIM to 5.5A and Mx\_FREQ to 1.0MHz through R25. To evaluate other default configurations (for different voltages/ranges upon first powerup), change the resistance at SEL1/2/3/4 and CFG1/2 with the potentiometers or R15, R17, R19, R21, R23, and R25. Refer to the device data sheet for more information.

# Alternative Low-Voltage Input (ALT\_IN) Functionality

The ALT\_IN pin can be accessed through Jumper J2. When ALT\_IN functionality is unused, either install a jumper on J2 to tie ALT\_IN to GND or leave J2 open to leave ALT\_IN disconnected. To power ALT\_IN using one of the buck outputs or another alternative power source, use a wire to tie pin 1 of J2 or the ALT\_IN test point to the desired power source. Refer to the device data sheet for more information on the operation of the ALT\_IN pin.

# Test Points and Critical Node Measurement (VOUT and LX)

The EV kit comes with test points where sockets can be soldered onto the board for measuring the critical nodes VOUT1-4 and LX1-4. Use these probe sockets to eliminate as much noise as possible when measuring the critical nodes. To ensure best results, use a very short ground wire from the ground sleeve of the scope probe to the GND side of the probe test point, and use the bare tip of the probe directly to the signal side of the probe socket. Following these guidelines give the most accurate results when measuring parameters like output voltage ripple, switching waveforms, and load transient response.

#### Table 5. Multiphase Buck Feedback Recommended Routing

BUCK	LOCALS	SENSING	REMOTE	SENSING
BUCK	SNSxP	SNSxN	SNSxP	SNSxN
Buck 1 (1¢, 2¢, 3¢, 4¢)	R5	R6	R38	R42
Buck 2 (1ø)	R8	N/A	R39	N/A
Buck 3 (1¢, 2¢)	R10	R11	R40	R43
Buck 4 (1¢)	R13	N/A	R41	N/A

#### Table 6. Test Point Selection for Measurement

LOAD TRANSIENT,	EEFICIENCY, LOAD REGULATION, V	REGULATION, LINE OUT ACCURACY	SWITCHING NODE
	OUTPUT VOLTAGE	INPUT VOLTAGE	LX1-4
OUT-1-4 SOCKET	OUTxS, PGNDxS	INxS, PGNDxS	LX1-4 SOCKET

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Figure 4. Example of Probing Sensitive Node

#### **Detailed Description of Software**

The GUI software allows for quick, easy, and thorough evaluation of the MAX77542. The GUI drives I<sup>2</sup>C communication with the EV kit. Every control in the GUI corresponds directly to a register within the MAX77542. Refer to the *Register Map* section of the MAX77542 IC data sheet for a complete description of the registers. See Figure 5 for a screenshot of the GUI upon first opening.

#### Installation

Visit the product webpage at <u>https://www.analog.com/</u> <u>max77542evkit</u> and navigate to Design Resources to download the latest version of the EV kit software. Save the EV kit software installation file to a temporary folder and decompress the ZIP file. Run the .EXE installer and follow the on-screen instructions to complete the installation.

#### **Windows Driver**

After plugging in the MAX77542EVKIT# to the PC with a Micro-USB cable for the first time, wait about 30 seconds for Windows to automatically install the necessary drivers.

#### **Connecting GUI**

After opening the GUI, click **Device** in the upper left corner of the GUI window. Click **Connect** in the drop-down menu.

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onfiguration 1	Write Read Once				Start Auto Read Every	600 ±
onfiguration 2	Interrupts			Interrupts Mask		
onfiguration	ADC Interrupt Source	0 = Not Occurred	Read	ADC Interrupt Source Mask	1 = Masked	Read
onfiguration	MFIO Interrupt Source	0 = Not Occurred	-	MFIO Interrupt Source Mask	1 = Masked	Write
onfiguration	Buck Interrupt Source	0 = Not Occurred	-	Buck Interrupt Source Mask	1 = Masked	
onfiguration	Top-Level Interrupt Source	0 = Not Occurred		Top-Level Interrupt Source Mask	1 = Masked	
figuration	TOPSYS Interrupts			TOPSYS Mask		
Мар	Alternate Input Switch-Over Interrupt	0 = Not Occurred	Read	Alternate Input Switch-Over Interrupt Mask	0 = Unmasked	Read
	V_IO Fault Interrupt	0 = Not Occurred	=	VIO Fault Interrupt Mask	0 = Unmasked	Write
	SYS Under-Voltage Lock-Out Interrupt	0 = Not Occurred	=	SYS Under-Voltage Lock-Out Interrupt Mask	1 = Masked	
	Thermal Shutdown Interrupt	0 = Not Occurred	=	Thermal Shutdown Interrupt Mask	1 = Masked	
	Thermal Warning Interrupt	0 = Not Occurred	7	Thermal Warning Interrupt Mask	1 = Masked	
	Status					
	Alternate Input Switch-Over Status	0 = VDD, LDOs are Powered from SYS				Read
	VIO Fault Status	0 = VIO is Greater than VIO_UVLO_R				
	SYS Under-Voltage Lock-Out Status	0 = VSYS is Greater than VUVLO_R				
	Thermal Shutdown Status	0 = Junction Temperature (Tj) is Lower than 150d	egC			
	Thermal Warning Status	0 = Junction Temperature (Tj) is Lower than TWAH	RN_1H[2:0]			
	Device Configuration			TOPSYS Configuration		
	Phase Configuration	0x00 = 1PH + 1PH + 1PH + 1PH (4 Outputs)	* Read	Alternative Input Control	0 = Powered from SYS	Read
	CFG1 Latched Code	0x00 = VOUT(0.50V), FSW(1.0MHz), RNG(Low)	* Write	CE Pulldown Control MAX77542	0 = Disable 800kΩ Internal Pulldown	Write
	CFG2 Latched Code	0x00 = 2-Phase Operation	w	Interrupt Mask Mode Sett Bit[ALT_IN_EN (5)]	0x0C)] 0 = Gated after the Interrupt bit when Masked	
	SEL1 Latched Code	0x00 = 2-Phase Operation	w.	Forced Junction Temper	o = Only when Output(s) is/are Enabled	
	SEL2 Latched Code	0x00 = 2-Phase Operation	w	System Clock Pre-nable Control	0 = Disable	
	SEL3 Latched Code	0x00 = 2-Phase Operation	w	VL12 and VL34 LDOs Pre-nable Control	0 = Disable	
	SEL4 Latched Code	0x00 = 2-Phase Operation	¥			

Figure 5. MAX77542 Evaluation Kit GUI Top-Level Interface (Before Connecting)

The **Device Synchronization** menu opens (Figure 6) once the MAX77542 IC responds (voltages on SYS pin,  $V_{IO}$  pin, and CE pin must be valid on the MAX77542 IC for it to respond). The I<sup>2</sup>C address shown is the MAX77542 IC's 7-bit slave address. The address shown changes depending on the EV kit's CFG1 configuration. Click **Connect and Read**. The text at the bottom right of the GUI window changes from MAXUSB\_INTERFACE# is Disconnected to MAXUSB\_INTERFACE# is Connected.

#### **Global Configuration Tabs**

The GUI has two tabs for global configuration of the bucks (**Global Configuration 1** and **Global Configuration 2**). Global Configuration 1 displays high-level information about the IC such as the interrupts, interrupt masks, status bits, and device configuration. <u>Figure 7</u> shows a snapshot of the **Global Configuration 1** tab.

Global Configuration 2 is used to enable and disable the buck outputs, enable and disable low power mode, and change the flexible power sequencer settings. Figure 8 shows a snapshot of the **Global Configuration 2** tab.

			D
Port	Interface	Infomation	Device Name
A	12C	7-bit Address (0x60)	MAX77542
	Port	Port Interface A I2C	Port Interface Information A I2C 7-bit Address (0x60)

Figure 6. Port Synchronization Menu

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-	Write Read Once					Start Auto Read Every	500 .
I Configuration 2	EN Configuration			GLB Configuration 1-5			
1 Configuration	Buck Master4 LPM Control	0 = Disable	Read	Buck Master1 Startup Delay Control	0x00 = 0.0ms	(V)	Read
Configuration	Buck Master3 LPM Control	O = Disable	Write	Buck Master1 Shutdown Delay Control	0x00 = 0.0ms	•	Write
Configuration	Buck Master2 LPM Control	0 = Disable		Buck Master2 Startup Delay Control	0x00 = 0.0ms	*	
onfiguration	Buck Master1 LPM Control	0 = Disable		Buck Master2 Shutdown Delay Control	0x00 = 0.0ms	(v)	
onfiguration	Buck Master4 Enable Control	0 = Disable		Buck Master3 Startup Delay Control	0x00 = 0.0ms	¥	
r Map	Buck Master3 Enable Control	0 = Disable		Buck Master3 Shutdown Delay Control	0x00 = 0.0ms	*	
	Buck Master2 Enable Control	0 = Disable		Buck Master4 Startup Delay Control	0x00 = 0.0ms	¥	
	Buck Master1 Enable Control	0 = Disable		Buck Master4 Shutdown Delay Control	0x00 = 0.0ms	*	
				FPSO Startup Delay Control	0x00 = 0.0ms	×	
				FPSO Shutdown Delay Control	0x00 = 0.0ms	*	
	GLB Configuration 6-7			I2C Configuration			
	Delay Step Size	0x00 = 0.5ms	* Read	I2C Watchdog Timer	0x00 = 31ms	×	Read
	Flexible Power Sequencer	0 = 0-to-1 Transition	Write				Write

Figure 7. Global Configuration 1 Window

	*						
obal Configuration 1	Inte Read-Once					(Statium field) Every	600 C m
bac Configuration 2	En Configuration			GLB Configuration 1-5			
a 1 Contiguration	Buck Master4 UPM Control	(20 0 + Deater	Rent	Buck Marter1 Startup Delay Control	0401+0.0%	/*	Final
3 Configuration	Buck Masher3 UPM Control	(21) 0 - Disatin	10.04	Buck Masker1 Shutdown Delay Control	0x00+110ms	*	virite
4 Conferration	Buck Mashed LPM Control	CID 0 = Deable		Buck Martini2 Startup Delay Control	0.02 = 0.0%	1	
Configuration	Buck Master1 LPM Control	(III) 0 - Deathe		Buck Master2 Shuttown Delay Control	0x00 + 0.0ms	(¥)	
Configuration	Buck Marteni Enable Control	(20) 0 = Dealere		Duch Manhoo Starfug Delay Control	0.01+1.010		
ster Map	Buck Master3 Enable Control	()) 0 - Disatile		Own Macher's Dhubbown Datay Control	dell-like		
	Buch Maxim/2 Enable Control	(20) 0 = Deable		Buck Macher4 Startup Delay Control	0409+1049		
	Buck Master1 Enable Control	CID 0 - Deaths		Buck Master# Stutdown Delay Control	0x00+010+x	14	
				FPSO Startup Delay Control	0409 = 0.0ms		
				FPSO Shuldown Datay Coresi	0x00 = 0.0ma		
	GLB-Configuration 6-7			OC Configuration			
	Dates they free	failt - Litra	Real	OC Watching Timer	(a)() = 31mm		Feat
	Flexible Power Sequencer	C20 0 x 0 4x 1 Transition	104				1010

Figure 8. Global Configuration 1 Window

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#### **Configuring the Regulator**

The GUI has a configuration tab for each buck (Buck 1-4 Configuration). Use these to adjust the various parameters of each buck. Note that Buck 2, Buck 3, and Buck 4 Configuration is disabled when those phases are configured as slave phases in multiphase configuration.

Figure 9 shows a snapshot of the Buck 1 Configuration tab. To use the GUI, select the desired option in one of the interactable fields (button, slider, drop-down list) and press **Write** next to it. Use the *Read* command to refresh the current state of the registers.

tene Fault-Once	Disk (hadbas) Day								
Non 2 Internant			Interrupt Maria						
Buck Master1 Short Casul Fault Internat	0 + Net Downed	Read	Buck Marter1 Diot-Carout Fault Internat Mark	C 1 - Washed					
Buck Masher's Power-OK Fault Interrupt	3 + Net Octored		Buch Mashert Power-OK Fault Interrupt Wash	1 - Washed		- 10			
for Status	Tata								
Buck Naster1 Shot-Circuit Fault Status	Al Market Shot Gradi Fast Takes (1 + Buck Washet Suppl' Intege in Higher than Its Broth Gradi Towahet), or Buck Market is Dealined								
Buck Master1 Power-OK/Fault Status	(1) Buck Waster's Dulput rollage is Lower than its PCK. Threshold, or Buck M	aster1 is Dealted							
Buck Normal Output Liptage									
Buck Master1 Culput Initiage	0x54 = 0.800v								
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Figure 9. Buck 1 Configuration Window

## Evaluates: MAX77542 in WLP Package

### Configuring the Multifunction I/Os

The GUI has a configuration tab for the MFIOs. The tab includes the interrupt bits, interrupt mask bits, and status

bits. It also includes the configuration registers for each MFIO pin to set its functionality. <u>Figure 10</u> shows a snapshot of the **MFIO Configuration** tab.

indiguration 1	Virte Read Once						Station feet Every	600 .
integration 2	internat				Interrupt March			
subgeration	Multi-function I/O @ Interrupt	8 + Net Occurred		Read	Multi-function VD 8 Interrupt Marin	1 = Masked		Fee
requirece	Multi-function I/O T Interrupt	8-+ Net Occurred			Math function (ID 7 Interrupt Vess)	1 = Mashad		100
and an other states	Multi-function I/O 6 Interrupt	8 + Net Occurred		Bull-Ande	Multi-function VD 5 Interrupt Vacio	C 4 = Maximi		
Configuration Configuration ster Map	Multi-function I/O 6 Interrupt	8 + tail Courred			Multi-function VD 5 Interrupt Wask	1 + Mashad		
	Multi-function I/O 4 Interrupt	Auth-fanction 10 4 Interrupt D + Not Occurred		Multi-function VD 4 Interrupt Wash				
	Multi-function I/O 3 Interrupt	8 + Net Goourned			Multi-function VO 3 Interrupt Wask	1 + Masked		
	Multi-function I/O 2 Interrupt	8 - Net Occurred			Multi-function VD 2 Interrupt Mask	1 + Masted		
	Multi-function I/O 1 Interrupt	8 + Aut Occurred			Multi-function VD 1 Interrupt Wask	1 - Masted		
	Dates							
	Multi-function I/O & Status	I + Input is NotAsserted			Read			
	Multi-function I/O 7 Disture	D 1 Hput is fait-Accented						
	Multi-function I/Q 4 Status	(i = trpul is hist-keserbed						
	Multi-function I/O 5 Status	2-1 Pput Is Not-Accented	0.1 Ppul II NRAsselled 0 - Inpul II NRAsselled					
	Multi-function I/O 4 Status	3 = input is hist-tasserfield						
	Multi-function I/O 3 Status	0 1 mput is hist-Asserted	2 : epst a hitrAccented					
	Multi-function I/O 2 Status	2 + Input is hold-basefield						
	Multi-function I/O 1 Status	1 + Hput is Not Asserted						
	MIC 1 Configuration MF							
	MPO 1 Centrguration				MPIO 2 Configuration			
	MHO 1 Configuration MHO1 Selection	(bd2 + H1 (Made1)	(*)	Read	MPIC 2 Configuration MPIC2 Selection	(xcb = M1 (Master1)	(v)	fee
	MPO1 Configuration MPO1 Selection MPO1 Function	Sull - H1 (Maser) Sull - Organ Scale (30)	(*) /*)	Read	MPIO 2 Configuration MPIO2 Selection MPIO2 Function	(5x50 = M1) (Master 1) (5x50 = Dusput Enable (DN)	1	Rea the
	MHO1 Configuration MHO1 Selection MHO1 Function MHO1 Output Driver Wode	Dolb = W1 (Master 1) Dolb = Oxpar (Instite (IP) (31) # 1 Open-Drain	(* )*	Read	MPIO 2 Configuration MPIO2 Detection MPIO2 Punction MPIO2 Output Driver Mode	(add + M) (Master') (add - Dayar Enails (Dk) (27): 8 + Open Strain		Rea Test
	MPO 1 Configuration MPO1 Selection MPO1 Function MPO1 Output Driver Mode MPO1 Pathopen and Pathop	Doll + H1 (Mexim 1) Boll + Organ Enails (Dh) (2011 d + Open-Drain Boll + Stable Pub deven to ADhD	(* /* /*	Read 208a	MPIC 2 Configuration MPIC2 Detection MPIC2 Detection MPIC2 Using Dever Node MPIC2 Using Dever Node MPIC2 Using down and Pull-tap	Bold = Mil (Master 1) Bold = Dupon Entelle (DN) (20) III = E Open Entell Bold = E Elblo F All-Islam ys JOHD		- Peo Teo
	MRD 1 Configuration MRD 1 Selection MRD 1 Fundion MRD 1 Output Driver Mode MRD 1 Output Driver Mode MRD 1 Debounce Timer	(b.0) = 41 (Marier1) (b.0) = Oyae Date (IN) ()) = 8 = Oyae Date ()) = 8 = Oyae Date () = 8 = Oyae Date () = 100 () = 100 () () = 100 () = 100 ()	(*) (*) (*)	Read Utile	MPO 2 Configuration MPO2 Selection MPO2 Foundain MPO2 Pull-date MPO2 Pull-dates and Pull-up MPO2 Pull-dates and Pull-up MPO2 Detoxynor Timer	bd0 = H1 (Hear) (eff = Dawt Faile (Nk )) = 1 (per Faile (eff = Min Failer in Kith) (eff = Min Failer in Kith) (eff = Ni Schurze	•	- Peop
	MIC 1 Configuration MIC 1 Selection MIC 1 Fundaun MIC 1 Could Draw Hode MIC 1 Fundaun and Full-sig MIC 1 Deteunce Timer MIC 2 Configuration	Buth = H1 (Marine T) (buth = H1 (Marine T) (buth = H1 (Marine T) (B) (buth = H1 (B) (B) (B) (B) (buth = H1 (B) (B) (B) (b) (B) = H1 (B)	(*) (*) (*)	Read 2010	MPIO 2 Configuration MPIO2 Selection MPIO2 Function MPIO2 Output Driver Mode MPIO2 Put Assess and Put up MPIO2 Historics Timer MPIO 4 Configuration	500 + M (Mean) (MII - Dana Ende (MI ))) - F Done Ende (MII - MIA France vs. ADD (SOI + NI Setauron	- - - -	And And
	MIC: 1 Curdgusten MIC: 1 Curdgusten MIC:1 Funden MIC:1 Funden MIC:1 Funden and Funde MIC:1 Funden and Funde MIC:2 Configuration MIC:2 Configuration	(b.00 = H1 (Marier 1) (b.00 = Orani Ensite (IPA) (c) = 4 - Open-Oran (b.00 = H0 (of all Associa ADAD (b.00 = H1 (Marier 1) (b.00 = H1 (Marier 1)	(*) (*) (*) (*)	Read 2018	APIC 2 Certifyeration MIRC2 Selection MIRC2 Fundain MIRC2 August Own Mode MIRC2 August Own Mode MIRC2 Delownor Timer AMIC4 Configuration MIRC4 Selection	(540 – M) (Maser) (641 – Dagos Frañs (191) (77) – Dagos Frañs (191) (78) – Milo Charlon II, Aldon II, Aldon (541 – Mil Scharzen (542 – M) (Maser)		Nex Sec
	MICE 1 Configuration MICE 1 Configuration MICE 1 Configuration MICE 1 Automatics MICE 1 Automatics MICE 2 Configuration MICE 3 Reindon MICE 3 Reindon	0.001 - H1 (Maxim1) 0.001 - Over-Enain 0.001 - State Enain 0.001 - H1 (Maxim1) 0.001 - H1 (Maxim1) 0.001 - H1 (Maxim1) 0.001 - H1 (Maxim1)		Read 2016 Final 2016	NPO 2 Configuration MPICO Selection MPICO AutoBat MPICO AutoBat MPICO AutoBat MPICO AutoBat MPICO Delowing Them MPICO Policy Them MPICO AutoBat MPICO AutoBat MPICO AutoBat MPICO AutoBat	ddl + MI (Mater)  del = Oung Entrie (MI C)   = 1 (Gen Form  del = SING Pul-same to ADHD  del = NI (Mater)   del = NI (Mater)  del = Camp Entrie (MI		Res
	MID 1 Computers MID 1 Computers MID 1 Poulais MID 1 Poulais MID 1 Poulais MID 1 Policies Time MID 2 Policies Time MID 2 Policies Time MID 2 Poulais	8x00+141(Maxim1) 0x00+0xxx6Tanite (00) (20) 8+0pen-Oran 0x00+0X02(Pin4 dawn to ADMO (0x0+Nto Defeature) (0x0+Nto Defeature) (0x0+Nto Defeature) (0x0+Nto Defeature) (0x0+0x0+0x0+0x0+0x0+0x0+0x0+0x0+0x0+0x0	**	Read 2016 Read 2016	NPC 2 Configuration MPC2 Selection anD22 Autosta MPC2 Device Show Mode MPC2 Public Show Mode MPC2 Public Show Mode MPC2 Public Show Mode MPC4 Selection MPC4 Bendton MPC4 Bendton MPC4 Power Show MPC4 Power S	Johl - Hil (Meaner)       Johl - Dopal Ender (IN)       Image: The Open Comm       Johl - No Open Comm       Johl - Nic (Near-1)       Johl - Nic (Near-1)       Johl - Comp Ender (IN)       Image: The Open Comm		Res
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Figure 10. MFIO Configuration Window

### Evaluates: MAX77542 in WLP Package

#### **Configuring the ADC**

The GUI has a configuration tab for the ADC. The **ADC** tab includes the interrupt bits, interrupt masks, and status

bit for each ADC channel. It also includes the readback control bits, averaging control bits, measurement settings, and readback values. Figure 11 shows a snapshot of the **ADC Configuration** tab.

<b>Global Configuration</b> 1	Inte Feed Once					Statium Read Every 500 2 ms		
<b>Global Configuration 2</b>	internant.			Interrupt Marit				
Suck 1 Configuration	40C Channel H Internati	D + Net Updated	Read	ADC Channel 11 Interrupt Nack	I + Washed	Read		
Nuclear Contemporation	4DC Channel 10 Interrupt	a + Not Up baled		ADC Charvel 10 Internet Wash	C 1 - Washed	startine		
hais & Conferenties	400 Channel 9 Interrupt	( if a here capitalities		ADC Channel 8 Interrupt Mack	C 1 = Washed			
MPO Configuration ADC Configuration Register Map	ADC Channel 8 Memaph	0 + Not Updated		ADC Channel & Interrupt Mask				
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	ADC Channel 6 Internet	D-+ Kell Lip-Balled		ADC Channel 6 Interrupt Mask	C 1 - Washed			
	ADC Channel 5 Internant	a - Net Up below		ADC Channel 5 Interrupt Marit	C 1 - Washed			
	400 Channel 4 Interrupt	(1 + Net Updated		ADC Channel 4 Interrupt Mark C 1 + Mached ADC Channel 3 Interrupt Mark C 1 Hapked				
	ADC Channel 3 Internant	( I - I NOT LAPONING						
	ADC Channel 2 Internal	0 + Not Updated		ADC Channel 2 Interrupt Mack	T = Washed			
	40C Channel 1 Internati	D-1 Net Updated		ADC Channel 1 Interrupt Mask	C 1 Washed			
	Teas -							
	4DC Channel & Current Monitor Statue	D-r Not value		Read				
	4DC Channel 3 Current Monitor Status	0 + Not raid						
	4DC Channel 2 Current Monitor Status	(the strength strengt						
	KDC Channel 1 Current Monitor Status	(0-+ Not valid						
				ADC Dalls 3-rt				
	ADC DATA 1-8			ADC DATA 3-11				
	ADC DATA 14 ADC OH1 JOUTS Data Readback	[3e30 + 4 436A	Read	ADC DATA 3.11 ADC OHT (XOUTS) Data Readback	[560 = 5.303v	Paul		
	ADC DHTA 14 ADC DHT (DUTT) Data Readback ADC DHT (DUTT) Data Readback	[3604 = 4.6804 [3604 = 4.6804	Real	ADC DATA 7-11 ADC CHP (HOUTS) Cata Readback ADC CHB (HOUTS) Cata Readback	[0x00 = 0.3009 [0x00 = 0.5009	Pead		
	ADC DATA 14 ADC OH1 (OUT1) Data Readback ADC OH2 (OUT2) Data Readback ADC OH3 (OUT2) Data Readback	[100] = 4.400A [100] = 4.400A [100] = 4.400A	Paul	ADC D476-7-41 ADC D47 (40/73) Data Readback ADC D48 (40/74) Data Readback ADC D48 (40/75) Data Readback	[000 = 0.300v [000 = 0.500v [000 = 0.300v	Feed		
	ADC DATA 14 ADC CH1 30/71/Data Readback ADC CH2 30/72/Data Readback ADC CH2 (0/72) Data Readback ADC CH2 (0/72) Data Readback	[10]0 = 4.40[A (00] = 4.00[A [00] = 4.00[A [00] = 4.00[A	Fast	ADC DATA 3.41 ADC OHT A GUTT) Data Readback ADC OHE (KOUTE) Data Readback ADC OHE (KTH) Data Readback ADC OHE (KTH) Data Readback ADC OHTO (Junctus Teng.) Data Readback	1000 = 3.000v 1000 = 3.000v 1000 = 3.000v 1000 = 571.000egC	Paid		
	ADC DATA 14 ADC DH1 (DUT); Della Readback ADC DH2 (DUT2; Della Readback ADC DH2 (DUT2); Della Readback ADC DH1 (DUT2); Della Readback ADC DH1 (DUT1); Della Readback	[hole = 4.400A [hole = 4.400A [hole = 4.400A [hole = 1.000] [hole = 1.000]	Real	ADC Dalla 3-51 ADC OHT (HOUTS) Data Readback ADC OHE (HOUTS) Data Readback ADC OHE (1011) Data Readback ADC OHE (2014) Data Readback ADC OHE (2014) Data Readback	5000 = 6.3000 5000 = 6.0000 5000 = 6.0000 5000 = 6.3000 5000 = 6.3000	Pad		
	ADC DATA 14 ADC DATA 100,1710 Data Readback ADC DATA 300,1731 Data Readback	[860] = 4 4004 [960] = 4 4004 [960] = 4 4004 [960] = 4 8064 [960] = 3 0064 [960] = 3 0064	Read	ADC DATA 3.5 1 ADC CRY (VUT); Cata Reattack ADC CRY (VUT); Cata Reattack ADC CRY (VIT); Cata Reattack ADC CRY (VIT); Cata Reattack ADC CRY (VIT); Cata Reattack ADC CRY (VIT); Cata Reattack	$\label{eq:2.1} \begin{array}{l} 0.0000 \\$	Peed		
	ADC CAIA 14 KOC CH 300/T10/bit Reatback ADC CH 300/T10/bit Reatback ADC CH 300/T10/bit Reatback ADC CH 300/T10/bit Reatback ADC CH 300/T10 bit Reatback ADC CH 300/T10 bit Reatback ADC CH 300/T10 bit Reatback	[M01 = 4 000A [M02 = 4 000A [M02 = 4 000A [M03 = 8 000A [M03 = 8 000A [M03 = 8 000A	- Fast	ADC Dalk 3.11 ADC OHP (VOLTE) Cale Nextexis ADC OHP (VOLTE)	[0x00 = 0.000v (0x00 = 0.000v [0x00 = 0.000v (0x00 = 0.000v (0x00 = 0.000v	Peed		
	200 0415 14 200 041 2017/0488 Realman 200 041 2017/0488 Realman 200 041 2017/0488 Realman 200 041 2017/0488 Realman 200 041 2017/0588 Realman 200 041 2017/0588 Realman 200 041 2017/0588 Realman 200 04120 2018	[b00 = 4 6004 [b00 = 4 6004 [b00 = 4 6004 [b00 = 2 6004 [b00 = 2 6004 [b00 = 2 0004 [b00 = 2 0004		ACC DATA THE ACC OHE (VOTE) Calls Readlesin ACC Control (VOTE) Calls Readlesin ACC Call Read	[hold = 5 000V [dold = 5 000V [dold = 5 000V [hold = 5 000V [hold = 6 000V	Past		
	ADD CAINs 14 KOC CH1 200/T10/bite Readback ADD CH1 200/T10 Dist Readback ADD CH1 200/T10 D	[bolt = 4 4964 [bolt = 4 6964 [bolt = 4 6964 [bolt = 4 6964 [bolt = 3 0000 [bolt = 3 0000 [bolt = 3 0000 [bolt = 3 0000 [bolt = 3 0000	fast	ADC Dalls 3 ct ADC Del 10 (SUT) Dals Readleaix ADC Centigenition 34 ADC Centigenition 34 ADC Centigenition 34 ADC Centigenition 34	(min = 5 000) (min = 5 000) (min = 5 000) (min = 273 000eg); (min = 273 000eg); (min = 5 000) (min = 5 000) (min = 5 000) (min = 5 000)	Peed		
	ADC CAIX.1-16     ADC CH 2017/1-04th Realitian     HOC CH 2017/1-04th     Realitian     HOC CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Realitian     Hoc CH 2017/1-04th     Hoc CH 2017/1     Hoc CH 2	(b)00 = 4 4004.           (b)01 = 4 4004.           (b)01 = 4 4004.           (b)02 = 4 4004.           (b)02 = 8 4004.           (b)04 = 8 0004.           (b)04 = 8 0004.           (b) 1 = 6 0004.           (b) 1 = 6 0004.           (b) 1 = 5 0004.           (b) 1 = 5 0004.	And And And And	ADC Dalk 3.11 ADC Def (XOTE) Dalk Nasteaux ADC Dalk Nasteaux ADC Dalk Nast	(add = 6.300v           (add = 6.300v)           (add = 6.300v)	Field Onk		
	ADD CAIN 14 ADD CH ADVTUCAIs Realised ADD CH ADVTUCAIS Realised ADD CH ADVTUCAIS Realised ADVTUCAIS ADVTUCAIS REALISED REALISED REALIS	b00 = 4 4004  b00 = 4 6004  b00 = 4 6004  b00 = 5 6004  b00	- And 	ACC Data 3-th ACC DHI (VALTE) Data Readback ACC DHI (VALTE) DATA R	[wint = 5 Mint (wint = 5 Mint) (wint = 5 Mint) (wint = 5 Mint (wint = 5 Mint) (wint = 5 Mint) (wint) (wint = 5 Mint) (wint =	Feed Send		
	ADD CAINs 14 ADD CH 200/T10/bits Readback ADD CH 200/T10/D10/D10/D10/D10/D10/D10/D10/D10/D10/D	(bit) = 4 4004.           (bit) = 4 0004.           (bit) = 4 0004.           (bit) = 4 0004.           (bit) = 0 0004.           (bit) = 3 0004.           (bit) = 5 0004.	Fast	ADC Dalls 3.11 ADC DM (76/17) Dalls Readback ADC DM (70/16) Dalls Readback ADC DM (70/16) Dalls Readback ADC DM (10/16)	(and - 5 300)*	Final Only		
	ADC CAIA: 14     40     CH 2017/10/48     Fisablack     ADC CH 2017/10/48     Fisablack     Control     ADC CH 2017/10/48     Fisablack     Control     ADC Channel 11     Fisablack     Control     ADC Channel 1     Fisablack     Control     ADC Channel 1     Fisablack     Control     ADC Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Channel     Fisablack     Control     ADC     Control     Control     Fisablack     Control     ADC     Control     Fisablack     Control	(b0) = 4 604.           (b0) = 4 604.           (b0) = 4 604.           (b0) = 8 604.           (b0) = 8 604.           (b0) = 8 604.           (b1) = 1 6044.           (b1) = 1 6049.	Fast 20%	Add Balls Ans Add Christ (Krist Add Rawslaw) Add Raw	Sector = 5 3000v           Sector = 5 3000v           Sector = 5 2000v           Sector = 5 200v           Sector = 5 200v <td>Field</td>	Field		
	ADC CAIA 1-6 ADC CH 2017/10/data Readmain ADC ADA RE	boli = 4 4004   boli = 4 6004   boli = 4 6004   boli = 6 6004   boli = 8 6004   boli		ADC DATA 3-11 ADC OHF OF UT II Data Readback ADC OHF OF UT II Data Readback ADC OHF OF UT II Data Readback ADC OHF OHF Data Readback ADC OHF OHF Data Readback ADC OHF OHF Data Readback ADC OHF OHF OHF AND AND AND AND AND ADC OHM II Data Analysis ADC OHM II DATA ANALYSIS	(mil) = 3 bills/           (mil) = 8 bills/           (mil) = 8 bills/           (mil) = 2 bills/           (mil) = 2 bills/           (mil) = 1	field for		
	Jabo Calls 14 400 CH 2017 Calls Realitian 400 Channel 11 Readiant Control 400 Channel 11 Readiant Control	(b)00 = 4 4004.           (b)01 = 4 4004.           (b)01 = 4 4004.           (b)01 = 3 4004.           (b)01 = 3 4004.           (b) = 2 4004.           (b) = 5 5004.	Fast	ADC Dalls 3.11 ADC COP (SUT) Dals Nachburk ADC Contigention 34 ADC Cont	(and - 5 300)*           (bno)*           (bno)*           (and - 5 300)*           (and - 5 300)*           (and - 5 300)*           (and - 5 300)* <td< td=""><td>Find Only</td></td<>	Find Only		

Figure 11. ADC Configuration Window

#### **PCB Layout Guidelines**

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Refer to the *PCB Layout Guidelines* of the MAX77542 data sheet at https://www.analog.com/max77542evkit

### **Ordering Information**

PART	TYPE
MAX77542EVKIT#	EV Kit

#Denotes RoHS compliance.

## Evaluates: MAX77542 in WLP Package

### MAX77542 EV Kit Bill of Materials

REF_DES	QTY*	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
C1, C4, C5	3	C1005X7S1A225K050BC	ток	2.2µF	CAP; SMT (0402); 2.2UF; 10%; 10V; X7S; CERAMIC
C2	1	C1005X5R1E225K050; GRM155R61E225KE11	TDK;MURATA	2.2µF	CAP; SMT (0402); 2.2µF; 10%; 25V; X5R; CERAMIC
C3, C6	2	C1005X7S1A105K; GRM155C71A105KE11	TDK;MURATA	1µF	CAP; SMT (0402); 1µF; 10%; 10V; X7S; CERAMIC
C7, C16, C25, C34	4	C1608X5R1E106M080AC; CL10A106MA8NRNC; GRM188R61E106MA73; ZRB18AR61E106ME01; GRT188R61E106ME13	TDK;SAMSUNG ELECTRONICS; MURATA; MURATA;MURATA	10µF	CAP; SMT (0603); 10µF; 20%; 25V; X5R; CERAMIC
C8, C17, C26, C35	4	C1005X7R1C104K050BC; ATC530L104KT16; 0402YC104KAT2A; C0402X7R160-104KNE; CL05B104KO5NNNC; GRM155R71C104KA88; C1005X7R1C104K; CC0402KRX7R7BB104; EMK105B7104KV; CL05B104KO5	TDK;AMERICAN TECHNICAL CERAMICS;AVK; VENKEL LTD.;SAMSUNG ELECTRONICS; MURATA; TDK;YAGEO PHICOMP;TAIYO YUDEN;SAMSUNG ELECTRONICS	0.1µF	CAP; SMT (0402); 0.1µF; 10%; 16V; X7R; CERAMIC
C9-C14, C18-C23, C27-C32, C36-C41	24	C1608X5R1A226M080AC; GRM188R61A226ME15; CL10A226MPCNUBE; CL10A226MPMNUB; GRM187R61A226ME15	TDK;MURATA; SAMSUNG; SAMSUNG;MURATA	22µF	CAP; SMT (0603); 22µF; 20%; 10V; X5R; CERAMIC
C15, C24, C33, C42, C53, C55, C58-C60, C63, C65-C67, C69-C71, C75, C80	18	GRM155R71E104KE14; C1005X7R1E104K050BB; TMK105B7104KVH; CGJ2B3X7R1E104K050BB	MURATA;TDK;TAIYO YUDEN;TDK	0.1µF	CAP; SMT (0402); 0.1µF; 10%; 25V; X7R; CERAMIC
C44-C47	4	TMK325ABJ476MM	TAIYO YUDEN	47µF	CAP; SMT (1210); 47µF; 20%; 25V; X5R; CERAMIC
L1, L2	2	DFE252012F-1R0M	MURATA	1UH	EVKIT PART - INDUCTOR; SMT (1008); METAL; 1UH; 20%; 3.3A
L3, L4	2	XEL4020-152ME	COIL CRAFT	1.5UH	INDUCTOR; SMT; N/A; 1.5UH; 20%; 7.5A
U1	1	MAX77542AAWU+	ADI	MAX77542AAWU+	EVKIT PART-IC; MAX77542; PACKAGE OUTLINE: 21-100610; PACKAGE CODE: W602A4Z+1; WLP60
COMPONE	NTS BELC	OW THIS LINE ARE OUTSIDE O	F THE IMMEDIATE MAX7754	2 EVALUATION CIRCU	JIT AND SOLUTION SILKSCREEN.
ALT_IN, CE, CFG1, CFG2, IRQB, MFI01-MFI08, SCL, SDA, SEL1- SEL4, VL12, VL34	21	5002	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; WHITE; PHOSPHOR BRONZE WIRE SILVER;

## Evaluates: MAX77542 in WLP Package

## MAX77542 EV Kit Bill of Materials (continued)

REF_DES	QTY*	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
C50-C52	3	ANY	ANY	10µF	CAPACITOR; SMT (0603); CERAMIC CHIP; 10µF; 16V; TOL=20%; MODEL=GRM SERIES; TG=-55 DEGC TO +85 DEGC; TC=X5R; FORMFACTOR
C54, C61, C64	3	C1005X5R1A475K050	ток	4.7µF	CAP; SMT (0402); 4.7µF; 10%; 10V; X5R; CERAMIC
C56, C57	2	C0402C0G500270JNP; GRM1555C1H270JA01	VENKEL LTD.;MURATA	27PF	CAP; SMT (0402); 27PF; 5%; 50V; C0G; CERAMIC
C72-C74, C79	4	C0402C105K8PAC; CC0402KRX5R6BB105	KEMET;YAGEO	1µF	CAP; SMT (0402); 1µF; 10%; 10V; X5R; CERAMIC
C76, C78	2	ZRB15XR61A475ME01; CL05A475MP5NRN; GRM155R61A475MEAA; C1005X5R1A475M050BC	MURATA;SAMSUNG; MURATA;TDK	4.7µF	CAP; SMT (0402); 4.7µF; 20%; 10V; X5R; CERAMIC
C77	1	C0402C103K5RAC; GRM155R71H103KA88; C1005X7R1H103K050BE; CL05B103KB5NNN; UMK105B7103KV	KEMET;MURATA;TDK; SAMSUNG ELECTRONIC;TAIYO YUDEN	0.01µF	CAP; SMT (0402); 0.01µF; 10%; 50V; X7R; CERAMIC
DS1, DS2	2	LTST-C190CKT	LITE-ON ELECTRONICS INC.	LTST-C190CKT	DIODE; LED; STANDARD; RED; SMT (0603); PIV=5.0V; IF=0.04A; -55 DEGC TO +85 DEGC
GND, PGND7	2	5011	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
IN1-IN4, LOAD1, LOAD2, OUT1- OUT4, PGND, PGND1-PGND6, SYS	18	9020 BUSS	WEICO WIRE	MAXIMPAD	EVK KIT PARTS; MAXIM PAD; WIRE; NATURAL; SOLID; WEICO WIRE; SOFT DRAWN BUS TYPE-S; 20AWG
IN1S-IN4S, LOADSP, OUT1S-OUT4S, VDD, VIO	11	5000	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; RED; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
J1	1	10118193-0001LF	FCI CONNECT	10118193-0001LF	CONNECTOR; FEMALE; SMT; MICRO USB B TYPE RECEPTACLE; RIGHT ANGLE; 5PINS
J2	1	PBC02SAAN	SULLINS ELECTRONICS CORP.	PBC02SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 2PINS
J3, J4, J8-J17, J19, J20	14	TSW-103-07-T-S	SAMTEC	TSW-103-07-T-S	CONNECTOR; THROUGH HOLE; TSW SERIES; SINGLE ROW; STRAIGHT; 3PINS

## Evaluates: MAX77542 in WLP Package

## MAX77542 EV Kit Bill of Materials (continued)

REF_DES	QTY*	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
J5-J7	5	TSW-102-26-T-T	SAMTEC	TSW-102-26-T-T	CONNECTOR; THROUGH HOLE; TSW SERIES; TRIPLE ROW; STRAIGHT; 6PINS
J18	1	PBC05SAAN	SULLINS ELECTRONICS CORP.	PBC05SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 5PINS; -65 DEGC TO +125 DEGC
L9, L10	2	DFE252012F-1R0M	MURATA	1UH	EVKIT PART - INDUCTOR; SMT (1008); METAL; 1UH; 20%; 3.3A
L11, L12	2	XEL4020-152ME	COIL CRAFT	1.5UH	INDUCTOR; SMT; N/A; 1.5UH; 20%; 7.5A
L5-L8	4	DFE252012F-R47M	MURATA	0.47UH	EVKIT PART - INDUCTOR; SMT (1008); METAL; 0.47UH; 20%; 4.9A
L13-L15	3	BLM18AG601SN1	MURATA	600	INDUCTOR; SMT (0603); FERRITE-BEAD; 600; TOL=+/-; 0.5A
LOADSN, PGND1S-PGND4S	5	5001	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH;
MH1-MH4	4	9032	KEYSTONE	9032	MACHINE FABRICATED; ROUND-THRU HOLE SPACER; NO THREAD; M3.5; 5/8IN; NYLON
R1, R58, R71, R72, R76-R80	9	RC0402FR-0710KL; CR0402-FX-1002GLF	YAGEO;BOURNS	10K	RES; SMT (0402); 10K; 1%; +/-100PPM/ DEGC; 0.0630W
R2, R3, R61, R62	4	ERJ-2GEJ472	PANASONIC	4.7K	RES; SMT (0402); 4.7K; 5%; +/-200PPM/ DEGC; 0.1000W
R4, R7, R9, R12, R44-R50, R57, R67-R70	14	RC0402JR-070RL; CR0402-16W-000RJT	YAGEO PHYCOMP;VENKEL LTD.	0	RES; SMT (0402); 0; 5%; JUMPER; 0.0630W
R5, R6, R8, R10, R11, R13, R23, R25, R29, R56, R59, R66, R73, R75	14	RC0402JR-070RL; CR0402-16W-000RJT	YAGEO PHYCOMP;VENKEL LTD.	0	RES; SMT (0402); 0; 5%; JUMPER; 0.0630W
R14, R16, R18, R20, R22, R24	6	3296Y-1-204LF	BOURNS	200K	RESISTOR; THROUGH HOLE-RADIAL LEAD; 3296 SERIES; 200K OHM; 10%; 100PPM; 0.5W
R15	1	ERJ-2RKF1871	PANASONIC	1.87K	RES; SMT (0402); 1.87K; 1%; +/-100PPM/ DEGC; 0.1000W
R17	1	CRCW040230K9FK	VISHAY DALE	30.9K	RES; SMT (0402); 30.9K; 1%; +/-100PPM/ DEGC; 0.0630W
R19	1	CRCW040264K9FK; RC0402FR-0764K9L	VISHAY;YAGEO	64.9K	RES; SMT (0402); 64.9K; 1%; +/-100PPM/ DEGK; 0.0630W
R21, R64	2	CRCW0402100KFK; RC0402FR-07100KL	VISHAY;YAGEO	100K	RES; SMT (0402); 100K; 1%; +/-100PPM/ DEGC; 0.0630W

## Evaluates: MAX77542 in WLP Package

## MAX77542 EV Kit Bill of Materials (continued)

REF_DES	QTY*	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
R26, R65	2	RC0402FR-072K2L	YAGEO	2.2K	RES; SMT (0402); 2.2K; 1%; +/-100PPM/ DEGC; 0.0630W
R27, R74	2	RC0402FR-0722RL	YAGEO PHYCOMP	22	RES; SMT (0402); 22; 1%; +/-100PPM/ DEGC; 0.0630W
R28	1	CRCW0402470RFK	VISHAY DALE	470	RES; SMT (0402); 470; 1%; +/-100PPM/ DEGC; 0.0630W
R51, R52	2	RC0402FR-0727RL	YAGEO	27	RES; SMT (0402); 27; 1%; +/-100PPM/ DEGC; 0.0630W
R53	1	ERJ-2RKF1202	PANASONIC	12K	RES; SMT (0402); 12K; 1%; +/-100PPM/ DEGC; 0.1000W
R54	1	CRCW04021M00FK	VISHAY DALE	1M	RES; SMT (0402); 1M; 1%; +/-100PPM/ DEGC; 0.0630W
R55	1	ERJ-2RKF1001	PANASONIC	1K	RES; SMT (0402); 1K; 1%; +/-100PPM/ DEGC; 0.1000W
R60	1	RC0402FR-07150RL	YAGEO	150	RES; SMT (0402); 150; 1%; +/-100PPM/ DEGC; 0.0630W
R63	1	CRCW0402169KFK	VISHAY DALE	169K	RES; SMT (0402); 169K; 1%; +/-100PPM/ DEGK; 0.0630W
U3	1	MAX38902A-ATA+	MAXIM	MAX38902A-ATA+	EVKIT PART - IC; MAX38902A-ATA+; PACKAGE OUTLINE DEVICE: 21-0168; PACKAGE CODE XXXX
U4	1	MAX8512EXK+	MAXIM	MAX3395EETC	IC; TRANS; 15KV ESD-PROTECTED HIGH-DRIVE CURRENT QUAD-LEVEL TRANSLATOR WITH SPEED-UP CIRCUITRY; TQFN12 4X4
U5, U8	2	MAX3395EETC+	MAXIM	MAX3395EETC	IC; TRANS; 15KV ESD-PROTECTED HIGH-DRIVE CURRENT QUAD-LEVEL TRANSLATOR WITH SPEED-UP CIRCUITRY; TQFN12 4X4
U6	1	FT2232HL	FUTURE TECHNOLOGY DEVICES INTL LTD.	FT2232HL	IC; MMRY; DUAL HIGH-SPEED USB TO MULTIPURPOSE UART/FIFO; LQFP64
VUSB	1	5010	KEYSTONE	N/A	TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN; BOARD HOLE=0.063IN; RED; PHOSPHOR BRONZE WIRE SIL;
Y1	1	7M-12.000MAAJ	TXC CORPORATION	12MHZ	CRYSTAL; SMT; 12MHZ; 18PF; TOL = +/-30PPM; STABILITY = +/-30PPM

## Evaluates: MAX77542 in WLP Package

### MAX77542 EV Kit Schematic



## Evaluates: MAX77542 in WLP Package



## MAX77542 EV Kit Schematic (continued)

## Evaluates: MAX77542 in WLP Package

# 12F-R47M L8 SPARE INDUCTORS DFE252012F-R47N 1ROM 0.47UH 147UH 5 47UH 847M 47UH L10 ₹₹ 9 Ξ Ω Ω ი DFE25201 DFE2520 4 SPARE RESISTORS R67 0 25138E1 R68 0 25138E2 R69 0 251286 R70 0 251286 EV\_KIT\_BOX MECHANICAL STAND OFF 33 H

### MAX77542 EV Kit Schematic (continued)

## Evaluates: MAX77542 in WLP Package

### MAX77542 EV Kit PCB Layout



MAX77542 EV—Silk Top



MAX77542 EV—Top



MAX77542 EV—Internal2



MAX77542 EV—Internal3

## Evaluates: MAX77542 in WLP Package



### MAX77542 EV Kit PCB Layout (continued)

MAX77542 EV—Internal4



MAX77542 EV—Internal5



MAX77542 EV—Bottom



MAX77542 EV—Silk Bottom

## Evaluates: MAX77542 in WLP Package

### **Revision History**

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	03/23	Initial release	—

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