MAX32690
ERRATA SHEET

Revision A2 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the top side of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the product webpage at www.analog.com/MAX32690.

1) SPIXF MAY READ INCORRECT ADDRESSES OF NON-PROGRAM DATA IF BUS IDLE TIMER LIMIT IS 0

Description:
SPIXF will not send a new address, and thus return incorrect values, if there is no idle time between two consecutive reads of non-program data that both generate a cache miss. This issue does not affect SPIXF reads of program data. (18144)

Workaround:
Set SPIXF_BUS_IDLE.busidle to 1 instead of setting SPIXF_BUS_IDLE.busidle to 0. This will have minimal effect on the speed of sequential code execution.

2) ECC FEATURE NOT SUPPORTED

Description:
This feature is not supported on this revision of the device. Treat all register fields associated with this feature as Do Not Modify (DNM). (18104)

Workaround:
None.

3) PHYSICALLY UNCLONABLE FUNCTION (PUF) FEATURE NOT SUPPORTED

Description:
This feature is not supported on this revision of the device. Treat all register fields associated with this feature as Do Not Modify (DNM). (1897).

Workaround:
None.

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4) INTERNAL TEMPERATURE SENSOR NOT SUPPORTED

Description:
This feature is not supported on this revision of the device. Treat all register fields associated with this feature as Do Not Modify (DNM). (18121)

Workaround:
None.

5) FLASH MEMORY MAY BE CORRUPTED DURING POWER-DOWN

Description:
An insufficient decay time of the V_{DDIO} supply can corrupt the flash memory contents.

Workaround:
The decay time of the V_{DDIO} supply from $V_{RST(VDDIOMIN)}$ to 1.47V must be greater than 100µs. V_{DDA} must be connected to V_{DDIO} as originally stated in the data sheet.

6) FLASH MEMORY MAY BE CORRUPTED DURING POWER-DOWN WHEN OPERATING IN DUAL-SUPPLY MODE

Description:
Incorrect sequencing of the V_{DDIO} and V_{CORE} supplies can corrupt the flash memory contents.

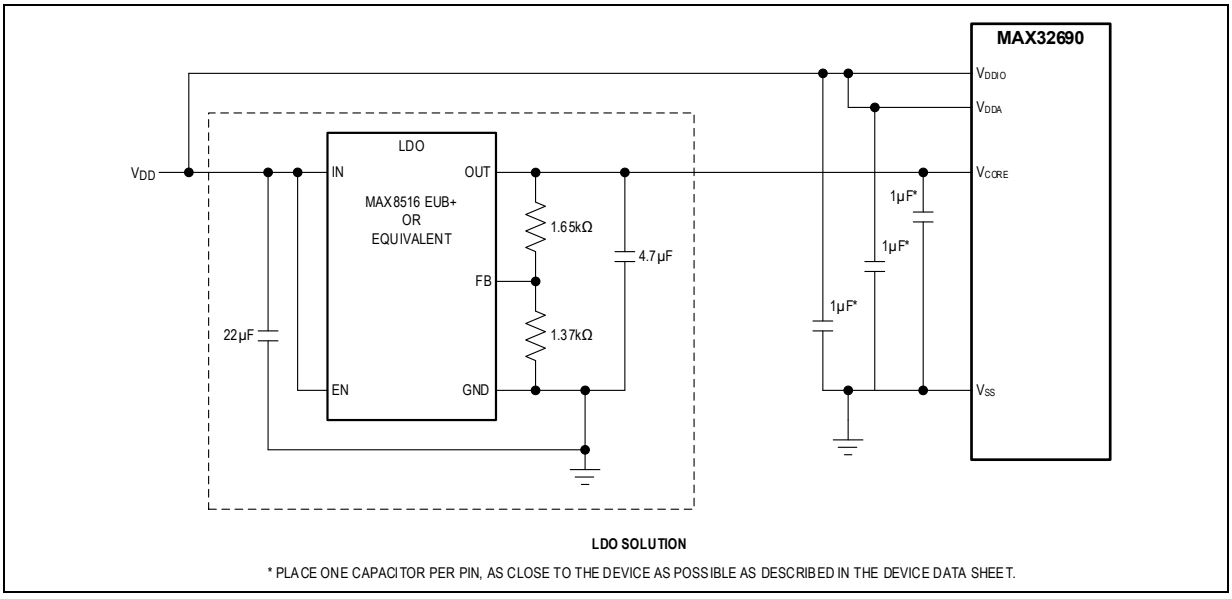
Workaround:
1. Control the power supplies so that:
   - $V_{CORE} \geq V_{CORE(MIN)}$ before $V_{DDIO} > V_{RST(VDDIOMIN)}$ on power-up
   - $V_{DDIO} < V_{RST(VDDIOMIN)}$ before $V_{CORE} \leq V_{CORE(MIN)}$ on power-down

or

2. Ensure RSTN is asserted active whenever $V_{CORE} \leq V_{CORE(MIN)}$.

V_{DDA} must be connected to V_{DDIO} as originally stated in the data sheet.

Workaround #1 can be implemented using an LDO such as the MAX8516 or equivalent as shown. The LDO is guaranteed to regulate its output, which drives V_{CORE} well below $V_{RST(VDDIOMIN)}$.



LDO SOLUTION

* PLACE ONE CAPACITOR PER PIN, AS CLOSE TO THE DEVICE AS POSSIBLE AS DESCRIBED IN THE DEVICE DATA SHEET.

7) BACK-TO-BACK ZEROIZATION ON IDCACHE0 DOES NOT WORK

Description:
Performing back-to-back zeroization operations on the cache does not work as expected. (1854)

Workaround:
Invalidate the cache immediately after the zeroization to properly zeroize the flash.

8) BACK-TO-BACK ZEROIZATION ON IDCACHEXIP DOES NOT WORK

Description:
Performing back-to-back zeroization operations on the cache does not work as expected. (1868)

Workaround:
Invalidate the cache immediately after the zeroization to properly zeroize the flash.

9) GPIO3[7:0] MAXIMUM VOLTAGE IS V_{DD3A}

Description:
Analog inputs will source current into the V_{DD3A} supply if the voltage exceeds V_{DD3A}. (1898)

Workaround:
Ensure the voltage applied to GPIO3[7:0] is less than or equal to V_{DD3A}.

10) SYSTEM CLOCK FREQUENCY DOES NOT CORRESPOND TO DEFAULT REGISTER SETTINGS AFTER SYSTEM RESET

Description:
The system oscillator prescaler divider logic does not get reset to match the GCR CLKCTRL.sysclk_div field value following a system reset. Instead, the logic will match the prescaler value prior to the system reset. The logic will match the GCR CLKCTRL.sysclk_div values following other types of reset events for that field that are described in the user guide. (18133)

Workaround:
Rewrite GCR CLKCTRL.sysclk_div after a reset to set the prescaler to the correct value.

11) UART TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18117)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

12) UART TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18135)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

13) I²S TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18118)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

14) I²S TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18136)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

15) I2C1A_SDA AND I2C1A_SCL MAPPED TO P2.17 OR P2.18 DO NOT SUPPORT I²C Hs-MODE OPERATION

Description:
In Hs-Mode operation, the I2C1_SDA and I2C1_SCL signals are not driven correctly on P2.17 or P2.18 when they are configured for alternate function 1. (1873)

Workaround:
For Hs-Mode operation, use P0.11 and P0.12 configured for alternate function 1 to access the I2C1_SDA and I2C1_SCL signals.

16) ENABLING I²C ALTERNATE FUNCTIONS DISABLES FUNCTIONALITY OF SOME PINS

Description:
Multiple instances of some I²C port's SDA and SCL signals are mapped to the same alternate function number. When the SCL and SDA pins of one instance are enabled, the pins corresponding to the other mapping on the same alternate function are unintentionally enabled in the same way. (18122)

Workaround:
The pins on the other mapping must not be used and must be left unconnected if the I²C function is enabled.

WHEN ENABLING I²C FUNCTION ON THESE PINS	LEAVE THESE PINS UNCONNECTED
P0.30, AF1 (I2C0A_SDA) P0.31, AF1 (I2C0A_SCL)	P2.7 P2.8
P2.7, AF1 (I2C0A_SDA) P2.8, AF1 (I2C0A_SCL)	P0.30 P0.31
P0.11, AF1 (I2C1A_SDA) P0.12, AF1 (I2C1A_SCL)	P2.17 P2.18
P2.17, AF1 (I2C1A_SDA) P2.18, AF1 (I2C1A_SCL)	P0.11 P0.12
P0.13, AF3 (I2C2C_SDA) P0.12, AF3 (I2C2C_SCL)	P1.7 P1.8
P1.7, AF3 (I2C2C_SDA) P1.8, AF3 (I2C2C_SCL)	P0.13 P0.12

17) CAN PERIPHERAL DOES NOT SUPPORT FD CLOCK RATES

Description:
The CAN peripheral supports the CAN FD protocol but does not support CAN FD clock rates. (18127)

Workaround:
The peripheral should only be used in CAN 2.0B networks.

18) DMA OPERATIONS ON FLASH MEMORY NOT SUPPORTED

Description:
Incorrect data is transferred during DMA operations on flash memory. (1892/18131)

Workaround:
None.

19) IN TARGET MODE, INCORRECT DATA IS TRANSMITTED IF AN EMPTY SPI FIFO IS WRITTEN WHILE A TRANSFER IS IN PROGRESS

Description:
In target mode, if data is fed into an empty transmit FIFO while chip select is active and an SPI transfer is in progress (SPI clock is provided by the controller), the first FIFO byte gets transferred immediately and is seen shifted or incomplete in the SPI MISO line. (18101)

Workaround:
Ensure that the target SPI does not let its transmit FIFO become empty.

20) IN TARGET MODE, SPI FIFO TRANSMITS UNEXPECTED DATA WHEN TX FIFO EMPTY

Description:
After an SPI transmit FIFO is empty, the device is expected to transmit 0x00 on subsequent clocks. Instead, when the FIFO empty condition is met, the device will continue to loop through the FIFO and transmit its contents. (18102)

Workaround:
None.

21) 140 WLP PACKAGE REQUIRES EXTERNAL LDO FOR BLUETOOTH LE OPERATION

Description:
Internal coupling in the 140 WLP package prevents proper operation of the Bluetooth LE peripheral. This issue does not affect any other packages.

Workaround:
If using the Bluetooth LE peripheral, follow these steps:
1. Drive the BLE_LDO pin with an external source that meets the VBLE_LDO_IN (GCR_BTLELDOCTRL.ldotxbyp = 1) electrical specification.
2. Set GCR_BTLELDOCTRL.ldotxbyp = 1 to bypass the internal Bluetooth LE LDO.

22) CACHE LINE FILL BUFFER NOT CLEARED

Description:
The cache line fill buffer is not automatically cleared when the cache is enabled, resulting in stale data. (18114)

Workaround:
Invalidate the cache, enable it, then invalidate it again to clear the stale data.

23) DEFAULT OSCILLATOR AUTOCALIBRATION TRIM SETTING INCORRECT

Description:
The autocalibration feature will not calibrate to the correct frequency with the default trim value. (18109)

Workaround:
Write FCR_AUTOCAL1.inittrm = 0x64 before beginning an autocalibration operation.

24) GCR CODE FLUSH DOES NOT WORK AFTER PROGRAMMING SAME FLASH ROW MULTIPLE TIMES

Description:
After programming the same flash location twice, the GCR Code Flush feature should allow the system to read the updated flash data from that location. Instead, the old, stale flash data is read back. (18105)

Workaround:
Use the ICC invalidate instead of setting Bit 6 of GCR.SCON register to perform a code flush.

25) UART RECEIVE FIFO FAILS TO ASSERT OVERRUN INTERRUPT

Description:
The receive FIFO does not reliably assert the overrun interrupt. (18125)

Workaround:
Poll the receive FIFO level and use software to manage the FIFO contents.

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REV A2 ERRATA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/22	Initial release	—
1	7/23	Added errata 1–6	All
2	1/24	Reworded erratum 1 for clarity; ECC and PUF errata changed from "removed" to "not supported on this revision;" removed individual ECC errata 3–5; added errata 4–25	All