*Click **here** to ask an associate for production status of specific part numbers.*

MAX32690

Arm Cortex-M4 with FPU Microcontroller and Bluetooth LE 5 for Industrial and Wearables

General Description

The MAX32690 microcontroller (MCU) is an advanced system-on-chip (SoC) featuring an Arm® Cortex®-M4F CPU, large flash and SRAM memories, and the latest generation Bluetooth® 5.2 Low Energy (LE) radio. This device unites processing horsepower with the connectivity required for IoT applications.

The MAX32690 is qualified to operate over the -40°C to +105°C range, which is ideal for industrial environments. This device is available in a 68-pin TQFN-EP (0.40mm pitch) and a 140-bump WLP (0.35mm pitch).

Bluetooth 5.2 Low Energy (LE) radio supports Mesh, angle of arrival (AoA), and angle of departure (AoD) for direction finding, long-range (coded), and high-throughput modes. LE Audio hardware implemented with software codec is provided separately. A RISC-V core optionally handles timing-critical controller tasks, freeing the programmer from Bluetooth LE interrupt latency concerns.

A cryptographic toolbox (CTB) provides advanced security features, including an MAA for fast Elliptic Curve Digital Signature Algorithm (ECDSA), Advanced Encryption Standard (AES) Engine, TRNG, SHA-256 hash, and secure boot loader. Internal code and SRAM space can be expanded off-chip through two quad-SPI execute-in-place (SPIXF and SPIXR) interfaces up to 512MB each.

Many high-speed interfaces are supported on the device, including multiple QSPI, UART, CAN 2.0B, and I^2C serial interfaces, plus one I^2S port for connecting to an audio codec. All interfaces support efficient DMA-driven transfers between peripheral and memory. A 12-input (8 external), 12-bit SAR ADC samples analog data at up to 1Msps.

Applications

- Fitness/Health Wearables
- Portable and Wearable Wireless Medical Devices
- Asset Tracking
- Industrial Sensors and Networks

Benefits and Features

- Ultra-Efficient Microcontroller for Battery-Powered Applications
  - 120MHz Arm Cortex-M4 Processor with FPU
  - Ultra-Low-Power, 32-Bit RISC-V (RV32) Coprocessor Available to Offload Data Processing
  - 7.3728MHz and 60MHz Low-Power Oscillators
  - External Crystal Support (32MHz Required for Bluetooth LE)
  - 32.768kHz RTC Clock (Requires External Crystal)
  - 8kHz Always-on Ultra-Low Power Oscillator
  - 3.25MB Internal Flash, 1MB Internal SRAM
  - 85µW/MHz ACTIVE Mode at 1.1V
  - 1.8V and 3.3V I/O with No Level Translators
  - External Flash and SRAM Expansion Interfaces
- Bluetooth 5.2 LE Radio
  - Fully Open-Source Bluetooth 5.2 Stack Available
  - Supports AoA, AoD, LE Audio, and Mesh
  - High-Throughput (2Mbps) Mode
  - Long-Range (125kbps and 500kbps) Modes
  - Rx Sensitivity: -97dBm; Tx Power: +4.5dBm
  - Single-Ended Antenna Connection (50Ω)
- Optimal Peripheral Mix Provides Platform Scalability
  - 16-Channel DMA
  - Five Quad-SPI Controller (60MHz)/Peripheral (30MHz)
  - Four UARTs with Flow Control
  - Two I^2C
  - I^2S
  - Eight External Channel, 12-Bit 1Msps SAR ADC
  - USB 2.0 Hi-Speed Device
  - 16 Pulse Train Engines
  - Four 32-Bit/Dual 16-Bit Timers with 8mA High Drive
  - Two 32-Bit/Dual 16-Bit Low-Power Timers
  - Two CAN 2.0B Controllers
  - Four Micropower Comparators
  - 1-Wire Controller
- Cryptographic Tool Box (CTB) for IP/Data Security
  - Modular Arithmetic Accelerator (MAA), True Random Number Generator (TRNG)
  - Secure Nonvolatile Key Storage, SHA-256, AES-128/192/256
- Optional Secure Communications Protocol Bootloader (SCPBL)

Ordering Information appears at end of data sheet.

19-101599; Rev 1; 5/23

Simplified Block Diagram

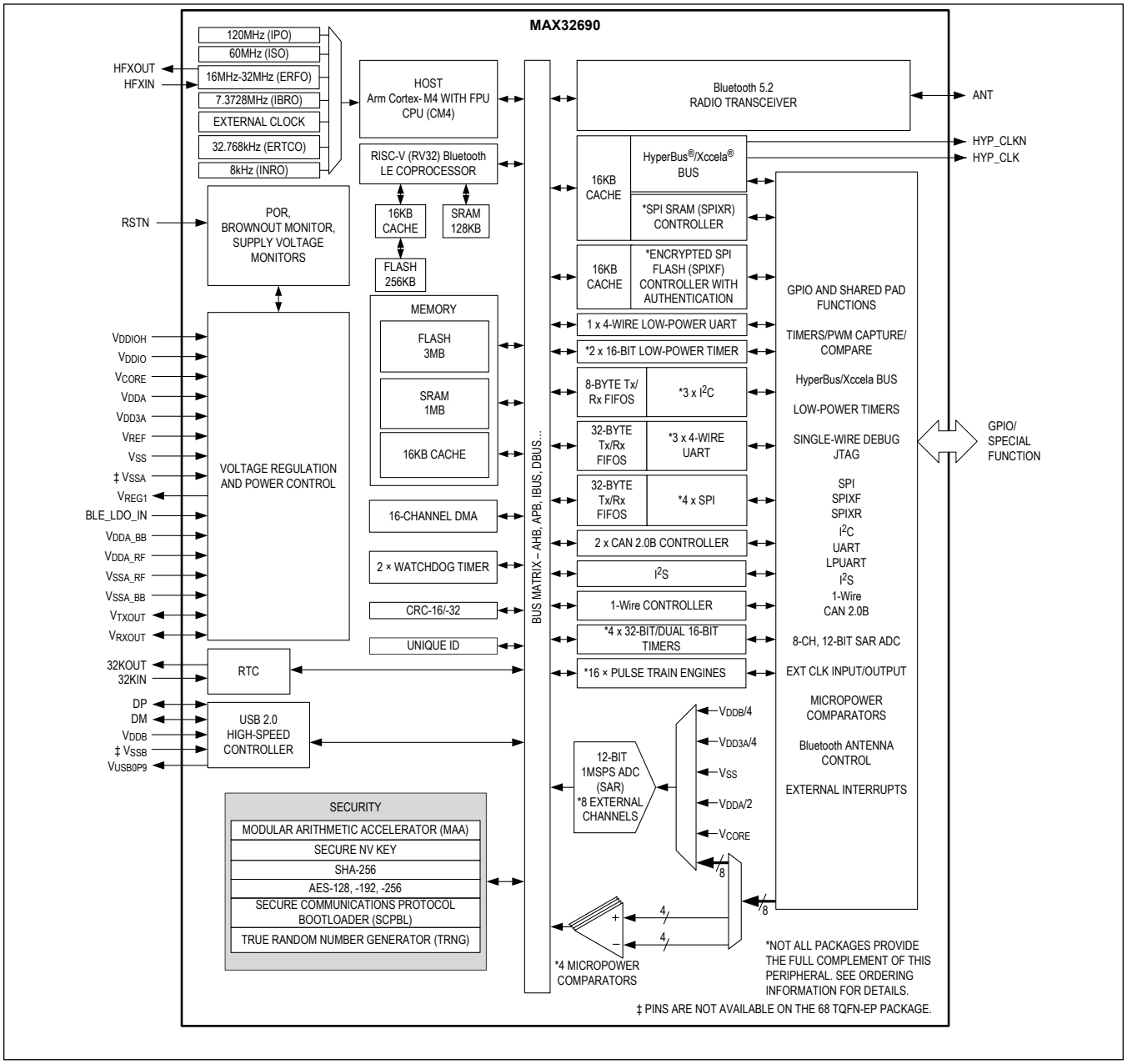


TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

V_{CORE} ..... -0.3V to +1.21V
V_{DDIO}, V_{DDA} ..... -0.3V to +1.89V
V_{DD3A}, V_{DDIOH} ..... -0.3V to +3.6V
V_{DDA_BB}, V_{DDA_RF} ..... -0.3V to +1.21V
V_{REF} ..... -0.3V to V_{DD3A} + 0.3V
BLE_LDO_IN (GCR_BTLELDOCTRL.ldotxbyp = 0) .....-0.3V to +1.89V
BLE_LDO_IN (GCR_BTLELDOCTRL.ldotxbyp = 1) .....-0.3V to 1.21V
RSTN, GPIO (V_{DDIOH}) .....-0.3V to V_{DDIOH} + 0.3V
RSTN, GPIO (V_{DDIO}) .....-0.3V to V_{DDIO} + 0.3V
32KIN, 32KOUT ..... -0.3V to V_{DDA} + 0.2V
HFXIN, HFXOUT .....-0.3V to V_{CORE} + 0.2V
HFXIN, HFXOUT (device pins shall not exceed) 1.21V
DM, DP (with respect to V_{SSB}) ..... -0.3V to +3.6V
V_{DDB} (with respect to V_{SSB}) .....-0.3V to +3.6V
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
V_{DDIO} Combined Pins (sink) 100mA
V_{DDIOH} Combined Pins (sink) 100mA
V_{SSA}, V_{SSA_RF}, V_{SSA_BB} 100mA
V_{SS} 100mA
Continuous Package Power Dissipation TQFN (multilayer board)
T_A = +70°C (derate 49.5mW/°C above +70°C) 3960.40mW
Continuous Package Power Dissipation WLP (multilayer board)
T_A = +70°C (derate 28.47mW/°C above +70°C) 1564.72mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +125°C
Soldering Temperature .....+260°C

Note 1: No device pins can exceed 3.6V. All voltages with respect to V_{SS} unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

68 TQFN-EP

Package Code	T6888+2
Outline Number	21-0510
Land Pattern Number	90-0354
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	20.20°C/W
Junction to Case (θ_{JC})	1°C/W

140 WLP

Package Code	W1404B4+1
Outline Number	21-100618
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35.13°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage, Core	V_{CORE}	f_{SYS_CLK} = 120MHz	0.99	1.1	1.21	V
Supply Voltage, Analog	V_{DD3A}	V_{DD3A} and V_{DDIOH} must be connected together at the circuit board level.	1.71	3.0	3.6	V
	V_{DDA}	V_{DDA} and V_{DDIO} must be connected together at the circuit board level.	1.71	1.8	1.89	
Supply Voltage, GPIO	V_{DDIO}	V_{DDA} and V_{DDIO} must be connected together at the circuit board level.	1.71	1.8	1.89	V
Supply Voltage, GPIO (High)	V_{DDIOH}	V_{DD3A} and V_{DDIOH} must be connected together at the circuit board level.	1.71	3.0	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{CORE}		0.76		V
		Monitors V_{DDA}	1.58	1.64	1.7	
		Monitors V_{DDIO}	1.58	1.64	1.7	
		Monitors V_{DDB}		2.95		
		Monitors V_{DDIOH}	1.58	1.64	1.7	
		Monitors V_{RXOUT}		0.773		
		Monitors V_{TXOUT}		0.773		
Power-On Reset Voltage	V_{POR}	Monitors V_{CORE}		0.585		V
		Monitors V_{DDA}		1.175		
		Monitors V_{DD3A}		1.175		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CORE} Current, ACTIVE Mode	I_{CORE_DACT}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{CORE} pin, V_{CORE} = 1.1V, CM4 in ACTIVE mode executing Coremark®, RV32 in SLEEP mode; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		85		µA/MHz
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{CORE} pin, V_{CORE} = 1.1V, CM4 and RV32 in ACTIVE mode executing While(1); inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. This specification is a function of the IPO frequency.		112		
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, total current into V_{CORE} pin, V_{CORE} = 1.1V, CM4 in ACTIVE mode executing While(1), RV32 in SLEEP mode; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		77		
		Dynamic, total current into V_{CORE} pin, V_{CORE} = 1.1V, CM4 in SLEEP mode, RV32 in ACTIVE mode running from ISO; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		73		
	I_{CORE_FACT}	Fixed, IPO enabled, ISO enabled, total current into V_{CORE}, V_{CORE} = 1.1V, CM4 in ACTIVE mode 0MHz, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.		1.79		mA
V_{DDA} Fixed Current, ACTIVE Mode	I_{DDA_FACT}	Fixed, IPO enabled, total current into V_{DDA} pins, V_{DDA} = 1.8, CM4 in ACTIVE mode 0MHz execution, RV32 in ACTIVE mode 0MHz execution; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA, V_{CORE} and V_{DDA} voltage monitors enabled. See *Temperature Variance*.		399		µA
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLP}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 120MHz, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, standard DMA with two channels active; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		25.4		µA/MHz
	I_{CORE_FSLP}	Fixed, IPO enabled, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.		3.4		mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DDA} Fixed Current, SLEEP Mode	I_{DDA_FSLP}	Fixed, IPO enabled, f_{SYS_CLK} = 120MHz, total current into V_{DDA} pins, CM4 in SLEEP mode, RV32 in SLEEP mode, standard DMA with two channels active. See *Temperature Variance*.		399		µA
V_{CORE} Current, LOW POWER Mode	I_{CORE_DLP}	Dynamic, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 powered off, RV32 in ACTIVE mode, $f_{SYS\_CLK(MAX)}$ = 60MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		37.1		µA/MHz
	I_{CORE_FLP}	Fixed, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 powered off, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.		1.01		mA
V_{DDA} Fixed Current, LOW POWER Mode	I_{DDA_FLP}	Standby state with full data retention, IBRO enabled, V_{CORE} and V_{DDA} voltage monitors enabled. See *Temperature Variance*.		54		µA
V_{CORE} Current, MICRO POWER Mode	I_{CORE_DMP}	Dynamic, ERTCO enabled, IBRO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, LPUART active, f_{LPUART} = 32.768kHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		86		µA
V_{CORE} Current, STANDBY Mode	I_{CORE_STBY}	Fixed, total current into V_{CORE} pins, V_{CORE} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.		0.61		µA
V_{DDA} Current, STANDBY Mode	I_{DDA_STBY}	Fixed, total current into V_{DDA} pins, V_{DDA} = 1.8V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.		23		µA
V_{DDIO} Current, STANDBY Mode	I_{DDIO_STBY}	GPIO input; pull-up/pull-down enabled		112		nA
V_{DDIOH} Current, STANDBY Mode	I_{DDIOH_STBY}	GPIO input; pull-up/pull-down enabled		114		nA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DDA} Current, BACKUP Mode	I_{DDA_BKU}	Total current into V_{DDA} pins, V_{DDA} = 1.8V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.	All SRAM retained		13.75		µA
		Total current into V_{DDA} pins, V_{DDA} = 1.8V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. See *Temperature Variance*.	No SRAM retention		2.09		
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_BKU}	V_{CORE} = 1.1V. See *Temperature Variance*.			0.65		µA
V_{DDIO} Current, BACKUP Mode	I_{DDIO_BKU}	GPIO input; pull-up/pull-down enabled			86		nA
V_{DDIOH} Current, BACKUP Mode	I_{DDIOH_BKU}	GPIO input; pull-up/pull-down enabled			110		nA
SLEEP Mode Resume Time	t_{SLP_ON}	Time from power mode exit to execution of first user instruction			0.500		µs
LOW POWER Mode Resume Time	t_{LP_ON}	Time from power mode exit to execution of first user instruction			18		µs
MICRO POWER Mode Resume Time	t_{MP_ON}	Time from power mode exit to execution of first user instruction			20		µs
STANDBY Mode Resume Time	t_{STBY_ON}	Time from power mode exit to execution of first user instruction			23		µs
BACKUP Mode Resume Time	t_{BKU_ON}	Time from power mode exit to execution of first user instruction			2.2		ms
CLOCKS							
System Clock Frequency	f_{SYS_CLK}					120	MHz
System Clock Period	t_{SYS_CLK}				$1/f_{SYS\_CLK}$		ns
Internal Primary Oscillator (IPO)	f_{IPO}				120		MHz
Internal Secondary Oscillator (ISO)	f_{ISO}				60		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}				7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}				8		kHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
External RTC Oscillator (ERTCO)	f_{ERTCO}	32kHz watch crystal, C_{L_XTAL} = 6pF, ESR < 90kΩ, C_0 ≤ 2pF, crystal power dissipation rating minimum 0.5µW, no external load capacitors.			32.768		kHz
External RF Oscillator Frequency (ERFO)	f_{ERFO}	32MHz crystal, C_{L_XTAL} = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm, crystal power dissipation rating minimum 100µW. Refer to the *MAX32690 User Guide* for details on calculating the load capacitors.			32		MHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled			0.3		µA
RTC Power-Up Time	t_{RTC_ON}				250		ms
External I²S Clock Input Frequency	$f_{EXT\_I2S\_CLK}$	I2S_CLKEXT selected				25	MHz
External System Clock Input Frequency	f_{EXT_CLK}	EXT_CLK selected				80	MHz
External Low-Power Timer1 Clock Input Frequency	$f_{EXT\_LPTMR1\_CLK}$	LPTMR1_CLK selected				8	MHz
External Low-Power Timer2 Clock Input Frequency	$f_{EXT\_LPTMR2\_CLK}$	LPTMR2_CLK selected				8	MHz
GENERAL-PURPOSE I/O							
Input Low Voltage for All GPIO Except P4.0 and P4.1	V_{IL_VDDIO}	P4.0 and P4.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO Except for P1.[11:21]	V_{IL_VDDIOH}	P1.[11:21] can only use V_{DDIO} as I/O supply and cannot use V_{DDIOH} as I/O supply	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}	V_{DDIOH} selected as I/O supply			0.5 x V_{DDIOH}		V
		V_{DDIO} selected as I/O supply			0.5 x V_{DDIO}		
Input High Voltage for All GPIO Except P4.0 and P4.1	V_{IH_VDDIO}	P4.0 and P4.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
Input High Voltage for All GPIO Except for P1.[11:21]	V_{IH_VDDIOH}	P1.[11:21] can only use V_{DDIO} as I/O supply and cannot use V_{DDIOH} as I/O supply	V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input High Voltage for RSTN	V_{IH_RSTN}	V_{DDIOH} selected as I/O supply			0.5 x V_{DDIOH}		V
		V_{DDIO} selected as I/O supply			0.5 x V_{DDIO}		
Output Low Voltage for All GPIO Except P4.0 and P4.1	V_{OL_VDDIO}	P4.0 and P4.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Output Low Voltage for P4.0 and P4.1	V_{OL_VDDIOH}	V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] fixed at 00, I_{OL} = 8mA			0.2	0.4	V
Output Low Voltage for All GPIO Except for P1.[11:21]	V_{OL_VDDIOH}	P1.[11:21] can only use V_{DDIO} as I/O supply and cannot use V_{DDIOH} as I/O supply	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
			V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
			V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
			V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}					48	mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage for All GPIO Except P4.0 and P4.1	V_{OH_VDDIO}	P4.0 and P4.1 can only use V_{DDIOH} as I/O supply and cannot use V_{DDIO} as I/O supply	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OH} = -1mA	V_{DDIO} - 0.4			V
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OH} = -2mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OH} = -4mA	V_{DDIO} - 0.4			
			V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OH} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO Except P4.0 and P4.1	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OH} = -1mA		V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OH} = -2mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OH} = -8mA		V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OH} = -8mA		V_{DDIOH} - 0.4			
Output High Voltage for P4.0 and P4.1	V_{OH_VDDIOH}	V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] fixed at 00, I_{OH} = -1mA		V_{DDIOH} - 0.4			V
Combined I_{OH}, All GPIO	I_{OH_TOTAL}					-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}				300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pull-up disabled		-100		+100	nA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pull-down disabled	-800		+800	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pull-up/Pull-down Resistor for All GPIO and RSTN	R_{PU1}	Normal resistance		25		kΩ
	R_{PU2}	Highest resistance		1		MΩ
RSTN Assertion Time	t_{RSTN}	Device in ACTIVE mode, RSTN device pin assertion duration to entry into device reset state.		6 x t_{SYS_CLK}		µs
BLUETOOTH RADIO / POWER						
Bluetooth LDO Input Voltage	$V_{BLE\_LDO\_IN}$	GCR_BTLELDOCTRL.ldotxbyp = 0	1.1	1.2	1.89	V
		GCR_BTLELDOCTRL.ldotxbyp = 1; input supply ripple < 0.3mV_{P-P}	1.1	1.2	1.21	
BLUETOOTH RADIO / FREQUENCY						
Operating Frequency		1MHz channel spacing	2360		2500	MHz
PLL Programming Resolution	PLL_{RES}			1		MHz
Frequency Deviation at 1Mbps	Δf_{1MHz}			±170		kHz
Frequency Deviation at Bluetooth LE 1Mbps	$\Delta f_{BLE1MHz}$			±250		kHz
Frequency Deviation at 2Mbps	Δf_{2MHz}			±320		kHz
Frequency Deviation at Bluetooth LE 2Mbps	$\Delta f_{BLE2MHz}$			±500		kHz
BLUETOOTH RADIO / CURRENT CONSUMPTION (IPO enabled, f_{SYS_CLK} = 120MHz, Bluetooth LE stack running on CM4. Measured at the V_{CORE} device pin at 1.1V, measured at the BLE_LDO_IN device pin at 1.2V, RV32 is disabled)						
Tx Run Current	I_{CORE}			9.08		mA
	$I_{BLE\_LDO\_IN\_+4.5DBM}$	P_{RF} = +4.5dBm		11.5		
	$I_{BLE\_LDO\_IN\_0DBM}$	P_{RF} = 0dBm		7.0		
	$I_{BLE\_LDO\_IN\_-10DBM}$	P_{RF} = -10dBm		4.7		
Tx Idle Current	$I_{CORE\_IDLE\_TX}$	Digital baseband idle channel		8.6		mA
	$I_{BLE\_LDO\_IN\_IDLE\_TX}$	Digital baseband idle channel		0.07		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BLUETOOTH RADIO / CURRENT CONSUMPTION (IPO enabled, f_{SYS_CLK} = 120MHz, Bluetooth LE stack running on CM4. Measured at the V_{CORE} device pin at 1.1V, measured at the BLE_LDO_IN device pin at 1.2V, RV32 is disabled)							
Rx Run Current	I_{CORE_1M}	f_{RX} = 1Mbps			10.2		mA
	$I_{BLE\_LDO\_IN\_1M}$	f_{RX} = 1Mbps			4.8		
	I_{CORE_2M}	f_{RX} = 2Mbps			10.8		
	$I_{BLE\_LDO\_IN\_2M}$	f_{RX} = 2Mbps			4.8		
Rx Idle Current	$I_{CORE\_IDLE\_RX}$	Digital baseband idle channel			8.6		mA
	$I_{BLE\_LDO\_IN\_IDLE\_RX}$	Digital baseband idle channel			0.07		µA
BLUETOOTH RADIO / TRANSMITTER							
Maximum Output Power	P_{RF}				+4.5		dBm
RF Power Accuracy	P_{RF_ACC}				±1		dB
First Adjacent Channel Transmit Power ±2MHz	P_{RF1_1}	2Mbps Bluetooth LE			-39.2		dBc
First Adjacent Channel Transmit Power ±4MHz	P_{RF2_1}	2Mbps Bluetooth LE			-52.7		dBc
BLUETOOTH RADIO / RECEIVER (Refer to the Bluetooth 5.2 test specification for adjacent interference and intermodulation test methodology.)							
Maximum Received Signal Strength at < 0.1% PER	P_{RX_MAX}				0		dBm
Receiver Sensitivity, Ideal Transmitter	P_{SENS_IT}	Measured with 37-byte payload	1Mbps Bluetooth LE		-97		dBm
			2Mbps Bluetooth LE		-94		
Receiver Sensitivity, Dirty Transmitter	P_{SENS_DT}	Measured with 37-byte payload	1Mbps Bluetooth LE		-96		dBm
			2Mbps Bluetooth LE		-93.2		
Receiver Sensitivity, Long Range Coded	P_{SENS_LR}	Measured with 37-byte payload	125kbps Bluetooth LE		-104.2		dBm
			500kbps Bluetooth LE		-101		
C/I Co-Channel	C/I_{1MHz}	1Mbps Bluetooth LE			8.5		dB
	C/I_{2Mhz}	2Mbps Bluetooth LE			8.6		
	C/I_{S2}	Coded mode at 125kbps			2.6		
	C/I_{S8}	Coded mode at 500kbps			3.8		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Adjacent Interference	C/I_{+1_1}	+1MHz offset, 1Mbps Bluetooth LE		2.1		dB
	C/I_{-1_1}	-1MHz offset, 1Mbps Bluetooth LE		-2.8		
	C/I_{+2_1}	+2MHz offset, 1Mbps Bluetooth LE		-29.6		
	C/I_{-2_1}	-2MHz offset, 1Mbps Bluetooth LE		-33.7		
	C/I_{+2_2}	+2MHz offset, 2Mbps Bluetooth LE		3		
	C/I_{-2_2}	-2MHz offset, 2Mbps Bluetooth LE		2		
	C/I_{+4_2}	+4MHz offset, 2Mbps Bluetooth LE		-21		
	C/I_{-4_2}	-4MHz offset, 2Mbps Bluetooth LE		-23		
Adjacent Interference, (3+n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{3+MHZ}	1Mbps Bluetooth LE		-34.3		dB
Adjacent Interference, (6+2n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{6+MHZ}	2Mbps Bluetooth LE		-32.9		dB
Intermodulation Performance, 1Mbps Bluetooth LE with 3MHz, 4MHz, 5MHz Offset	P_{IMD_1MBPS}	1Mbps Bluetooth LE		-37.2		dBm
Intermodulation Performance, 2Mbps Bluetooth LE with 6MHz, 8MHz, 10MHz Offset	P_{IMD_2MBPS}	2Mbps Bluetooth LE		-37.8		dBm
Received Signal Strength Indicator Accuracy	$RSSI_{ACC}$			±3		dB
Received Signal Strength Indicator Range	$RSSI_{RANGE}$			-98 to -15		dBm
12-BIT SAR ADC						
V_{DD3A} Idle Current	I_{VDD3A}	ADC_CTRL0.*resetb* = 0, ADC_CTRL0.*bias_en* = 0, ADC_CTRL0.*adc_en* = 0, input buffer disabled		2.1		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD3A} ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, ADC clock = 25MHz	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 0, V_{DD3A} = 3.3V		283		µA
			MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 1, V_{DD3A} = 3.3V		339		
		ADC active, reference buffer enabled, ADC clock = 16MHz	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 0, V_{DD3A} = 3.3V		216		
			MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 1, V_{DD3A} = 3.3V		271		
12-BIT SAR ADC / Input Buffer Enabled (FCR_SARBUFCN.thru_pad_sw_enx = 1; FCR_SARBUFCN.thru_en = 1; FCR_SARBUFCN.amp_en = 1)							
Resolution					12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.*clkdiv* = 0b000; AINx input pk-pk = V_{REF} - 10mV			10		bits
External Reference Voltage	V_{REF}	$V_{REF} \le V_{DD3A}$		2.048		V_{DD3A}	V
Internal Reference Voltage	V_{INT_REF}	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 0			1.25		V
	V_{INT_REF}	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 1			2.048		
ADC Clock Rate Maximum	f_{ACLK}					25	MHz
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DATA.*chan* = [7:0]	FCR_SARBUFCN.*divsel* = 0b00	V_{SSA} + 0.05		MIN (V_{REF}, V_{DDIOH})	V
			FCR_SARBUFCN.*divsel* = 0b01	V_{SSA} + 0.05		MIN (V_{REF}, V_{DDIOH})	
			FCR_SARBUFCN.*divsel* = 0b10	V_{SSA} + 0.05		MIN (2 x V_{REF}, V_{DDIOH})	
			FCR_SARBUFCN.*divsel* = 0b11	V_{SSA} + 0.05		MIN (3 x V_{REF}, V_{DDIOH})	
ADC Buffer Current	$I_{ADCBUFFER}$	FCR_SARBUFCN = 0b11, input voltage = 1.1V			67.7		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	R_{AIN}	Input impedance is leakage only when the input buffer is enabled.		100		MΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		2		pF
Integral Nonlinearity	INL			±4		LSb
Differential Nonlinearity	DNL			±0.75		LSb
Offset Error	V_{OS}	Chopping enabled		±0.25		LSb
ADC Input Buffer Offset	V_{OS}			±1.5		LSb
ADC Sample Rate	f_{ADC}	Bandwidth limited by the input buffer			25	kHz
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			500	µs
ADC Input Leakage	I_{ADC_LEAK}			±1.2		nA
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		±45		ppm
12-BIT SAR ADC / Input Buffer Disabled (FCR_SARBUFCN.thru_pad_sw_enx = 0; FCR_SARBUFCN.thru_en = 0; FCR_SARBUFCN.amp_en = 0)						
Resolution				12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.*clkdiv* = 0b000; AINx input pk-pk = V_{REF} - 10mV		10		bits
External Reference Voltage	V_{REF}	$V_{REF} \le V_{DD3A}$	2.048		V_{DD3A}	V
Internal Reference Voltage	V_{INT_REF}	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 0		1.25		V
	V_{INT_REF}	MCR_ADCCFG0.*ext_ref* = 0, MCR_ADCCFG0.*ref_sel* = 1		2.048		
ADC Clock Rate Maximum	f_{ADCCLK}				25	MHz
Input Voltage Range	V_{AIN}	AIN[7:0], ADC_DATA.*chan* = [7:0] / FCR_SARBUFCN.*divsel* = 0b00	V_{SSA} + 0.05		V_{REF}	V
Input Impedance	R_{AIN}			1.2		MΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		2		pF
		Dynamically switched capacitance		1.2		pF
Integral Nonlinearity	INL			±1.5		LSb
Differential Nonlinearity	DNL			±0.75		LSb
Offset Error	V_{OS}	Chopping enabled		±0.25		LSb
ADC Sample Rate	f_{ADC}				1	Msps
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			500	µs
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected		±1.2		nA
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		±45		ppm

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATORS						
Input Offset Voltage	V_{OFFSET}			±1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00		±23		mV
		AINCOMPHYST[1:0] = 01		±50		
		AINCOMPHYST[1:0] = 10		±2		
		AINCOMPHYST[1:0] = 11		±7		
Input Voltage Range	V_{IN_CMP}	Common-mode range	0.6		1.35	V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}			42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +105°C	10			years
Current Consumption During Flash Programming	I_{PROG}	Current required for flash write/erase, V_{DD}		6.5		mA
USB						
USB Transceiver Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
Pin Capacitance (DP, DM)	C_{IN_USB}	Pin to V_{SSB}		8		pF
Driver Output Resistance	R_{DRV}	Steady-state drive		44 ±10%		Ω
USB / FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.1			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.5	V
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5kΩ from DP and DM to V_{SSB}, I_{OH} = -4mA	2.8		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.3	V
Differential Input Sensitivity	V_{DI}	|DP to DM|; system requirement, not tested	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range; system requirement, not tested	0.8		2.5	V
Transition Time (Rise/Fall) DP, DM	t_{RF}	C_L = 50pF	4		20	ns
Pull-up Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB / HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low-Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High-Level Output Voltage	V_{HSOH}			400 ±40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ±200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ±200		mV

Electrical Characteristics—I^2C

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs

Electrical Characteristics—I²C (continued)

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST-MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns

Electrical Characteristics—I²C (continued)

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—I²S

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TARGET						
Bit Clock Frequency	f_{BCLKS}				25	MHz
Bit Clock Period	t_{BCLKS}		$\frac{1}{f_{BCLKS}}$			µs
BCLK High Time	$t_{WBCLKHS}$			$0.5 \times \frac{1}{f_{BCLKS}}$		µs
BCLK Low Time	$t_{WBCLKLS}$			$0.5 \times \frac{1}{f_{BCLKS}}$		µs
Setup Time for LRCLK	t_{LRCLK_BLCKS}			20		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOS}			20		ns
Setup Time for SD (Input)	t_{SU_SDIS}			10		ns
Hold Time SD (Input)	t_{HD_SDIS}			10		ns
CONTROLLER						
Bit Clock Frequency	f_{BCLKM}	Source only from I2S0B_CLKEXT (P0.23 Alternate Function 2)			80	MHz
Bit Clock Period	t_{BCLKM}		$\frac{1}{f_{BCLKM}}$			µs
BCLK High Time	$t_{WBCLKHM}$			$0.5 \times \frac{1}{f_{BCLKM}}$		µs
BCLK Low Time	$t_{WBCLKLM}$			$0.5 \times \frac{1}{f_{BCLKM}}$		µs
Delay Time BCLK to LRCLK Valid	t_{BLCK_LRCLKM}			20		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOM}			20		ns
Setup Time for SD (Input)	t_{SU_SDIM}			10		ns

Electrical Characteristics—I²S (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time SD (Input)	t_{HD_SDIM}			10		ns

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER MODE						
SPI Controller Operating Frequency (SPI0, SPI1, SPI2)	f_{MCK}	f_{SYS_CLK} = 120MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/4$			30	MHz
SPI Controller Operating Frequency (SPI3, SPI4)	f_{MCK}	f_{SYS_CLK} = 120MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/2$			60	MHz
SPI Controller SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
TARGET MODE						
SPI Target Operating Frequency	f_{SCK}				60	MHz
SPI Target SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		ns
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—HyperBus

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HYP_CLK, HYP_CLKN Frequency	f_{HYP_CLK}				60	MHz
HYP_CLK, HYP_CLKN Period	t_{HYP_CLK}		$1/f_{HYP\_CLK}$			ns
HYP_CLK, HYP_CLKN High Time	t_{WHCKH}			7		ns
HYP_CLK, HYP_CLKN Low Time	t_{WHCKL}			7		ns
CS Setup to RWDS	t_{CSSU}			6		ns
RWDS Setup to CK	t_{RWDS_CK}			10		ns
Dx Output Setup	t_{OSU}			5		ns
Dx Output Hold	t_{OH}			3		ns
CS Hold after CK Falling Edge	t_{CSH}			5		ns
CS High between Transactions	t_{CHSI}			15		ns
Dx Input Setup to RWDS	t_{ISU}			4		ns
Dx Input Hold	t_{IHD}			2		ns

Electrical Characteristics—1-Wire Controller

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		

Electrical Characteristics—1-Wire Controller (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

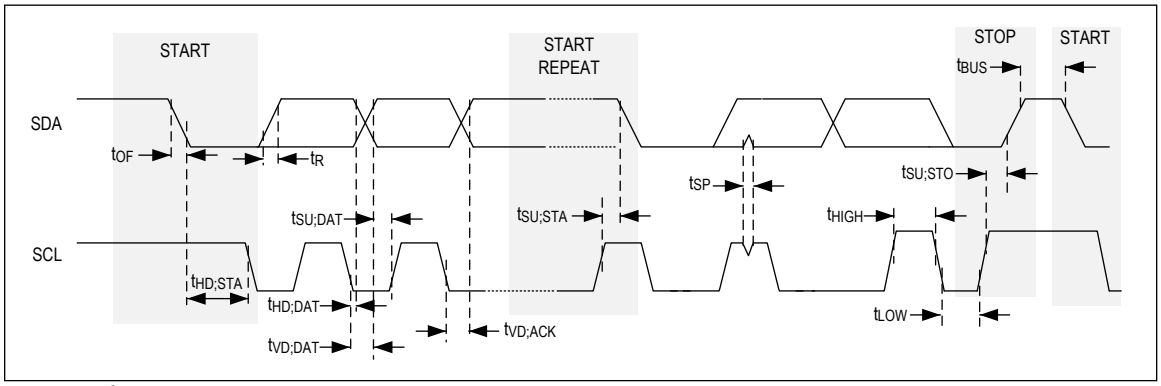


Figure 1. I²C Timing Diagram

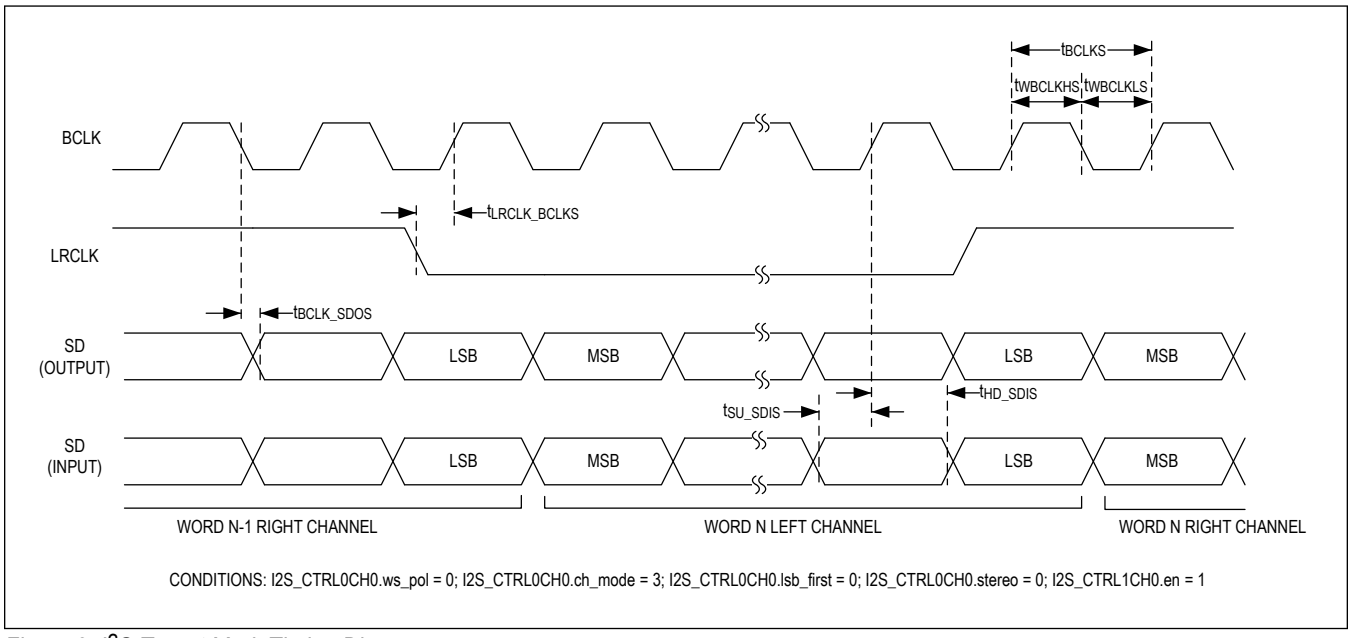


Figure 2. I²S Target ModeTiming Diagram

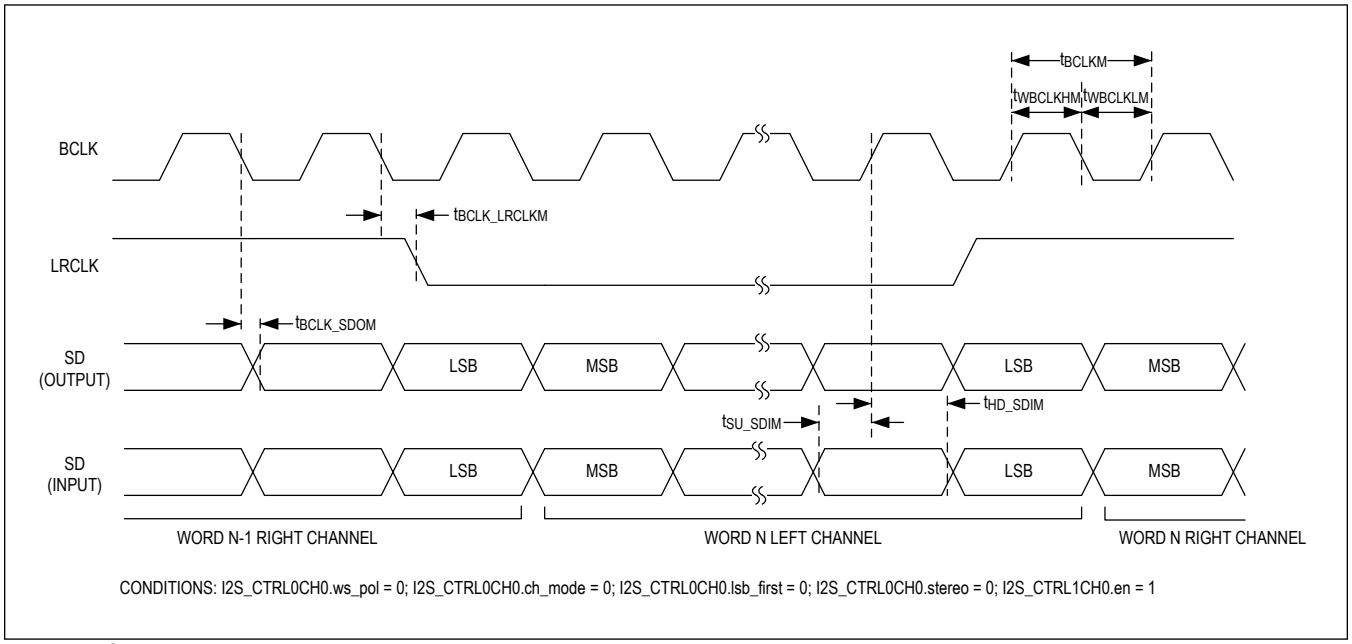


Figure 3. I²S Controller Timing Diagram

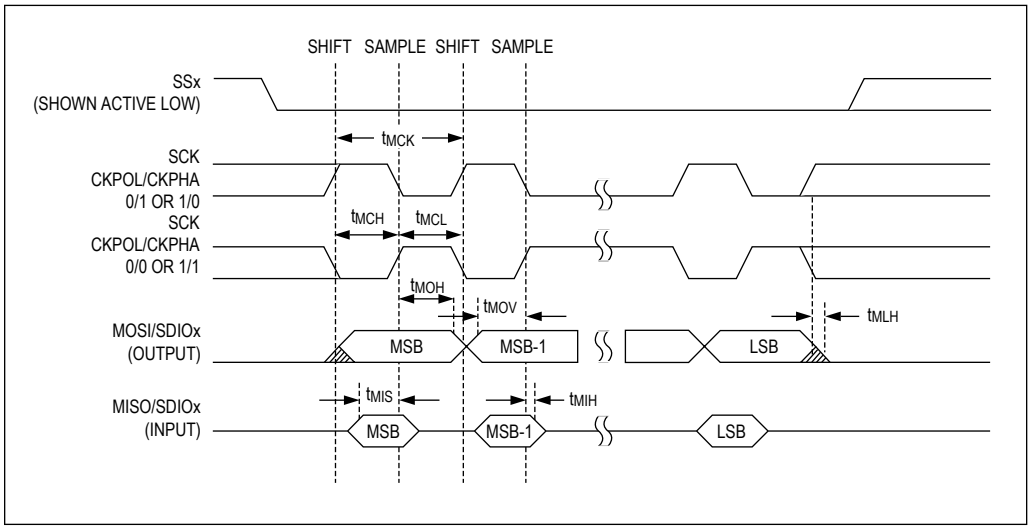


Figure 4. SPI Controller Mode Timing Diagram

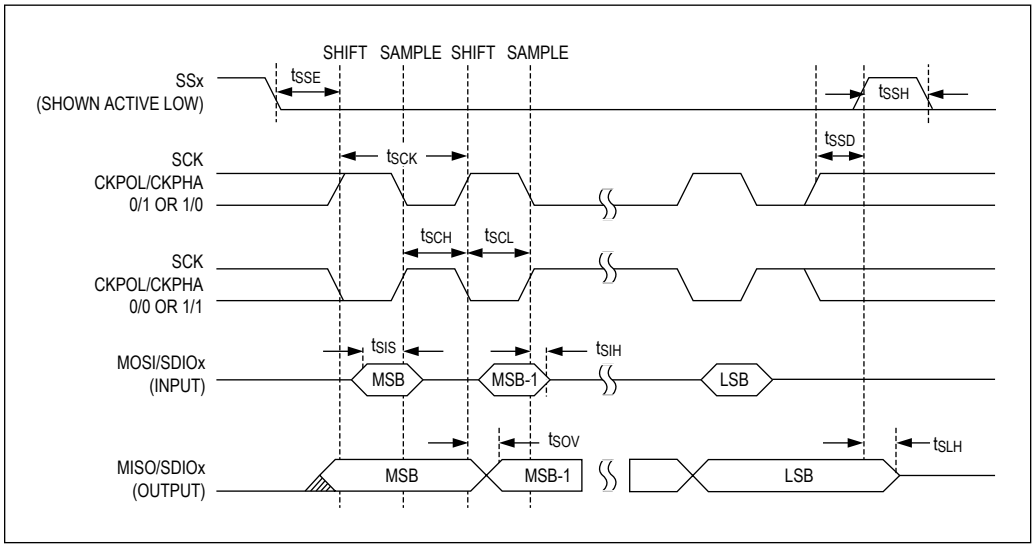


Figure 5. SPI Target Mode Timing Diagram

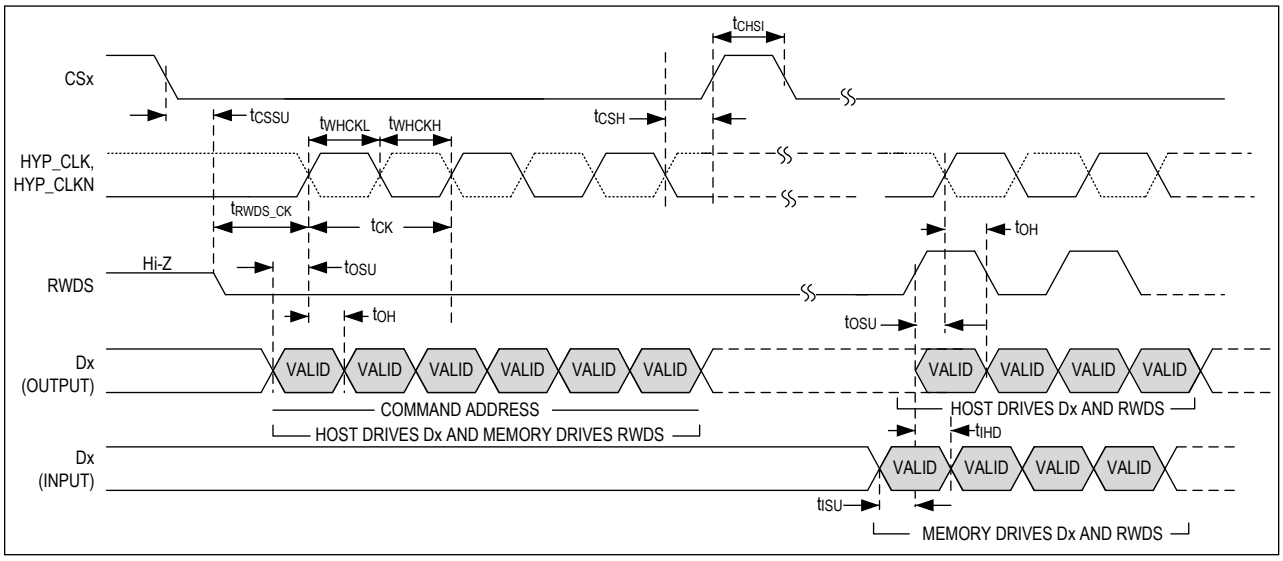


Figure 6. HyperBus/Xccela Bus Timing Diagram

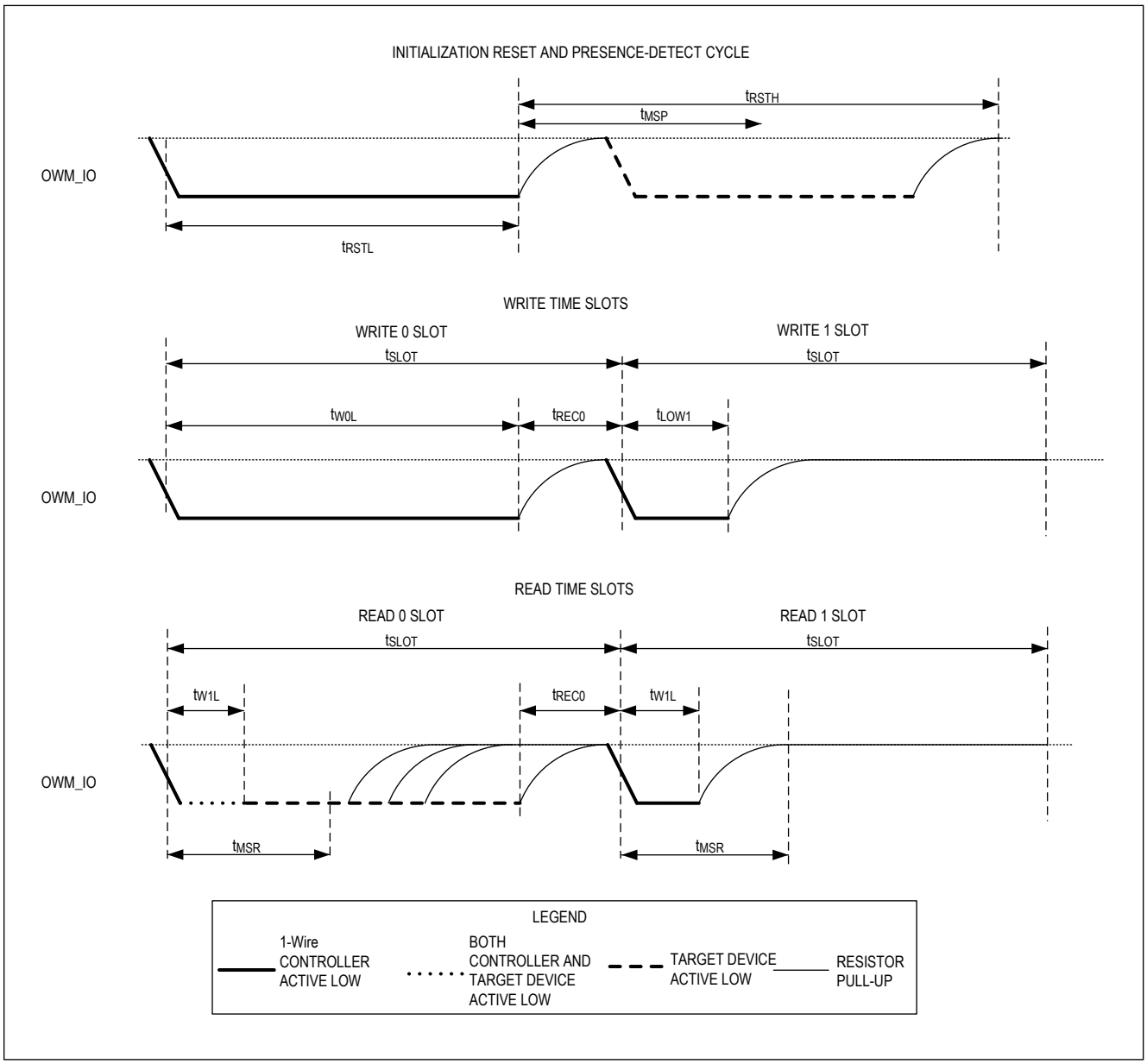
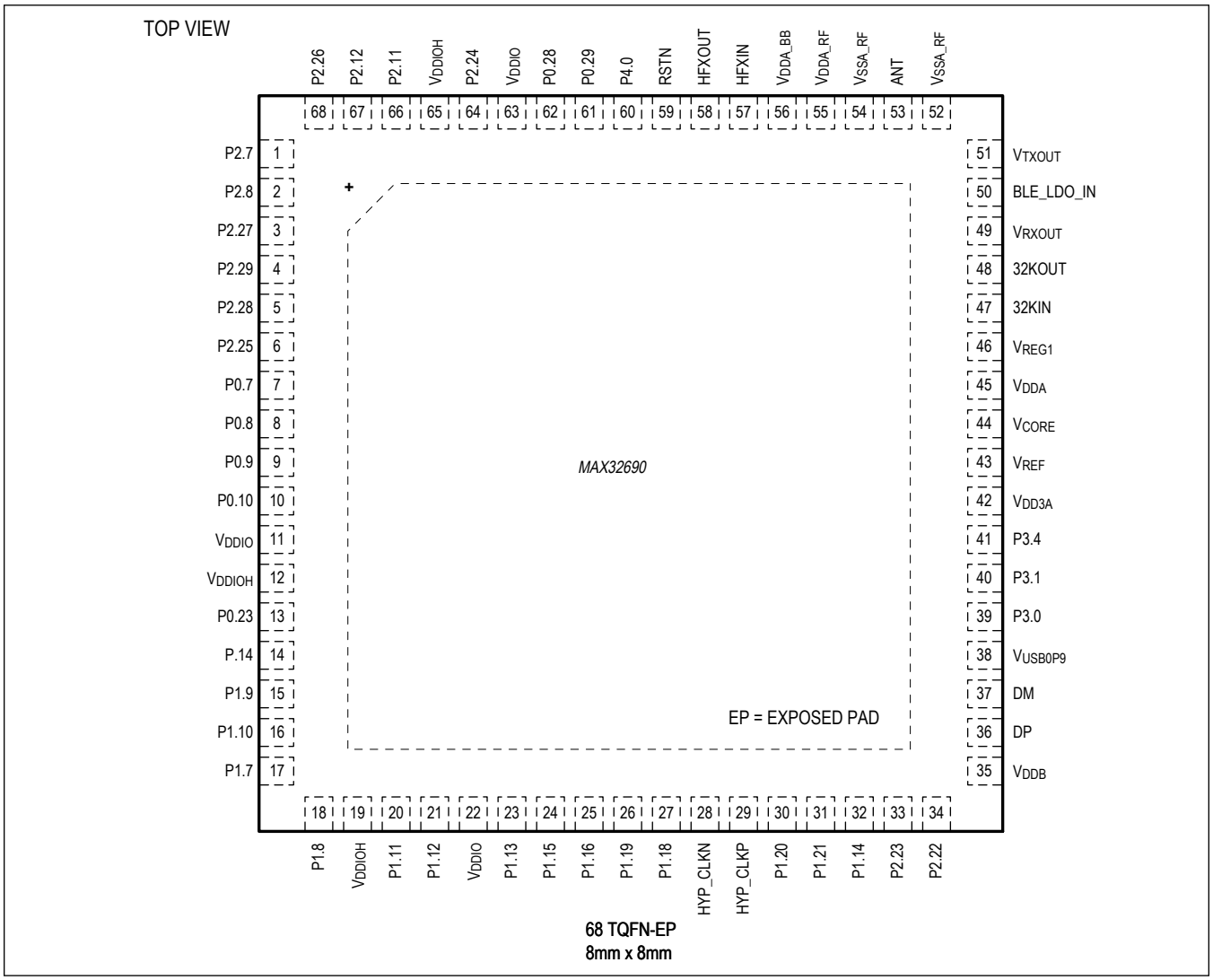


Figure 7. 1-Wire Controller Data Timing Diagram

Pin Configuration

68 TQFN-EP



Pin Description

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
POWER AND SYSTEM PINS (See *Bypass Capacitor Recommendations*)						
44	V_{CORE}	—	—	—	—	Digital Supply Voltage. Bypass with 1.0µF to V_{SS}.

68 TQFN-EP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
46	V_{REG1}	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
11, 22, 63	V_{DDIO}	—	—	—	—	GPIO Supply Voltage. This pin must always be connected to the V_{DDA} device pin at the PCB level. Bypass with 1.0µF to V_{SS}.
12, 19, 65	V_{DDIOH}	—	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass with 1.0µF to V_{SS}. This pin must be connected to the V_{DD3A} device pin at the PCB level.
EP	V_{SS}	—	—	—	—	Digital Ground. Exposed Pad (TQFN only). Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
43	V_{REF}	—	—	—	—	ADC External Reference Input. This is the reference input for the analog-to-digital converter (ADC). Bypass with 1.0µF to V_{SS}.
42	V_{DD3A}	—	—	—	—	Analog Supply Voltage. Bypass with 1.0µF to V_{SS}. This pin must be connected to the V_{DDIOH} device pin at the PCB level.
45	V_{DDA}	—	—	—	—	Analog Supply Voltage. Bypass with 1.0µF to V_{SS}. This pin must always be connected to the V_{DDIO} device pin at the PCB level.
50	BLE_LDO_IN	—	—	—	—	LDO Input for Bluetooth and the ERFO. Bypass with 100nF and 1µF to V_{SS}. This pin must be connected to use either Bluetooth or the ERFO.
56	V_{DDA_BB}	—	—	—	—	0.9V Analog Power Supply for the Bluetooth Analog Baseband. Bypass with 100nF and 1µF to V_{SS}.
55	V_{DDA_RF}	—	—	—	—	0.9V Analog Power Supply for the Bluetooth Radio. Bypass with 100nF and 1µF to V_{SS}.
49	V_{RXOUT}	—	—	—	—	Radio Baseband Supply Voltage Output. Bypass with 1.0µF to V_{SS}. This pin must always be connected to the V_{DDA_BB} device pin at the PCB level.
51	V_{TXOUT}	—	—	—	—	Radio RF Supply Voltage Output. Bypass with 1.0µF to V_{SS}. This pin must always be connected to the V_{DDA_RF} device pin at the PCB level.
54, 52	V_{SSA_RF}	—	—	—	—	Bluetooth Radio Ground
35	V_{DDB}	—	—	—	—	USB Transceiver Supply Voltage Input. See *USB Design Considerations*.

68 TQFN-EP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
38	V_{USB0P9}	—	—	—	—	Bypass with 1.0µF to V_{SS}. Do not connect this device pin to any other external circuitry.
59	RSTN	—	—	—	—	Active-Low. External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a system reset and begins execution at the first instruction. This pin has an internal pull-up to the V_{DDIO} supply.
CLOCK PINS						
48	32KOUT	—	—	—	—	32kHz Crystal Oscillator Output.
47	32KIN	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
57	HFXIN	—	—	—	—	RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square-wave source. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32690 User Guide* for determination of the required external stability capacitors.
58	HFXOUT	—	—	—	—	RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32690 User Guide* for determination of the required external stability capacitors.
28	HYP_CLKN	—	—	—	—	HyperBus Negative Clock
29	HYP_CLKP	—	—	—	—	HyperBus Positive Clock
GPIO AND ALTERNATE FUNCTION						
7	P0.7	P0.7	OWM_PE	TMR1B_IOA	—	1-Wire Controller Pull-up Enable; Timer1 Port Map B Input/Output 32-Bits or Lower 16-Bits Only
8	P0.8	P0.8	OWM_IO	TMR1B_IOB	—	1-Wire Controller Data; Timer1 Port Map B Input/Output Upper 16-Bits Only
9	P0.9	P0.9	ADC_CLK_EXT	—	TMR0C_IOAN	ADC External Clock Input; Timer0 Port Map C Input/Output 32-Bits or Lower 16-Bits Only Inverted Output

68 TQFN-EP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
10	P0.10	P0.10	ADC_TRIG_A	—	TMR0C_IOBN	ADC Trigger Input; Timer0 Port Map C Input/Output Upper 16-Bits Only Inverted Output
14	P0.14	P0.14	—	TMR0B_IOB	I2C2C_SCL	Timer0 Port Map B Input/Output Upper 16-Bits Only; I2C2 Port Map C Serial Clock
13	P0.23	P0.23/ CLKEXT	PT15	I2S0B_CLKEXT	—	Pulse Train 15; I2S0 Port Map B External Clock Input. This device pin can also be configured as an input to provide a clock source for the SYS_CLK.
62	P0.28	P0.28/ SWDIO	—	—	—	Single-Wire Debug I/O. After reset, this device pin performs as the single-wire debug I/O when selected.
61	P0.29	P0.29/ SWDCLK	—	—	—	Single-Wire Debug Clock. After reset, this device pin performs as the single-wire debug clock when selected.
17	P1.7	P1.7	UART2A_CTS	PT1	I2C2C_SDA	UART2 Port Map A Clear to Send; Pulse Train 1; I2C2 Port Map C Serial Data
18	P1.8	P1.8	UART2A_RTS	PT2	I2C2C_SCL	UART2 Port Map A Request to Send; Pulse Train 2; I2C2 Port Map C Serial Clock
15	P1.9	P1.9	UART2A_RX	PT3	—	UART2 Port Map A Receive; Pulse Train 3
16	P1.10	P1.10	UART2A_TX	PT4	—	UART2 Port Map A Transmit; Pulse Train 4
20	P1.11	P1.11	—	—	HYP_CS0N	HyperBus Chip Select 0 Active Low
21	P1.12	P1.12	PT5	HYP_D0	—	Pulse Train 5; Hyperbus Data 0
23	P1.13	P1.13	TMR3A_IOA	—	HYP_D4	Timer3 Port Map A Input/Output 32-Bits or Lower 16-Bits; HyperBus Data 4
32	P1.14	P1.14	TMR3A_IOB	—	HYP_RWDS	Timer3 Port Map A Input/Output Upper 16-Bits Only; HyperBus Read/Write Data Strobe
24	P1.15	P1.15	—	—	HYP_D1	HyperBus Data 1
25	P1.16	P1.16	—	—	HYP_D5	HyperBus Data 5
27	P1.18	P1.18	—	PT6	HYP_D6	Pulse Train 6; HyperBus Data 6
26	P1.19	P1.19	—	PT7	HYP_D2	Pulse Train 7; HyperBus Data 2
30	P1.20	P1.20	—	—	HYP_D3	HyperBus Data 3
31	P1.21	P1.21	—	PT8	HYP_D7	Pulse Train 8; HyperBus Data 7
1	P2.7	P2.7	I2C0A_SDA	—	—	I2C0 Port Map A Serial Data
2	P2.8	P2.8	I2C0A_SCL	—	—	I2C0 Port Map A Serial Clock
66	P2.11	P2.11	UART0A_RX	PT13	—	UART0 Port Map A Receive; Pulse Train 13
67	P2.12	P2.12	UART0A_TX	PT15	—	UART0 Port Map A Transmit; Pulse Train 15

68 TQFN-EP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
34	P2.22	P2.22	PT8	CAN0B_RX	—	Pulse Train 8; Controller Area Network 0 Port Map B Receive Input
33	P2.23	P2.23	PT6	CAN0B_TX	—	Pulse Train 6; Controller Area Network 0 Port Map B Transmit Output
64	P2.24	P2.24	PT10	CAN1B_RX	—	Pulse Train 10; Controller Area Network 1 Port Map B Receive Input
6	P2.25	P2.25	PT11	CAN1B_TX	—	Pulse Train 11; Controller Area Network 1 Port Map B Transmit Output
68	P2.26	P2.26	PT12	SPI0B_SS1	I2S0C_WS	Pulse Train 12; SPIO Port Map B Target Select 1; I2S0 Port Map C Left/Right Word Select
3	P2.27	P2.27	PT13	SPI0B_MISO	I2S0C_SDI	Pulse Train 13; SPI0 Port Map B Controller In Target Out/Data 1; I2S0 Port Map C Serial Data In
5	P2.28	P2.28	PT14	SPI0B_MOSI	I2S0C_SDO	Pulse Train 14; SPI0 Port Map B Controller Out Target In/Data 0; I2S0 Port Map C Serial Data Out
4	P2.29	P2.29	PT0	SPI0B_SCK	I2S0C_SCK	Pulse Train 0; SPI0 Port Map B Serial Clock; I2S0 Port Map C Serial Clock
39	P3.0	P3.0	AIN0/AIN0N	LPUART0B_RX	—	ADC Input 0/Comparator 0 Negative Input; Low-Power UART0 Port Map B Receive
40	P3.1	P3.1	AIN1/AIN0P	LPUART0B_TX	—	ADC Input 1/Comparator 0 Positive Input; Low-Power UART0 Port Map B Transmit
41	P3.4	P3.4	AIN4/AIN2N	LPTMR0B_IOA	—	ADC Input 4/Comparator 2 Negative Input; Low-Power Timer0 Port Map B Input/Output 32-Bits or Lower 16-Bits
60	P4.0	P4.0/PDOWN	—	—	—	Power-Down Output
USB						
36	DP	—	—	—	—	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See *USB Design Considerations*.
37	DM	—	—	—	—	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See *USB Design Considerations*.
ANTENNA OUTPUT						
53	ANT	—	—	—	—	Antenna for Bluetooth Radio. Attach the single-ended, unbalanced Bluetooth radio antenna.

Pin Configuration

140 WLP

Pin Description

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
POWER AND SYSTEM PINS (See *Bypass Capacitor Recommendations*)						
H12	V_{CORE}	—	—	—	—	Digital Supply Voltage. Bypass with 1.0µF to V_{SS}.
J12	V_{REG1}	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
A6, D10, E1, M4	V_{DDIO}	—	—	—	—	GPIO Supply Voltage. Bypass with 1.0µF to V_{SS}. This pin must always be connected to the V_{DDA} device pin at the PCB level.
A4, D1, D12, M3	V_{DDIOH}	—	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass with 1.0µF to V_{SS}. This pin must be connected to the V_{DD3A} device pin at the PCB level.
A8, F1, H11, M8	V_{SS}	—	—	—	—	Digital Ground
G12	V_{REF}	—	—	—	—	ADC External Reference Input. This is the reference input for the analog-to-digital converter. Bypass with 1.0µF to V_{SS}.
F11	V_{DD3A}	—	—	—	—	Analog Supply Voltage. Bypass with 1.0µF to V_{SSA}. This pin must be connected to the V_{DDIOH} device pin.
J11	V_{DDA}	—	—	—	—	Analog Supply Voltage. Bypass with 1.0µF to V_{SSA}. This pin must always be connected to the V_{DDIO} device pin at the PCB level.
G11	V_{SSA}	—	—	—	—	Analog Ground
K12	BLE_LDO_IN	—	—	—	—	LDO Input for Bluetooth and the ERFO. Bypass with 100nF and 1µF to V_{SS}. This pin must be connected to use either Bluetooth or the ERFO.
M10	V_{DDA_BB}	—	—	—	—	0.9V Analog Power Supply for the Bluetooth Analog Baseband. Bypass with 100nF and 1µF to V_{SS}.
L10	V_{DDA_RF}	—	—	—	—	0.9V Analog Power Supply for the Bluetooth Radio. Bypass with 100nF and 1µF to V_{SS}.
—	V_{RXOUT}	—	—	—	—	Radio Baseband Supply Voltage Output. This signal is internally connected to V_{DDA_BB}.
—	V_{TXOUT}	—	—	—	—	Radio RF Supply Voltage Output. This signal is internally connected to the V_{DDA_RF} device pin.
M11	V_{SSA_BB}	—	—	—	—	Bluetooth Baseband Ground

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
L11	V_{SSA_RF}	—	—	—	—	Bluetooth Radio Ground
B11	V_{DDB}	—	—	—	—	USB Transceiver Supply Voltage. Bypass with 1.0µF to V_{SSB}.
D11	V_{USB0P9}	—	—	—	—	Bypass with 1.0µF to V_{SSB}. Do not connect this device pin to any other external circuitry.
C11	V_{SSB}	—	—	—	—	USB Transceiver Ground. Connect to V_{SS}.
K9	RSTN	—	—	—	—	Active-Low. External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a system reset and begins execution at the first instruction. This pin has an internal pull-up to the V_{DDIO} supply.
CLOCK PINS						
K11	32KOUT	—	—	—	—	32kHz Crystal Oscillator Output.
K10	32KIN	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
L9	HFXIN	—	—	—	—	RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square-wave source. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32690 User Guide* for determination of the required external stability capacitors.
M9	HFXOUT	—	—	—	—	RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32690 User Guide* for determination of the required external stability capacitors.
A10	HYP_CLKP	—	—	—	—	HyperBus Positive Clock
A9	HYP_CLKN	—	—	—	—	HyperBus Negative Clock
GPIO AND ALTERNATE FUNCTION						
J2	P0.1	P0.1	SPIXR_SDIO0	SPIXF_SDIO0	UART2C_TX	SPI External RAM Data 0; SPI External Flash Data 0; UART2 Port Map C Transmit

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
J3	P0.2	P0.2	SPIXR_SDIO2	SPIXF_SDIO2	UART2C_CTS	SPI External RAM Data 2; SPI External Flash Data 2; UART2 Port Map C Clear to Send
J1	P0.3	P0.3	SPIXR_SCK	SPIXF_SCK	UART2C_RTS	SPI External RAM Serial Clock; SPI External Flash Serial Clock; UART2 Port Map C Request to Send
H3	P0.4	P0.4	SPIXR_SDIO3	SPIXF_SDIO3	TMR0C_IOA	SPI External RAM Data 3; SPI External Flash Data 3; Timer0 Port Map C Input/Output 32-Bits or Lower 16-Bits
H2	P0.5	P0.5	SPIXR_SDIO1	SPIXF_SDIO1	TMR2C_IOB	SPI External RAM Data 1; SPI External Flash Data 1; Timer2 Port Map C Input/Output Upper 16-Bits Only
H1	P0.6	P0.6	SPIXR_SS0	SPIXF_SS0	UART2C_RX	SPI External RAM Target Select 0; SPI External Flash Target Select 0; UART2 Port Map C Receive
G2	P0.7	P0.7	OWM_PE	TMR1B_IOA	—	1-Wire Controller Pull-up Enable; Timer1 Port Map B Input/Output 32-Bits or Lower 16-Bits Only
G1	P0.8	P0.8	OWM_IO	TMR1B_IOB	—	1-Wire Controller Data; Timer1 Port Map B Input/Output Upper 16-Bits Only
G7	P0.9	P0.9	ADC_CLK_EXT	—	TMR0C_IOAN	ADC External Clock Input; Timer0 Port Map C Input/Output 32-Bits or Lower 16-Bits Only Inverted Output
F7	P0.10	P0.10	ADC_TRIG_A	—	TMR0C_IOBN	ADC Trigger Input; Timer0 Port Map C Input/Output Upper 16-Bits Only Inverted Output
F2	P0.11	P0.11	I2C1A_SDA	—	TMR1C_IOAN	I2C1 Port Map A Serial Data; Timer1 Port Map C Input/Output 32-Bits or Lower 16-Bits Only Inverted Output
F3	P0.12	P0.12	I2C1A_SCL	—	TMR1C_IOBN	I2C1 Port Map A Serial Clock; Timer1 Port Map C Input/Output Upper 16-Bits Only Inverted Output
D2	P0.13	P0.13	SPI3A_SS1	TMR0B_IOA	I2C2C_SDA	SPI3 Port Map A Target Select 1; Timer0 Port Map B Input/Output 32-Bits or Lower 16-Bits Only; I2C2 Port Map C Serial Data
C1	P0.14	P0.14	SPI3A_SS2	TMR0B_IOB	I2C2C_SCL	SPI3 Port Map A Target Select 2; Timer0 Port Map B Input/Output Upper 16-Bits Only; I2C2 Port Map C Serial Clock
C2	P0.15	P0.15	SPI3A_SDIO3	—	TMR1C_IOA	SPI3 Port Map A Data 3; Timer1 Port Map C Input/Output 32 Bits or Lower 16 Bits Only
B3	P0.16	P0.16	SPI3A_SCK	—	—	SPI3 Port Map A Serial Clock
D3	P0.17	P0.17	SPI3A_SDIO2	—	TMR1C_IOB	SPI3 Port Map A Data 2; Timer1 Port Map C Input/Output Upper 16 Bits Only
C6	P0.18	P0.18	—	—	—	

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
A3	P0.19	P0.19	SPI3A_SS0	RV_TCK	—	SPI3 Port Map A Target Select 0; RV32 JTAG Tap Controller Clock Input
C3	P0.20	P0.20	SPI3A_MISO	RV_TMS	—	SPI3 Port Map A Controller In Target Out/ Data 1; RV32 JTAG Tap Controller Mode Select
B2	P0.21	P0.21	SPI3A_MOSI	RV_TDI	—	SPI3 Port Map A Controller Out Target In/ Data 0; RV32 JTAG Tap Controller Data In
K1	P0.22	P0.22	SPI0A_SS0	RV_TDO	—	SPI0 Port Map A Target Select 0; RV32 JTAG Tap Controller Data Out
F4	P0.23	P0.23/ CLKEXT	PT15	I2S0B_CLKEXT	—	Pulse Train 15; I2S0 Port Map B External Clock Input. This device pin can also be configured as an input to provide a clock source for the SYS_CLK.
G4	P0.24	P0.24	RXEV0	I2S0B_SCK	—	CM4 Rx Event Output; I2S0 Port Map B Serial Clock
H4	P0.25	P0.25	TXEVO	I2S0B_SDI	—	CM4 Tx Event Output; I2S0 Port Map B Serial Data Input
F5	P0.26	P0.26	—	I2S0B_SDO	—	I2S0 Port Map B Serial Data Output
G5	P0.27	P0.27/ USBCLKEXT	ERFO_CLK_OUT	I2S0B_WS	—	USB External Clock Input; ERFO Output; I2S0 Port Map B Left/Right Clock
J8	P0.28	P0.28/ SWDIO	—	—	—	Single-Wire Debug I/O. After reset, this device pin performs as the single-wire debug I/O.
H8	P0.29	P0.29/ SWDCLK	—	—	—	Single-Wire Debug Clock. After reset, this device pin performs as the single-wire debug clock.
G6	P0.30	P0.30	I2C0A_SDA	—	—	I2C0 Port Map A Serial Data
F6	P0.31	P0.31	I2C0A_SCL	—	—	I2C0 Port Map A Serial Clock
E5	P1.0	P1.0	SPI4A_SS0	ADC_TRIG_B	—	SPI4 Port Map A Target Select 0; ADC Trigger B
C4	P1.1	P1.1	SPI4A_MOSI	—	—	SPI4 Port Map A Controller Out Target In/ SDIO0
D5	P1.2	P1.2	SPI4A_MISO	—	—	SPI4 Port Map A Controller In Target Out/ SDIO1
C5	P1.3	P1.3	SPI4A_SCK	—	—	SPI4 Port Map A Serial Clock
B4	P1.4	P1.4	SPI4A_SDIO2	TMR2B_IOA	—	SPI4 Port Map A Data 2; Timer2 Port Map B Input/Output 32-Bits or Lower 16-Bits Only
A5	P1.5	P1.5	SPI4A_SDIO3	TMR2B_IOB	—	SPI4 Port Map A Data 3; Timer2 Port Map B Input/Output Upper 16 Bits Only
B5	P1.6	P1.6	SPI4A_SS1	PT0	—	SPI4 Port Map A Target Select 1; Pulse Train 0
D4	P1.7	P1.7	UART2A_CTS	PT1	I2C2C_SDA	UART2 Port Map A Clear to Send; Pulse Train 1; I2C2 Port Map C Serial Data

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
A2	P1.8	P1.8	UART2A_RTS	PT2	I2C2C_SCL	UART2 Port Map A Request to Send; Pulse Train 2; I2C2 Port Map C Serial Clock
B1	P1.9	P1.9	UART2A_RX	PT3	—	UART2 Port Map A Receive; Pulse Train 3
E4	P1.10	P1.10	UART2A_TX	PT4	—	UART2 Port Map A Transmit; Pulse Train 4
B6	P1.11	P1.11	SPI4A_SS2	—	HYP_CS0N	SPI4 Port Map A Target Select 2; HyperBus Chip Select 0 Active Low
C7	P1.12	P1.12	PT5	HYP_D0	—	Pulse Train 5; Hyperbus Data 0
B7	P1.13	P1.13	TMR3A_IOA	—	HYP_D4	Timer 3 Port Map A Input/Output 32-Bits or Lower 16-Bits; Hyperbus Data 4
A11	P1.14	P1.14	TMR3A_IOB	—	HYP_RWDS	Timer 3 Port Map A Input/Output Upper 16-Bits Only; Hyperbus Read/Write Data Strobe
C8	P1.15	P1.15	—	—	HYP_D1	Hyperbus Data 1
B8	P1.16	P1.16	—	—	HYP_D5	Hyperbus Data 5
A7	P1.17	P1.17	PT9	—	HYP_CS1N	Pulse Train 9; Hyperbus Chip Select 1 Active Low
B9	P1.18	P1.18	—	PT6	HYP_D6	Pulse Train 6; Hyperbus Data 6
C9	P1.19	P1.19	—	PT7	HYP_D2	Pulse Train 7; Hyperbus Data 2
C10	P1.20	P1.20	—	—	HYP_D3	Hyperbus Data 3
B10	P1.21	P1.21	—	PT8	HYP_D7	Pulse Train 8; Hyperbus Data 7
K8	P1.23	P1.23	SPI1A_SS0	—	—	SPI1 Port Map A Target Select 0
J7	P1.24	P1.24	SPI1A_SS2	CAN0B_RX	—	SPI1A Port Map A Target Select 2; Controller Area Network 0 Port Map B Receive Input
H7	P1.25	P1.25	SPI1A_SS1	CAN0B_TX	—	SPI1 Port Map A Target Select 1; Controller Area Network 0 Port Map B Transmit Output
L8	P1.26	P1.26	SPI1A_SCK	—	—	SPI1 Port Map A Serial Clock
K7	P1.27	P1.27	SPI2A_SS2	—	—	SPI2 Port Map A Target Select 2
L7	P1.28	P1.28	SPI1A_MISO	CAN1B_RX	—	SPI1 Port Map A Controller In Target Out/ SDIO1; Controller Area Network 1 Port Map B Receive Input
M7	P1.29	P1.29	SPI1A_MOSI	CAN1B_TX	—	SPI1 Port Map A Controller Out Target In/ SDIO0; Controller Area Network 1 Port Map B Transmit Output
G8	P1.30	P1.30	OWM_PE	SPI1B_SDIO2	—	1-Wire Controller Pull-up Enable; SPI1 Port Map B Data 2
F8	P1.31	P1.31	OWM_IO	SPI1B_SDIO3	—	1-Wire Controller Data I/O; SPI1 Port Map B Data 3
H6	P2.1	P2.1	SPI2A_SS1	PT10	—	SPI2 Port Map A Target Select 1; Pulse Train 10

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
M6	P2.2	P2.2	SPI2A_SCK	—	—	SPI2 Port Map A Serial Clock
L6	P2.3	P2.3	SPI2A_MISO	—	—	SPI2 Port Map A Controller In Target Out/ Data 1
K6	P2.4	P2.4	SPI2A_MOSI	—	—	SPI12 Port Map A Controller Out Target In/Data 0
J6	P2.5	P2.5	SPI2A_SS0	PT11	—	SPI2 Port Map A Target Select 0; Pulse Train 11
K4	P2.6	P2.6	—	SPI2B_SDIO 2	—	SPI2 Port Map B Data 2
H5	P2.7	P2.7	I2C0A_SDA	SPI2B_SDIO 3	—	I2C0 Port Map A Serial Data; SPI2 Port Map B Data 3
J4	P2.8	P2.8	I2C0A_SCL	—	—	I2C0 Port Map A Serial Clock
M5	P2.9	P2.9	UART0A_CT S	PT12	—	UART0 Port Map A Clear to Send; Pulse Train 12
L5	P2.10	P2.10	UART0A_RT S	PT14	—	UART0 Port Map A Request to Send; Pulse Train 14
K5	P2.11	P2.11	UART0A_RX	PT13	—	UART0 Port Map A Receive; Pulse Train 13
J5	P2.12	P2.12	UART0A_TX	PT15	—	UART0 Port Map A Transmit; Pulse Train 15
E6	P2.13	P2.13	UART1A_CT S	—	—	UART1 Port Map A Clear to Send
D6	P2.14	P2.14	UART1A_RX	—	—	UART1 Port Map A Receive
D7	P2.15	P2.15	UART1A_RT S	ADC_HW_TR IG_C	—	UART1 Port Map A Request to Send; ADC Hardware Trigger Input C
E7	P2.16	P2.16	UART1A_TX	—	—	UART1 Port Map A Transmit
E2	P2.17	P2.17	I2C1A_SDA	BLE_ANT_C TRL1	—	I2C1 Port Map A Serial Data; Bluetooth Antenna Control Line 1
E3	P2.18	P2.18	I2C1A_SCL	BLE_ANT_C TRL0	—	I2C1 Port Map A Serial Clock; Bluetooth Antenna Control Line 0
E9	P2.20	P2.20	PT5	BLE_ANT_C TRL2	TMR2C_IOA	Pulse Train 5; Bluetooth Antenna Control Line 2; Timer2 Port Map C Input/Output 32-Bits or Lower 16-Bits
D9	P2.21	P2.21	PT7	BLE_ANT_C TRL3	TMR2C_IOB	Pulse Train 7; Bluetooth Antenna Control Line 3; Timer2 Port Map C Input/Output Upper 16-Bits
G9	P2.22	P2.22	PT8	CAN0B_RX	—	Pulse Train 8; Controller Area Network 0 Port Map B Receive Input
F9	P2.23	P2.23	PT6	CAN0B_TX	—	Pulse Train 6; Controller Area Network 0 Port Map B Transmit Output
L4	P2.24	P2.24	PT10	CAN1B_RX	—	Pulse Train 10; Controller Area Network 1 Port Map B Receive Input
G3	P2.25	P2.25	PT11	CAN1B_TX	—	Pulse Train 11; Controller Area Network 1 Port Map B Transmit Output

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
M2	P2.26	P2.26	PT12	SPI0B_SS1	I2S0C_WS	Pulse Train 12; SPIO Port Map B Target Select 1; I2S0 Port Map C Left/Right Word Select
L2	P2.27	P2.27	PT13	SPI0B_MISO	I2S0C_SDI	Pulse Train 13; SPI0 Port Map B Controller In Target Out/Data 1; I2S0 Port Map C Serial Data In
L1	P2.28	P2.28	PT14	SPI0B_MOSI	I2S0C_SDO	Pulse Train 14; SPI0 Port Map B Controller Out Target In/Data 0; I2S0 Port Map C Serial Data Out
K3	P2.29	P2.29	PT0	SPI0B_SCK	I2S0C_SCK	Pulse Train 0; SPI0 Port Map B Serial Clock; I2S0 Port Map C Serial Clock
L3	P2.30	P2.30	PT1	SPI0B_SDIO 2	TMR3C_IOA	Pulse Train 1; SPI0 Port Map B Data 2; Timer 3 Port Map C Input/Output 32-Bits or Lower 16-Bits
K2	P2.31	P2.31	PT2	SPI0B_SDIO 3	TMR3C_IOB	Pulse Train 2; SPI0 Port Map B Data 3; Timer 3 Port Map C Input/Output Upper 16-Bits Only
E10	P3.0	P3.0	AIN0/AIN0N	LPUART0B_ RX	—	ADC Input 0/Comparator 0 Negative Input; Low-Power UART0 Port Map B Receive
E11	P3.1	P3.1	AIN1/AIN0P	LPUART0B_ TX	—	ADC Input 1/Comparator 0 Positive Input; Low-Power UART0 Port Map B Transmit
E12	P3.2	P3.2	AIN2/AIN1N	LPUART0B_ CTS	—	ADC Input 2/Comparator 1 Negative Input; Low-Power UART0 Port Map B Clear to Send
F10	P3.3	P3.3	AIN3/AIN1P	LPUART0B_ RTS	—	ADC Input 3/Comparator 1 Positive Input; Low-Power UART0 Port Map B Request to Send
G10	P3.4	P3.4	AIN4/AIN2N	LPTMR0B_IO A	—	ADC Input 4/Comparator 2 Negative Input; Low-Power Timer0 Port Map B Input/Output 32-Bits or Lower 16-Bits
H10	P3.5	P3.5/ LPTMR0_CL K	AIN5/AIN2P	—	—	ADC Input 5/Comparator 2 Positive Input; LPTMR0 External Clock
F12	P3.6	P3.6/ LPTMR1_CL K	AIN6/AIN3N	—	—	ADC Input 6/Comparator 3 Negative Input; TLPTMR1 External Clock
J10	P3.7	P3.7	AIN7/AIN3P	LPTMR1B_IO A	—	ADC Input 7/Comparator 3 Positive Input; Low Power Timer1 Port Map B Input/ Output 32-Bits or Lower 16-Bits Only Inverted Output
E8	P3.8	P3.8	—	—	—	
D8	P3.9	P3.9	—	—	—	
J9	P4.0	P4.0/PDOWN	—	—	—	Power-Down Output
H9	P4.1	P4.1/ SQWOUT	—	—	—	Square-Wave Output

140 WLP

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	
USB						
B12	DP	—	—	—	—	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See the *USB Design Considerations* section.
C12	DM	—	—	—	—	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled. See the *USB Design Considerations* section.
ANTENNA OUTPUT						
L12	ANT	—	—	—	—	Antenna for Bluetooth Radio. Attach the single-ended, unbalanced Bluetooth radio antenna.
NO CONNECT						
A1, A12, M1, M12	N.C.	—	—	—	—	No Connect.

Detailed Description

The MAX32690 MCU is an advanced SoC featuring an Arm Cortex-M4F CPU, large flash and SRAM memories, and the latest generation Bluetooth 5.2 Low Energy (LE) radio. This device unites processing horsepower with the connectivity required for IoT applications.

The MAX32690 is qualified to operate over the -40°C to +105°C range, which is ideal for industrial environments. The device is available in a 68-pin TQFN-EP (0.40mm pitch) and a 140-bump WLP (0.35mm pitch).

Bluetooth 5.2 Low Energy (LE) radio supports Mesh, LE Audio, AoA, and AoD for direction finding, long-range (coded), and high-throughput modes. A RISC-V core optionally handles timing-critical controller tasks, freeing the programmer from Bluetooth LE interrupt latency concerns.

A cryptographic toolbox (CTB) provides advanced security features, including an MAA for fast ECDSA, AES engine, TRNG, SHA-256 hash, and secure boot loader. Internal code and SRAM space can be expanded off-chip through two quad-SPI execute-in-place (SPIXF and SPIXR) interfaces, up to 512MB each.

Many high-speed interfaces are supported on the device, including multiple QSPI, UART, CAN 2.0B, and I^2C serial interfaces, plus one I^2S port for connecting to an audio codec. Most interfaces support efficient DMA-driven transfers between peripheral and memory. A 12-input (8 external), 12-bit SAR ADC samples analog data at up to 1Msps.

Arm Cortex-M4 with FPU Processor

The Arm Cortex-M4 with FPU CPU is ideal for industrial IoT applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Signed or unsigned data with or without saturation
- Four parallel 8-bit add/sub
- Floating-point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
  - 32- or 64-bit accumulate

RISC-V 32-Bit Core

The RISC-V 32-bit open-source core (RV32) provides stand-alone processing capability as well as being capable of running the Bluetooth stack. The RV32 can access the SPI0, SPI1, SPI2, Bluetooth LE, CAN0, CAN1, all UARTs, all timers, I^2C, 1-Wire, pulse train engines, I^2S, TRNG, and comparators, as well as SRAM8 and a dedicated bank of 256KB flash.

Memory

Internal Flash Memory

3MB of internal flash memory provides nonvolatile program and data memory storage. An additional 256KB of flash is dedicated to the RV32 processor.

Flash can be expanded through the SPIXF flash serial interface backed by 16KB of cache. The SPIXF flash interface can address an additional 512MB.

Internal SRAM

The internal 1MB SRAM provides low-power retention of application information in all power modes. This data-retention feature is optional and configurable. An additional 128KB of SRAM is available to the RV32 (SRAM8). SRAM can be expanded through the SPIXR SRAM serial interface supported by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Spansion HyperBus/Xccela Bus

The Spansion® HyperBus/Xccela bus interface provides external Cypress® Spansion HyperBus and Xccela bus memory products for SRAM and flash. This interface provides a means of high-speed execution from external SRAM or flash, allowing system expansion when internal memory resources are insufficient. Target memory devices are selected with two chip selects. Each chip select addresses up to 512MB SRAM or flash at a speed of up to 60MHz or 120MB/s. It is a high-speed, low-pin count interface that is memory-mapped into the CPU memory space, making access to this external memory as easy as accessing on-chip RAM. Data is transferred over a high-speed, 8-bit bus. HyperBus transfers are clocked using a differential clock, while Xccela bus transfers use a single-ended clock. This interface supports 1.8V operation only.

Features of the HyperBus/Xccela bus interface include:

- Controller/target system
- 120MB/s maximum data transfer rate
- Double data rate (DDR): two data transfers per clock cycle
- Transparent bus operation to the processor
- 16KB write-through cache
- Two chip selects for two memory ports
  - Each port supports memories up to 512MB
- Addresses two external memories, one at a time
- Interfaces to HyperFlash®, HyperRAM®, and Xccela PSRAM
- Zero-wait state burst-mode operation
- Low-power half-sleep mode
  - It puts the external memory device into low-power mode while retaining memory contents
- Configurable timing parameters

External Memory SPI Execute-in-Place (SPIX) Interface

A dedicated high-speed SPI execute-in-place engine supports up to 512MB of external flash memory (SPIXF) running at a speed of up to 60MHz. The use of an external memory provides the flexibility to choose the lowest-cost solution for the application. The SPIXF controller supports single-, dual-, or quad-speed I/O for fast, efficient operation. Instructions are fetched and stored in a 16kB cache to reduce latency and improve system performance. The external program memory is programmed during an authenticated bootloader session. It can be optionally encrypted during loading. Encryption and authentication keys are stored in the fast-wipe key memory.

A second dedicated high-speed SPI execute-in-place engine supports up to 512MB of external SRAM (SPIXR) running at a speed of up to 60MHz. The use of an external memory provides the flexibility to choose the lowest-cost solution for the application. The SPIXR controller supports single-, dual-, or quad-speed I/O for fast, efficient operation. Data or instructions are fetched and stored in a 16kB cache to reduce latency and improve system performance.

Bluetooth 5.2

Bluetooth 5.2 Low Energy (LE) Radio

Bluetooth 5.2 LE is the latest version of the Bluetooth wireless communication standard. It is used for wireless headphones and other audio hardware, as well as for communication between various smart home and internet of things (IoT) devices. Devices operate in the unlicensed 2.4GHz industrial, scientific, and medical (ISM) band. A frequency-hopping transceiver is used to combat interference and fading. The system operates in the 2.4GHz ISM band at 2400MHz to 2483.5MHz. It uses 40 RF channels. These RF channels have center frequencies 2402 + k x 2MHz, where k = 0, ..., 39. The features of the radio include the following:

- Higher transmit power up to +4.5dbm
- 1Mbps, 2Mbps, and long-range coded (125kbps and 500kbps)
- Increased broadcast capability
  - Advertising packet up to 255 bytes
- On-chip matching network to the antenna
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Supports mesh networking

- Supports high-quality audio streaming (isochronous)

Bluetooth 5.2 Software Stack

A Bluetooth 5.2 software stack is available for application developers to quickly add support to devices. The Packetcraft® Host and Controller software stack is provided in library form and provides application developers access to Bluetooth without validation and development of a software stack. The Packetcraft Host and Controller software stack interfaces to the Bluetooth link layer running on RV32. The Packetcraft Host and Controller feature the following:

- C library for linking directly into an application
- Change PHY support
  - Host selects the PHY it needs to use at any given time, enabling long-range or higher bandwidth only when required
    - LE 1M
    - LE Coded S = 2
    - LE Coded S = 8
    - LE 2M
- Bluetooth 5 advertising extension support for enabling next-generation Bluetooth beacons
  - Larger packets and advertising channel offloading
  - Packets up to 255 octets long
  - Advertising packet chaining
  - Advertising sets
  - Periodic advertising
  - High-duty-cycle, nonconnectable advertising
  - Sample applications using standard profiles built on the Packetcraft Host and Controller software framework

Comparators

The eight analog inputs AIN[7:0] can be configured as four pairs and deployed as four independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake the CPU from SLEEP, LOW POWER, or BACKUP operating modes
- Can be active in all power modes

Clocking Scheme

The IPO operates at a maximum frequency of 120MHz.

Optionally, six other oscillators can be selected depending upon power needs:

- 60MHz ISO
- 8kHz INRO
- 32.768kHz ERTCO (external crystal required)
- 7.3728MHz IBRO
- 32MHz ERFO (external crystal required)
- CLKEXT

The SYS_CLK is the primary clock source for the digital logic and peripherals. Select the IBRO to optimize active power consumption. Using the IBRO allows UART communications to meet a 2% baud rate tolerance. Wakeup is possible from either the IBRO or the IPO. The device exits power-on reset using ISO.

An external 32.768kHz timebase is required when using the ERTCO.

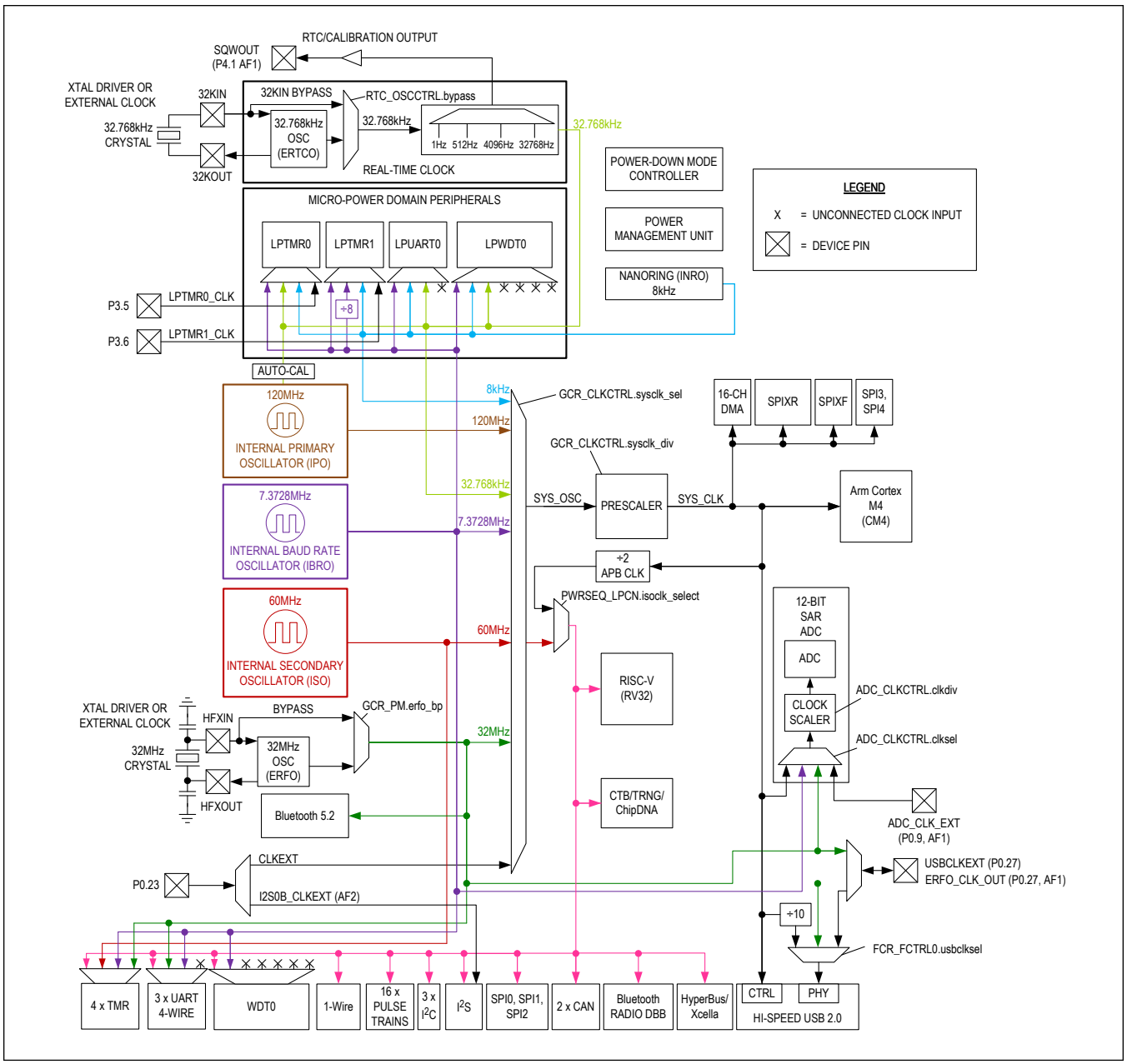


Figure 8. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share a software-controlled I/O function and one or more alternate functions associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a software-controlled I/O. Although this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pull-up resistor or internal pull-down resistor when configured as an input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32690 provides up to 104 GPIO pins. See the *Ordering Information* table for the specific number of GPIOs by part number.

Analog-to-Digital Converter

The 12-bit SAR ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the external analog input signals or the internal power supply inputs.

The reference for the ADC can be:

- External V_{REF} input
- V_{DD3A} analog supply

The ADC measures the following voltages:

- External inputs up to V_{DD3A}
- V_{DDB} divided by 4
- V_{CORE}
- V_{DDA} divided by 2
- V_{DD3A} divided by 4
- V_{SS}

The MAX32690 provides up to eight external analog inputs (AIN[7:0]). See the *Ordering Information* table for the specific number of analog inputs by part number.

Power Management

Power Management Unit (PMU)

The PMU provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains
- Fast wake-up of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CM4 and the RV32 can execute software, and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low-power consumption. The CM4 has access to all system SRAM. The RV32 has a dedicated flash bank of 256KB and access to SRAM8 (128KB). Both the CM4 and the RV32 can execute from their own dedicated internal flash simultaneously.

SLEEP Mode

This mode consumes less power than ACTIVE mode, but wakes faster than LPM because the clocks can optionally be enabled.

The device status is as follows:

- CM4 is asleep
- RV32 is asleep

- Peripherals are on
- Standard DMA is available for optional use
- All oscillators are available for use

LOW POWER Mode (LPM)

This mode is suitable for running the RV32 processor to collect and move data from enabled peripherals.

The device status is as follows:

- The CM4, SRAM0-SRAM7 are in state retention.
- The RV32 can access the SPI0, SPI1, SP2, Bluetooth LE, CAN0, CAN1, all UARTs, all timers, I^2C, 1-Wire, pulse train engines, I^2S, TRNG, and comparators, as well as SRAM8.
- CRC, AES, MAA, and USB are powered down.
- The transition from LPM to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The DMA is not available.
- IPO can optionally be powered down.
- INRO is on.
- The following oscillators are optionally enabled:
  - IBRO
  - ERTCO
  - ISO
  - ERFO

MICRO POWER Mode (UPM)

This mode provides extremely low-power consumption while using a minimal set of peripherals to provide the wake-up capability.

The device status is as follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is retained.)
- The GPIO pins retain their state.
- All non-MICRO POWER domain peripherals are state retained.
  - USB and Bluetooth LE are powered down
  - CRC, AES, and MAA are powered down.
- IPO, ISO, ERFO are powered down.
- INRO is on.
- The following oscillators are optionally enabled:
  - IBRO
  - ERTCO

STANDBY Mode

This mode is used to maintain the system operation while keeping time with the RTC.

The device status is as follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is retained.)
- The GPIO pins retain their state.
- RTC is optionally enabled.
- Wakeup timers are optionally enabled.
- Comparator 0 (CMP0) is optionally enabled.
- All peripherals are state retained except:
  - USB, Bluetooth LE, CRC, AES, and MAA are powered down.
- INRO is on.
- The following oscillators are optionally enabled:
  - ERTCO

BACKUP Mode

This mode is used to maintain the system RAM. The device status is as follows:

- CM4 and RV32 are powered off.
- SRAM can be configured to be state retained as per Table 1.
- All peripherals are powered down.
- The GPIO pins retain their state.
- RTC is optionally enabled.
- Wakeup timers are optionally enabled.
- INRO is on.
- The following oscillators are powered down:
  - IPO
  - ISO
  - IBRO
  - ERFO
- The following oscillators are optionally enabled:
  - ERTCO

Table 1. BACKUP Mode SRAM Retention

RAM BLOCK	RAM SIZE	RETAINED RAM
SRAM0	128KB	121KB
SRAM1	128KB	128KB
SRAM2	128KB	128KB
SRAM3	128KB	128KB
SRAM4	128KB	128KB
SRAM5	128KB	128KB
SRAM6	64KB	64KB
SRAM7	192KB	192KB
SRAM8	128KB	128KB

Note: The boot ROM uses certain ranges of system RAM during a system reset, watchdog timer reset, an external reset, and an exit from BACKUP. The boot ROM uses this RAM to perform system checks. As a result, not all of each RAM can be retained during an exit from BACKUP. Refer to the *MAX32690 User Guide* for details on the address range of retained memory.

Wake-Up Sources

The wake-up sources from the SLEEP, LPM, UPM, STANDBY, and BACKUP operating modes are summarized in Table 2.

Table 2. Wake-Up Sources

OPERATING MODE	WAKE-UP SOURCE
SLEEP	Any enabled peripheral with interrupt capability; RSTN
LOW POWER (LPM)	SPI0, SPI1, SPI2, I^2S, I^2C, CAN0, CAN1, UARTs, Bluetooth LE, watchdog timers, wakeup timer, all comparators, RTC, GPIOs, RSTN, and RV32
MICRO POWER (UPM)	All comparators, LPUART0 (where available), LPTMR0, LPTMR1, LPWDT0, RTC, wakeup timer, GPIOs, and RSTN
STANDBY	RTC, wakeup timer, GPIOs, CMP0 (where available), and RSTN
BACKUP	RTC, wakeup timer, GPIOs, CMP0 (where available), and RSTN

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 sub-second alarm can be programmed with a tick resolution of 244µs. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the SQWOUT alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC polynomial is programmable to support custom CRC algorithms as well as the common algorithms shown in Table 3.

Table 3. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION
CRC-32-ETHERNET	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + x^0$
CRC-CCITT	$x^{16} + x^{12} + x^5 + x^0$
CRC-16	$x^{16} + x^{15} + x^2 + x^0$
USB DATA	$x^{16} + x^{15} + x^2 + x^0$
PARITY	$x^1 + x^0$

Programmable Timers

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0–TMR3 can be individually configured as two 16-bit general-purpose timers
- Timer interrupt

The MAX32690 provides six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, and LPTMR1). LPTMR0 and LPTMR1 are capable of operation in the SLEEP, LPM, and UPM modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See Table 4 for individual timer features.

Table 4. MAX32690 Timer Instances

INSTANCE	REGISTER ACCESS NAME	SINGLE 32-BIT	DUAL 16-BIT	SINGLE 16-BIT	POWER MODE	CLOCK SOURCE						
						PCLK	ISO	IBRO	INRO	ERTCO	LPTMR0_CLK	LPTMR1_CLK
TMR0	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No	Yes	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	Yes	No
LPTMR1*	TMR5	No	No	Yes	ACTIVE, SLEEP, LPM, UPM	No	No	Yes	Yes	Yes	No	Yes

**Available as an internal timer only on the 68-pin TQFN-EP package. There is no external connection to this timer on the 68-pin TQFN-EP package.*

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed WDT, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time. See Table 5 for individual timer features.

The MAX32690 provides two instances of the watchdog timer—WDT0 and LPWDT0.

Table 5. MAX32690 Watchdog Timer Instances

INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE	CLOCK SOURCE			
			PCLK	IBRO	INRO	ERTCO
WDT0	WDT0	ACTIVE, SLEEP, LPM	Yes	Yes	No	No
LPWDT0	WDT1	ACTIVE, SLEEP, LPM, UPM	No	Yes	Yes	Yes

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square-wave or a repeating pattern from 2 to 32 bits

in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Input pulse train module clock can be optionally configured to be independent from the system AHB clock
- Multiple repetition options
  - Single shot (nonrepeating pattern of 2 to 32 bits)
  - Pattern repeats a user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

See Table 6 for details of instances of the pulse train peripheral.

Table 6. MAX32690 Pulse Train Instances

PACKAGE	PULSE TRAIN INSTANCE
140 WLP	PT0-PT15
68 TQFN-EP	PT0-PT8, PT10-PT15

Wakeup Timer

The wakeup timer (WUT) is a unique instance of a 32-bit timer.

- Uses the ERTCO for its clock source
- Programmable prescaler with values from 1 to 4096
- Supports two timer modes:
  - One-Shot: The timer counts up to the terminal value then halts.
  - Continuous: The timer counts up to the terminal value, then repeats.
- Independent interrupt handler

Serial Peripherals

USB Controller

The integrated USB device controller is compliant with the High-Speed (480Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. The USB controller supports DMA for the endpoint buffers. 11 endpoint buffers are a configurable selection of IN or OUT in addition to endpoint 0.

Controller Area Network 2.0B

The integrated CAN interface is compliant with Bosch CAN 2.0B specification (2.0B Active) according to ISO 11898-1.

The key features of the interface:

- ISO 11898-1:2015 compliance
- Up to 8-byte data frame
- Selectable ID type
  - 11-bit standard ID
  - 11-bit standard ID + 18-bit extended ID
- Selectable frame type
  - Data frame (remote transmission request (RTR) = 0)
  - Remote frame (RTR = 1)

- Hardware message filtering (dual/single filters)
- DMA support for transmit and receive
- 128-byte transmit buffer and 256-byte receive buffer
- Overload frame generated on FIFO overflow
- Protocol exception event detection
- Normal and Listen Only modes
- Transmitter delay compensation up to three data bits long
- Single-shot transmission
- Readable error counters
- Last error code
- Sleep mode and wake up unit

I²C Interface

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. This interface supports Standard-mode, Fast-mode, Fast-mode Plus, and High-speed mode I²C speeds. It provides the following features:

- Controller or target mode operation
  - Up to four different target addresses in target mode
- Standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode (IRXM)
- Transmitter FIFO preloading
- Clock stretching to allow slower target devices to operate on higher speed busses
- Multiple transfer rates
  - Standard-mode: 100kbps
  - Fast mode: 400kbps
  - Fast-mode Plus: 1000kbps
  - High-speed mode: 3.4Mbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

See Table 7 for details of the instances of the I²C peripheral.

Table 7. MAX32690 I²C Instances

INSTANCE	PACKAGE	
	140 WLP	68 TQFN-EP
I2C0	Yes	Yes
I2C1	Yes	No
I2C2	Yes	Yes

I²S Interface

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Controller and target mode operation
- 8, 16, 24, and 32-bit frames
- Receive and transmit DMA support
- Wake-up on FIFO status (full/empty/threshold)
- Pulse density modulation support for the receive channel
- Word-select polarity control
- First-bit position selection
- FIFO status interrupts

- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32690 provides one instance of the I^2S peripheral (I2S0).

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface where multiple SPI devices can coexist on a single bus. The bus uses a single clock signal and multiple data signals, as well as one or more target select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either target or controller mode and provide the following features:

- SPI modes 0, 1, 2, or 3 for single-bit communication
- 3- or 4-wire mode for single-bit target device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple target selects on some instances
- Multicontroller mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Target select assertion and deassertion timing with respect to leading/trailing SCK edge

See Table 8 for SPI configuration options.

Table 8. MAX32690 SPI Instances

PACKAGE		INSTANCE	DATA		TARGET SELECT LINES		MAXIMUM FREQUENCY CONTROLLER MODE (MHz)	MAXIMUM FREQUENCY TARGET MODE (MHz)
140 WLP	68 TQFN-EP		140 WLP	68 TQFN-EP	140 WLP	68 TQFN-EP		
Yes	Yes	SPI0	3-wire, 4-wire, dual, or quad data support	3-wire or 4-wire only	2	1	30	60
Yes	No	SPI1	3-wire, 4-wire, dual, or quad data support		3		30	60
Yes	No	SPI2	3-wire, 4-wire, dual, or quad data support		3		30	60
Yes	No	SPI3	3-wire, 4-wire, dual, or quad data support		3		60	60
Yes	No	SPI4	3-wire, 4-wire, dual, or quad data support		3		60	60

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support

- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32690 provides four instances of the UART peripheral—UART0, UART1, UART2, and LPUART0. LPUART0 is capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes. See Table 9 for configuration options.

Table 9. MAX32690 UART Instances

PACKAGE		INSTANCE NAME	REGISTER ACCESS NAME	HARDWARE FLOW CONTROL	POWER MODE	CLOCK SOURCE			
140 WLP	68 TQFN-EP					PCLK	IBRO	ERFO	ERTCO
Yes	Yes	UART0	UART0	140 WLP only	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No
Yes	No	UART1	UART1	Yes	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No
Yes	Yes	UART2	UART2	Yes	ACTIVE, SLEEP, LPM	Yes	Yes	Yes	No
Yes	No	LPUART0	UART3	140 WLP only	ACTIVE, SLEEP, LPM, UPM	No	Yes	No	Yes

1-Wire Controller (OWM)

Analog Device's 1-Wire bus consists of one signal that carries data and also supplies power to the target devices and a ground return. The bus controller communicates serially with one or more target devices through the bidirectional, multidrop 1-Wire bus. The single-contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire controller supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line
- 1-Wire pullup modes include internal pull-up, external fixed pull-up, and optional external strong pull-up

The OWM supports both standard (15.6kbps) and overdrive (110kbps) speeds.

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either RAM or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 16-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Cryptographic Tool Box (CTB)

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers useable for cryptographic seeds or strong cryptography keys to ensure data privacy. Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. Random strings can be added to messages to make encryption indeterministic and avoid replay attacks.

The TRNG is continuously updated by a high-quality, physically-unpredictable entropy source. It generates one random bit per cryptographic clock cycle.

The TRNG can support the system-level validation of many security standards. Contact Analog Devices for details of compliance with specific standards.

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

SHA-2

SHA-2 is a cryptographic hash function. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-2 engine for fast computation of digests supporting:

- SHA-224
- SHA-256
- SHA-384
- SHA-512

Memory Decryption Integrity Unit (MDIU)

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on the fly. Encryption keys are stored in the always-on domain and preserved as long as V_{CORE} is present.

Software Integrity and Root of Trust

Root of Trust

On devices that support SCPBL, the root of trust starts with trusted software and the microcontroller's complement of security features. Communications between a host and the device must be secure and authenticated, and program integrity must be verified each time before execution to ensure the device's trustworthiness. The device's root of trust is based on a secret Analog Devices root verification key and a signed customer verification key (CVK). Customers submit their public CVK, which is then signed, and a certificate is returned to the customer. This process is quick and required only once, before the software is released for the first time, and is unnecessary during the software development. A customer can then load their own key and download their signed binary executable code.

Secure Communications Protocol Bootloader (SCPBL)

On devices that support SCPBL, communication between a host system and the device uses a system of ECDSA-256 digitally signed packets. This guarantees the integrity and authenticity of all communication before executing configuration commands and loading or verifying of program memory. One or more serial interfaces are available for communication. This also enables the assembly and programming of the customer's final product by third-party assembly houses without the required cost and complexity of ensuring that the assembly house implements and maintains a secure production facility. It also allows for in-field software upgrades to deployed products, thus eliminating the costly need to return a product to the manufacturer for any software changes. The serial interfaces available for SCPBL communication are shown in Table 10. Following any reset or exit from certain low-power modes, the device tests the assigned stimulus pin and, if active, begins an SCPBL session. The stimulus pin can be reassigned once an SCPBL session begins. The host can disable the bootloader interface before deployment to prevent any changes to program memory.

See the *Ordering Information* table for availability.

Secure Boot

On devices that support SCPBL, the device performs a secure boot to confirm that the root of trust has not been compromised. Following every reset and exit from certain low-power modes, the secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted, thereby ensuring the trustworthiness of the application software. Failure to verify the digital signature transitions the device to safe mode, which prevents execution of the customer code. During the development phase, the bootloader can be reactivated and a new, trusted program memory loaded.

Applications Information

Bypass Capacitor Recommendations

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Description* table indicates which pins should be connected to bypass capacitors and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the pin description shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Place capacitors as close as possible to their corresponding device pins. When more than one value of capacitor is recommended per pin, the capacitors should be placed in parallel starting with the lowest value capacitor closest to the pin.

USB Design Considerations

If USB is not used, the DP and DM signals should be left unconnected, V_{DDB} should be tied to V_{SS} through a 500Ω resistor, and V_{SSB} (if available on the package) connected to V_{SS}.

The device does not provide a dedicated USB V_{BUS} detect pin, so the 3.3V V_{DDB} supply input serves as both the power supply for the embedded USB transceiver and the detect for the V_{BUS} signal. Voltage should be applied to the V_{DDB} pin only while the V_{BUS} signal is present and removed whenever the V_{BUS} signal is not present. Figure 9 and Figure 10 suggests two solutions.

1. Power can be controlled by connecting a 3.3V LDO regulator between V_{BUS} and the V_{DDB} pin. The LDO requires a 1µF capacitor placed as close as possible to the LDO for proper operation. The 1µF capacitor can be omitted if the capacitor required by the USB specification is located close to the LDO.
2. V_{DDB} can be connected to a 3.3V supply through a load switch. The 5V-compatible enable of the load switch should be tied to V_{BUS}. A 10kΩ resistor between V_{BUS} and V_{SS} is required to discharge the capacitance on V_{BUS} for the load switch enable.

In any implementation, bypass the V_{DDB} signal to V_{SSB} (or V_{SS}, if V_{SSB} is not pinned out) through an additional 1µF capacitor placed as close as possible to the V_{DDB} pin.

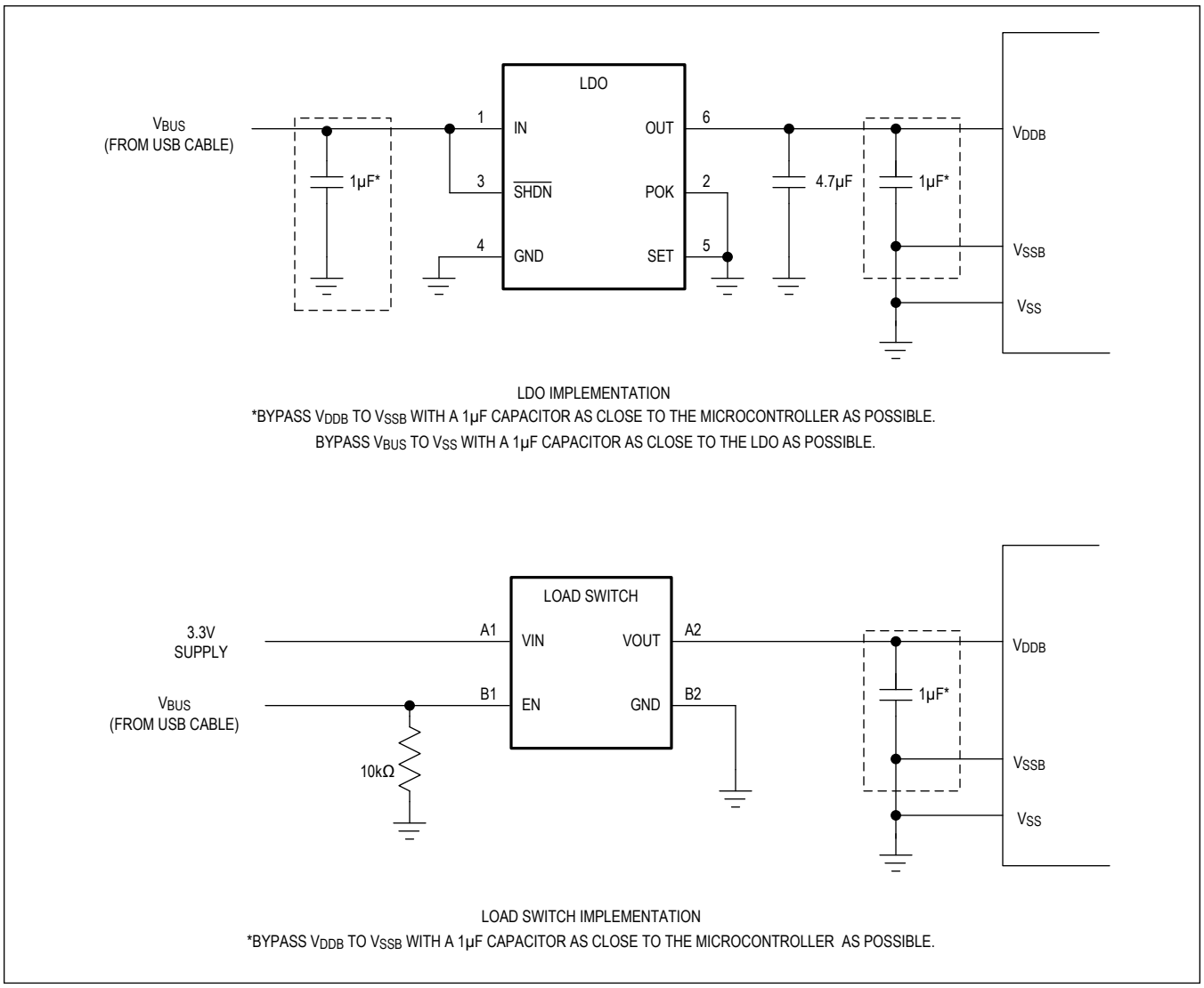


Figure 9. V_{DDB} Signal Implementation, 140-Bump WLP

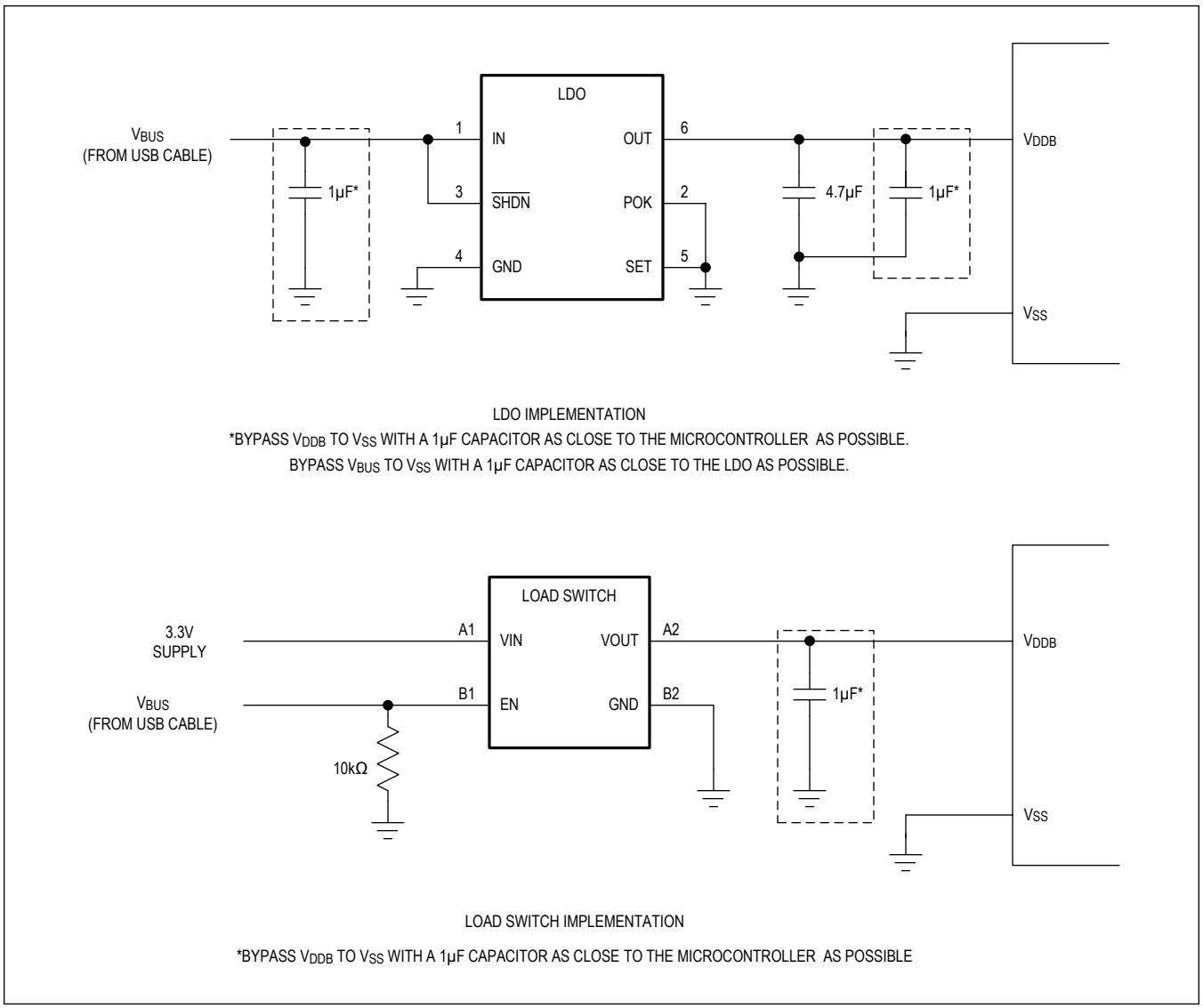


Figure 10. V_{DDB} Signal Implementation, 68-Pin TQFN

Transmitted Spurious Emissions

Various local regulatory agencies can impose limits on transmitted spurious emissions. At maximum output power of +4.5dBm, compliance with local regulations can require either an antenna with at least 6dB rejection at the 7.2GHz third harmonic or the use of a low-pass filter network between the device RF port and antenna. The MAX32690 is designed with an on-chip matching network providing a 50Ω impedance at the ANT device pin. Filter design must match this impedance for best efficiency.

Bootloader Activation

The SCPBL can use the interfaces shown in Table 10.

Table 10. Bootloader Activation Summary

PART NUMBER	BOOTLOADER INTERFACE		DEFAULT STIMULUS PIN
	UART	USB	
MAX32690GTKBL MAX32690GWEBL	UART0_RX UART0_TX	DP DM	P4.0 (ACTIVE LOW)

On devices that support SCPBL, the SCPBL is activated following any reset or exiting certain low-power modes if the assigned stimulus pin is asserted. The design must ensure that the desired bootloader interface and stimulus pin is accessible by the host or the SCPBL cannot be activated. A different stimulus pin can be assigned once an SCPBL session has been started.

The RSTN signal must also be accessible by the host for initial synchronization with the SCPBL.

Typical Fixed Current Consumption Temperature Variance

ACTIVE Mode

Table 11. Fixed V_{CORE} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{CORE} Current, ACTIVE Mode	I_{CORE_FACT}	Fixed, IPO enabled, ISO enabled, total current into V_{CORE} pin, V_{CORE} = 1.1V, CM4 in ACTIVE mode 0MHz, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA, V_{CORE} and V_{DDA} voltage monitors enabled	1	1.8	3.1	6	8.1	mA

ACTIVE Mode

Table 12. Fixed V_{DDA} Current Consumption ACTIVE Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{DDA} Fixed Current, ACTIVE Mode	I_{DDA_FACT}	Fixed, IPO enabled, total current into V_{DDA} pins, V_{DDA} = 1.8V, CM4 in ACTIVE mode 0MHz execution, RV32 in ACTIVE mode 0MHz execution; inputs tied to V_{SS} or V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA, V_{CORE} and V_{DDA} voltage monitors enabled	370	400	430	450	445	µA

Fixed SLEEP Mode

Table 13. Fixed V_{CORE} Current Consumption SLEEP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{CORE} Fixed Current, SLEEP Mode	I_{CORE_FSLP}	Fixed, IPO enabled, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	2.9	3.7	5	7.9	10	mA

Fixed SLEEP Mode

Table 14. Fixed V_{DDA} Current Consumption SLEEP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{DDA} Fixed Current, SLEEP Mode	I_{DDA_FSLP}	Fixed, IPO enabled, f_{SYS_CLK} = 120MHz, total current into V_{DDA} pins, CM4 in SLEEP mode, RV32 in SLEEP mode, standard DMA with two channels active	370	400	430	450	445	µA

Fixed LOW POWER Mode

Table 15. Fixed V_{CORE} Current Consumption LOW POWER Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{CORE} Fixed Current, LOW POWER Mode	I_{CORE_FLP}	Fixed, ISO enabled, total current into V_{CORE} pins, V_{CORE} = 1.1V, CM4 powered off, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	0.65	1	1.6	2.9	3.9	mA

Fixed LOW POWER Mode

Table 16. Fixed V_{DDA} Current Consumption LOW POWER Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{DDA} Fixed Current LOW POWER Mode	I_{DDA_FLP}	Standby state with full data retention, V_{CORE} and V_{DDA} voltage monitors enabled	50	54	57	60	61	µA

Fixed STANDBY Mode

Table 17. Fixed V_{CORE} Current Consumption STANDBY Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{CORE} Fixed Current, STANDBY Mode	I_{CORE_STBY}	Fixed, total current into V_{CORE} pins, V_{CORE} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	0.28	0.61	1.7	5.3	9	µA

Fixed STANDBY Mode

Table 18. Fixed V_{DDA} Current Consumption STANDBY Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{DDA} Fixed Current, STANDBY Mode	I_{DDA_STBY}	Fixed, total current into V_{DDA} pins, V_{DDA} = 1.8V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	8.2	23	61	170	275	µA

Fixed BACKUP Mode

Table 19. Fixed V_{DDA} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	COMMON CONDITIONS	CONDITIONS	TYPICAL					UNITS
				-40°C	+25°C	+55°C	+85°C	+105°C	
V_{DDA} Fixed Current, BACKUP Mode	I_{DDA_BKU}	Total current into V_{DDA} pins, V_{DDA} = 1.8V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	All SRAM retained	7.4	17	42	120	190	µA
			No SRAM retention	1.7	2.5	4.1	7.9	11.5	µA

Fixed BACKUP Mode

Table 20. Fixed V_{CORE} Current Consumption BACKUP Mode

PARAMETER	SYMBOL	CONDITIONS	TYPICAL					UNITS
			-40°C	+25°C	+55°C	+85°C	+105°C	
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_BKU}	V_{CORE} = 1.1V	0.29	0.695	2	6.6	11	µA

Ordering Information

PART NUMBER	SCPBL	SPIXR/ SPIXF	TMR	LPTMR	I²C	SPI	PT	CMP	EXTERNAL ADC INPUTS	UART	GPIO	PIN-PACKAGE
MAX32690GTK+	No	No	3	1	1	3	15	1	3	2	38	68 TQFN-EP, 8mm x 8mm, 0.4mm pitch
MAX32690GTK+T	No	No	3	1	1	3	15	1	3	2	38	68 TQFN-EP, 8mm x 8mm, 0.4mm pitch
MAX32690GWE+	No	Yes	4	2	3	5	16	4	8	3	104	140 WLP, 4.5mm x 4.5mm, 0.35mm pitch
MAX32690GWE+T	No	Yes	4	2	3	5	16	4	8	3	104	140 WLP, 4.5mm x 4.5mm, 0.35mm pitch

All packages contain USB 2.0 device, CAN 2.0B, Bluetooth 5.2, HyperBus, LPUART, OWM, and I²S.

CMP = Comparators; PT = Pulse Train; TMR = Timer; SPIXR = SPI Execute-in-Place RAM; SPIXF = SPI Execute-in-Place Flash; LPTMR = Low-Power Timer; SCPBL = Secure Communications Protocol Bootloader

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/22	Release for market intro	—
1	5/23	Updated Benefits and Features, Simplified Block Diagram, Absolute Maximum Ratings, Electrical Characteristics, the 68 TQFN-EP Pin Descriptions, the 140 WLP Pin Descriptions, the Detailed Description, added USB Design Considerations, updated Bootloader Activation, Typical Fixed Current Consumption Temperature Variance, and removed future product from MAX32690GWE+ and MAX32690GWE+T in the Ordering Information table.	1–2, 8–13, 15–18, 20, 31-34, 36, 38–40, 45–46, 49–50, 52–55, 57–60, 61–63, 64–66, 67