MAX32655
ERRATA SHEET

Revision B1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the top side of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the product webpage at www.analog.com/MAX32655.

1) BOOTLOADER SHA-256 HASH CHECK COMMAND OUTPUTS INCORRECT RESULT WHEN LENGTH NOT A MULTIPLE OF 64 BYTES

Description:
Bootloader SHA-256 Hash Check Command "H" outputs an incorrect result when the length is not a multiple of 64 bytes.

Workaround:
When issuing the “H” command, ensure that the requested HASH length is a multiple of 64 bytes.

2) DEVICE WILL NOT EXIT FROM MICRO POWER MODE WHILE RUNNING FROM THE IBRO

Description:
If the device is running from the IBRO and then subsequently enters the MICRO POWER mode, the device will not exit properly from the MICRO POWER mode as intended. (MBU2318)

Workaround:
Set the system clock (f_{SYS_CLK}) to operate from the IPO or the ISO before entering MICRO POWER mode.

3) INCORRECT DATA IS TRANSMITTED IF AN EMPTY SPI FIFO IS WRITTEN WHILE A TRANSFER IS IN PROGRESS

Description:
In target mode, if data is fed into an empty transmit FIFO while chip select is active and an SPI transfer is in progress (the SPI clock is provided by the controller), the first FIFO byte gets transferred immediately and is seen as shifted or incomplete in the SPI MISO line. (18101)

Workaround:
Ensure that the target SPI does not let its transmit FIFO become empty.

4) UART TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

419-100124; Rev 0; 4/24

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18117)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

5) UART TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18135)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

6) I^2S TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18118)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

7) I^2S TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18136)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

MAX32655
REV B1 ERRATA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/24	Initial release	—