MAX32655
ERRATA SHEET

Revision A1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the top side of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the product webpage at ***www.analog.com/MAX32655****.*

1) BOOTLOADER SHA-256 HASH CHECK COMMAND OUTPUTS INCORRECT RESULT WHEN LENGTH NOT A MULTIPLE OF 64 BYTES

Description:
Bootloader SHA-256 Hash Check Command "H" outputs an incorrect result when the length is not a multiple of 64 bytes.

Workaround:
When issuing the “H” command, ensure that the requested HASH length is a multiple of 64 bytes.

2) HIGH V_{REGI} SUPPLY CURRENT IN BACKUP (BKU) AND STANDBY (STB) MODES OF OPERATION

Description:
The V_{REGI} supply current is higher than expected in the BACKUP (BKU) and STANDBY (STB) modes of operation.

Workaround:
When it is desired to operate in BACKUP or STANDBY modes of operation, the V_{DDA} power supply pin should be biased to its lowest range of operation. This will minimize the V_{REGI} current. Refer to the device datasheet for V_{DDA} power supply pin operating range.

3) SPI MODE 1 AND MODE 3 FAIL AT MAXIMUM SERIAL CLOCK RATES

Description:
Both SPI0 and SPI1 include this limitation in both controller and target mode operation.

Workaround:
Operate the SPI0 at a maximum speed of 25MHz for both controller and target mode. Operate SPI1 at a maximum speed of 25MHz for controller mode and 12.5MHz for target mode.

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4) ALL ADC/COMPARATOR INPUTS HAVE RESTRICTED OPERATING VOLTAGE RANGE

Description:
The operating range of the ADC/comparator inputs is restricted to 1.8V, max.

Workaround:
None.

5) DEVICE WILL NOT EXIT FROM MICRO POWER MODE WHILE RUNNING FROM THE IBRO

Description:
If the device is running from the IBRO and then subsequently enters the MICRO POWER mode, the device will not exit properly from the MICRO POWER mode as intended.

Workaround:
Set the system clock (f_{SYS_CLK}) to operate from the IPO or the ISO before entering MICRO POWER mode.

6) ECC FEATURE NOT SUPPORTED

Description:
This feature is not supported on this revision of the device. Treat all register fields associated with the ECC feature as Do Not Modify (DNM). (MBU2300)

Workaround:
None.

7) I^2C TARGET REGISTER OFFSETS DIFFERENT

Description:
The addressing scheme of the I^2C Target Address Registers in this silicon revision differs from later versions. (MBU2301)

Workaround:
Use the following register offsets:

REGISTER OFFSET	REVISION A1 REGISTER	REVISION B1 REGISTER
[0x004C]	I2Cn_SLAVE	N/A
[0x004C]	N/A	I2Cn_SLAVE0
[0x0050]	N/A	I2Cn_SLAVE1
[0x0054]	N/A	I2Cn_SLAVE2
[0x0058]	N/A	I2Cn_SLAVE3

8) POWER SEQUENCING REQUIREMENT FOR V_{REGI} AND V_{DDA} SUPPLIES

Description:
The design of the SIMO requires that V_{REGI} must rise to a valid level within a window related to the V_{DDA} voltage.

Workaround:
If power to the device is cycled, V_{REGI} must exceed $V_{REGI\_POR(MIN)}$ within 20ms after V_{DDA} > 1.24V. After that, V_{REGI} can settle to its final value.

9) PART MAY RESET IF RTC SUBSECOND ALARM IS USED TO EXIT DEEPSLEEP

Description:
When using the RTC subsecond alarm to wake the device from DEEPSLEEP, after a few successful wake events, the part will eventually reset. Further attempts to enter DEEPSLEEP then continue to cause the part to reset. (MBU2299)

Workaround:
Clear PWRSEQ_LPPWST.rstwkst before entering DEEPSLEEP mode.

10) RTC FAILS TO WAKE DEVICE FROM DEEPSLEEP

Description:
The device does not behave as expected if the device immediately enters DEEPSLEEP too soon after a DEEPSLEEP wakeup from the RTC occurs. (MBU2298)

Workaround:
Delay at least 85µs before reentering DEEPSLEEP after a DEEPSLEEP wakeup from the RTC occurs.

11) I^2C CONTROLLER FAILS AT OVR SETTING OF V_{CORE} = 0.9V

Description:
The SDA signal does not work as expected. (MBU2325)

Workaround:
Set the GCR_SYSCTRL.OVR field to a V_{CORE} voltage higher than 0.9V.

12) QSPI CONTROLLER TXFIFO EMPTY CONDITION CHANGE FOLLOWING ACTIVE SCK CYCLE

Description:
The internal assertion of the TXFIFO empty condition corrupts the SCK signal. (MBU2319)

Workaround:
Ensure that the QSPI does not let its transmit FIFO become empty.

13) LOW SIMO REGULATOR OUTPUT VOLTAGE SETTINGS IGNORED

Description:
Hardware default settings could override the values of the SIMO_VREGO_A.vseta, SIMO_VREGO_B.vsetb, SIMO_VREGO_C.vseta, or SIMO_VREGO_A.vseta fields if set too low. (17219)

Workaround:
None.

14) CM4 INTERRUPT ASSIGNED TO VECTOR 4

Description:
On this revision of the device, the CM4 interrupt request is assigned to vector 4, which is shared with the power-fail interrupt. (17249)

Workaround:
None.

15) GPIO0.14 DOES NOT SUPPORT THE I²S EXTERNAL CLOCK SOURCE FUNCTION

Description:
The I²S external clock source function is not supported. (MBU2297)

Workaround:
None.

16) WAKEUP TIMER 1 (WUT1) NOT SUPPORTED

Description:
This peripheral is not supported on this revision of the device. Treat all register fields associated with the peripheral as Do Not Modify (DNM). (MBU296)

Workaround:
None.

17) UART RECEIVE FIFO FAILS TO ASSERT OVERRUN INTERRUPT

Description:
The receive FIFO does not reliably assert the overrun interrupt. (MBU2303)

Workaround:
Poll the receive FIFO level and use software to manage the FIFO contents.

18) ERFO READY INTERRUPT AND INTERRUPT ENABLE NOT SUPPORTED

Description:
The EFRO_INTFL.rdy and ERFO_INTEN.rdy fields are not supported. Treat these fields as Do Not Modify (DNM). (MBU2324)

Workaround:
None.

19) ERTCO DISABLE FEATURE NOT SUPPORTED

Description:
The MCR_CTRL.x32k_en field is not supported on this revision. Treat it as Do Not Modify (DNM). (MBU2294)

Workaround:
None.

20) IN TARGET MODE, SPI FIFO TRANSMITS UNEXPECTED DATA WHEN TX FIFO EMPTY

Description:
After an SPI transmit FIFO is empty, the device is expected to transmit 0x00 on subsequent clocks. Instead, when the FIFO empty condition is met, the device will continue to loop through the FIFO and transmit its contents. (17277)

Workaround:
None.

21) INCORRECT DATA IS TRANSMITTED IF AN EMPTY SPI FIFO IS WRITTEN WHILE A TRANSFER IS IN PROGRESS

Description:
In target mode, if data is fed into an empty transmit FIFO while chip select is active and an SPI transfer is in progress (the SPI clock is provided by the controller), the first FIFO byte gets transferred immediately and is seen as shifted or incomplete in the SPI MISO line. (18101)

Workaround:
Ensure that the target SPI does not let its transmit FIFO become empty.

22) IPO WARMUP COUNTER DOES NOT RESET CORRECTLY

Description:
The IPO warmup counter is not reset correctly, which causes GCR_CLKCTRL.ipo_rdy to be set to 1 prematurely. (MBU2320)

Workaround:
Use a counter to delay 2048 IPO clocks after setting GCR_CLKCTRL.ipo_en to 1 before using the IPO for precision timing.

23) ICC1 CACHE LINE FILL BUFFER NOT CLEARED

Description:
The cache line fill buffer is not automatically cleared when the cache is enabled, resulting in stale data. (17246)

Workaround:
Invalidate the cache, enable it, then invalidate it again to clear the stale data.

24) UART TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18117)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

25) UART TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18135)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

26) I²S TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18118)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

27) I²S TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18136)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/20	Initial release	—
1	4/24	Removed erratum 4; updated master/slave to controller/target; added errata 6–27	All

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