

4.5V to 60V, 300mA, Ultra Small, High-Efficiency Synchronous Step-Down DC-DC Converters

MAX17570

Product Highlights

- Reduces External Components and Total Cost
 - No Schottky—Synchronous Operation
 - Internal Compensation
 - Internal Soft-Start
 - All-Ceramic Capacitors, Ultra-Compact Layout
- Flexibility to Support Multiple Rails in a System
 - Wide 4.5V to 60V Input Voltage Range
 - Fixed 3.3V and 5V Output Options
 - Adjustable Output from 0.9V to 97% of V_{IN}
 - Delivers Up to 300mA Load Current
 - 200kHz to 1MHz Adjustable Switching Frequency with External Clock Synchronization
- Reduces Power Dissipation
 - 95.8% Peak Efficiency for $V_{IN} = 15V$, $V_{OUT} = 12V$, $I_{OUT} = 150mA$
 - Shutdown Current = 2.2 μA (typ)
 - PFM Options for Superior Light Load Efficiency
- Operates Reliably in Adverse Industrial Environments
 - Hiccup-Mode Current Limit and Autoretry Startup
 - Open-Drain Power Good Output (RESET Pin)
 - Programmable EN/UVLO Threshold
 - Monotonic Startup into Prebiased Output
 - Overtemperature Protection
 - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range
 - Complies with CISPR32 (EN55032) Class B Conducted and Radiated Emissions

Key Applications

- Factory Automation

Within the factory automation space, which includes many different applications, one key need is the ability to generate less heat. Heat within the system must be managed, prevent overheating and shutdown. The MAX17570 produces less heat as it is a fully synchronous DC-DC with integrated FETs with high efficiency. The more efficient a switching regulator is, the less it loses the power and therefore create less heat in the system.

- Aftermarket Automotive

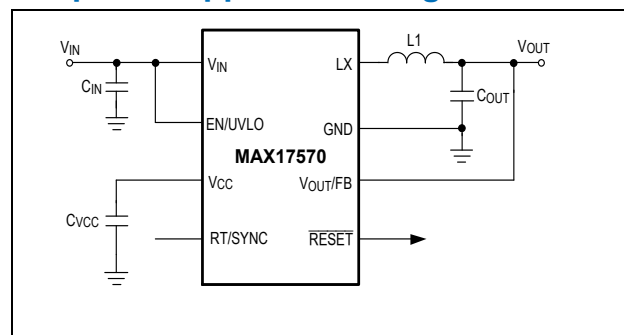
An example of within the aftermarket automotive space where the MAX17570 provides a benefit is asset tracking application. Asset tracking has increased in popularity as the ability to wireless connect to these

monitors has become easier. Typically, these units are designed to be as small as possible. The MAX17570 has integrated FETs, integrated compensation, and can even have pre-programmed output voltages, all delivering a small solution size. Small size and fewer components help drive overall design cost down for the system.

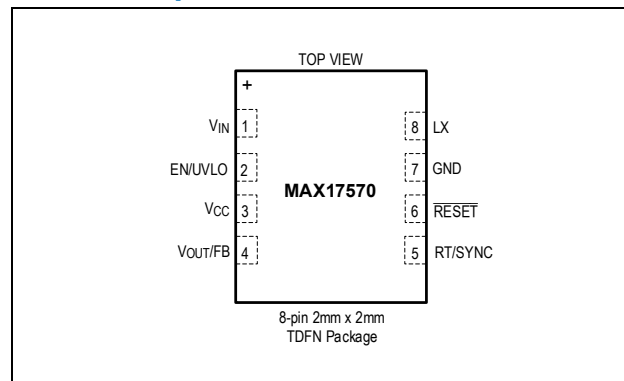
- General Point of Load

General point of load is just that, a generic term. It applies to a switching regulator that serves many applications and design environments. Critical to any environment is the robustness of the power conversion. With an operating range of -40°C to +125°C, current limit protection, overtemperature protection, and the ability to adhere to the CISPR-32 class B emission standards, the MAX17570 delivers a small, highly efficient power conversion in the most adverse environments and provides the designer the peace of mind that it is robust and reliable.

Simplified Application Diagram



Pin Description



[Ordering Information](#) appears at end of data sheet.

Absolute Maximum Ratings

| | | | |
|--|---------------------------------|--|---|
| V_{IN} to GND | -0.3V to +70V | Continues Power Dissipation ($T_A = +70^{\circ}\text{C}$) (derate 6.2mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)..... | 496mW |
| EN/UVLO, LX to GND | -0.3V to $V_{IN} + 0.3\text{V}$ | Operating Temperature Range (Note 1) | -40°C to $+125^{\circ}\text{C}$ |
| V_{CC} , $V_{OUT}/\overline{\text{FB}}$, $\overline{\text{RESET}}$ to GND | -0.3V to +6V | Junction Temperature | $+150^{\circ}\text{C}$ |
| RT/SYNC to GND | -2V to +6V | Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| LX total RMS Current | 800mA | Soldering Temperature (reflow)..... | $+260^{\circ}\text{C}$ |
| Output Short-Circuit Duration | Continuous | Lead Temperature (soldering, 10s) | $+300^{\circ}\text{C}$ |

Note 1: Junction temperature greater than $+125^{\circ}\text{C}$ degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

| | |
|---|---------------------------------|
| Package Code | T822C+6C |
| Outline Number | 21-100514 |
| Land Pattern Number | 90-100183 |
| Thermal Resistance, Four Layer Board | |
| Junction-to-Ambient (θ_{JA}) | 162 $^{\circ}\text{C}/\text{W}$ |
| Junction-to-Case Thermal Resistance (θ_{JC}) | 20 $^{\circ}\text{C}/\text{W}$ |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN} = 24V$, $V_{GND} = 0V$, RT/SYNC = unconnected ($f_{SW} = 400kHz$), $C_{IN} = C_{VCC} = 1\mu F$, $V_{EN/UVLO} = 1.5V$, LX = \overline{RESET} = OPEN, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to GND, unless otherwise noted. (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|------------------------|---|-------|-------|-------|--------|
| INPUT SUPPLY (V _{IN}) | | | | | | |
| Input Voltage Range | V _{IN} | | 4.5 | | 60 | V |
| Input Shutdown Current | I _{IN-SH} | V _{EN/UVLO} = 0V, shutdown mode | | 2.2 | 4 | μA |
| Input Supply Current | I _{Q-PFM} | MAX17570D/E/F, V _{OUT} /FB = 1.03 x V _{OUT} /FB-REG | | 145 | 300 | μA |
| | I _{Q-PWM} | MAX17570A/B/C, Normal switching mode, V _{IN} = 24V | | 2.5 | 4 | mA |
| ENABLE/UVLO (EN/UVLO) | | | | | | |
| EN/UVLO Threshold | V _{ENR} | V _{EN/UVLO} rising | 1.19 | 1.215 | 1.24 | V |
| | V _{ENF} | V _{EN/UVLO} falling | 1.06 | 1.09 | 1.15 | |
| | V _{EN-TRUESD} | V _{EN/UVLO} falling, true shutdown | | 0.75 | | |
| EN/UVLO Input Leakage Current | I _{EN/UVLO} | V _{EN/UVLO} = 60V, T _A = +25°C | -100 | | +100 | nA |
| LDO (V _{CC}) | | | | | | |
| V _{CC} Output Voltage Range | V _{CC} | 6V ≤ V _{IN} ≤ 60V, 0mA < I _{VCC} < 10mA | 4.75 | 5 | 5.25 | V |
| V _{CC} Current Limit | I _{VCC-MAX} | V _{CC} = 4.3V, V _{IN} = 12V | 13 | 30 | 50 | mA |
| V _{CC} Dropout | V _{CC-DO} | V _{IN} = 4.5V, I _{VCC} = 5mA | | 0.15 | 0.3 | V |
| V _{CC} UVLO | V _{CC-UVR} | V _{CC} rising | 4.05 | 4.18 | 4.3 | V |
| | V _{CC-UVF} | V _{CC} falling | 3.7 | 3.8 | 3.95 | |
| POWER MOSFETs | | | | | | |
| High-Side pMOS On-Resistance | R _{DS-ONH} | I _{LX} = 0.3A, (sourcing) | | 1.38 | 2.76 | Ω |
| Low-Side nMOS On-Resistance | R _{DS-ONL} | I _{LX} = 0.3A, (sinking) | | 0.5 | 1 | Ω |
| LX Leakage Current | I _{LX-LKG} | V _{EN/UVLO} = 0V, V _{IN} = 60V, T _A = +25°C, V _{LX} = (V _{GND} + 1V) to (V _{IN} - 1V) | -1 | | +1 | μA |
| SOFT-START (SS) | | | | | | |
| Soft-Start Time | t _{SS} | Soft-Start Clock Period is twice the RT calculated period | | 512 | | Cycles |
| FEEDBACK (FB) | | | | | | |
| FB Regulation Voltage | V _{FB-REG} | MAX17570C | 0.887 | 0.9 | 0.913 | V |
| | | MAX17570F | 0.887 | 0.915 | 0.936 | |
| FB Leakage Current | I _{FB} | MAX17570C, MAX17570F, T _A = +25°C | -100 | -25 | | nA |
| OUTPUT VOLTAGE | | | | | | |
| V _{OUT} Regulation Voltage | V _{OUTREG} | MAX17570A | 3.25 | 3.3 | 3.35 | V |
| | | MAX17570D | 3.25 | 3.35 | 3.42 | |
| | | MAX17570B | 4.93 | 5 | 5.07 | |
| | | MAX17570E | 4.93 | 5.08 | 5.18 | |
| V _{OUT} Leakage Current | I _{VOUT} | MAX17570A, MAX17570B, MAX17570D, MAX17570E | | 11.5 | | uA |
| CURRENT LIMIT | | | | | | |

($V_{IN} = 24V$, $V_{GND} = 0V$, $RT/SYNC$ = unconnected ($f_{SW} = 400kHz$), $C_{IN} = C_{VCC} = 1\mu F$, $V_{EN/UVLO} = 1.5V$, $LX = \overline{RESET} = OPEN$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. All voltages are referenced to GND, unless otherwise noted. ([Note 2](#))

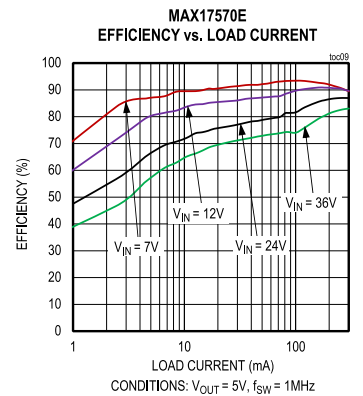
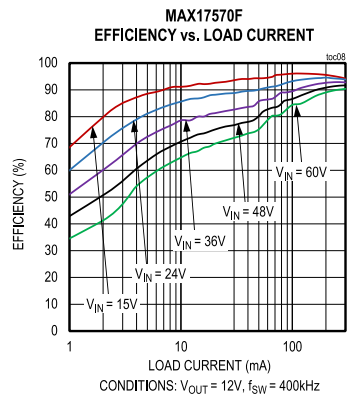
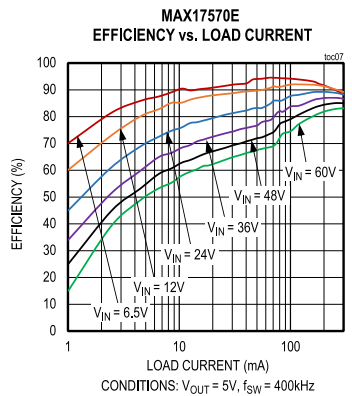
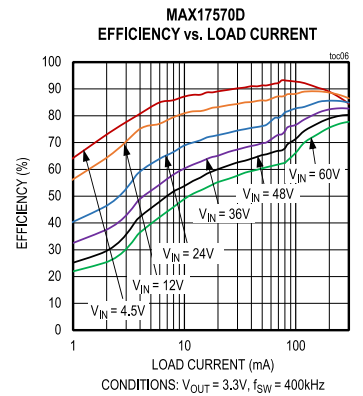
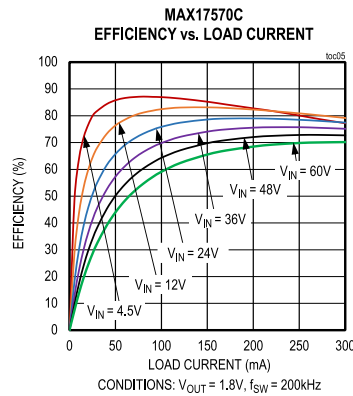
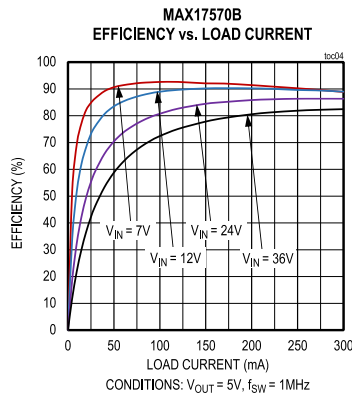
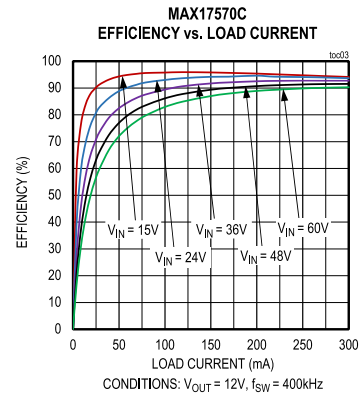
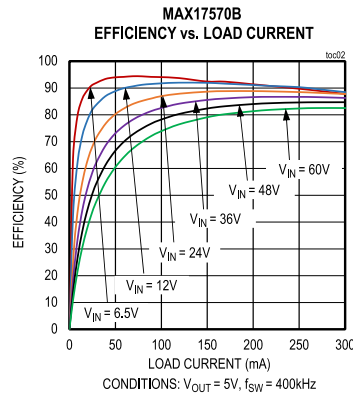
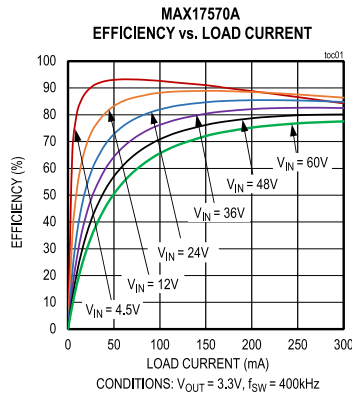
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------------------|---|-----------------------------|-------|-----------------------|--------|
| Peak Current-Limit Threshold | I _{PEAK-LIMIT} | | 0.49 | 0.56 | 0.62 | A |
| Runaway Current-Limit Threshold | I _{RUNAWAY-LIMIT} | | 0.58 | 0.66 | 0.73 | A |
| Negative Current-Limit Threshold | I _{SINK-LIMIT} | MAX17570A/B/C | -0.25 | -0.3 | -0.35 | A |
| | | MAX17570D/E/F | | +15 | | mA |
| Pulse-Frequency Modulation (PFM) Current Level | I _{PFM} | MAX17570D/E/F | | 0.15 | | A |
| RT AND SYNC | | | | | | |
| Switching Frequency | f _{SW} | R _{RT} = 4.7k | 180 | 200 | 220 | kHz |
| | | R _{RT} = 26.4k | 900 | 1000 | 1100 | |
| | | R _{RT} = unconnected | 360 | 400 | 440 | |
| V _{FB} Undervoltage Trip Level to Cause Hiccup | V _{FB-HICF} | | 62.5 | 64.5 | 66.5 | % |
| HICCUP Timeout | | Hiccup Clock Period is twice the RT calculated period | | 32768 | | Cycles |
| Minimum On-Time | t _{ON-MIN} | | | 90 | 130 | ns |
| Minimum Off-Time | t _{OFF-MIN} | | | 125 | 145 | ns |
| LX Dead Time | | | | 5 | | ns |
| RT/SYNC Bias Current | I _{RT_BIAS} | | | 45 | | uA |
| SYNC Frequency Capture Range | | f _{SW} set by R _{RT/SYNC} | 1.1 X f _{SW} | | 1.4 X f _{SW} | kHz |
| SYNC Pulse Width | t _{SYNC} | | 100 | | | ns |
| SYNC Duty-Cycle Range | D _{SYNC} | | 10 | | 90 | % |
| SYNC Threshold | V _{IH} | At RT/SYNC pin (Note 3) | V _{RT/SYN C} + 0.2 | | | V |
| | V _{IL} | At RT/SYNC pin (Note 3) | V _{RT/SYN C} - 0.2 | | | V |
| RESET | | | | | | |
| FB/V _{OUT} Threshold for RESET Rising | | V _{OUT} /FB rising | 93.5 | 95 | 97.5 | % |
| FB/V _{OUT} Threshold for RESET Falling | | V _{OUT} /FB falling | 90 | 92 | 94 | % |
| RESET Delay After FB/V _{OUT} Reaches 95% Regulation | | RESET Clock Period is the RT calculated period | | 1024 | | Cycles |
| RESET Output Level Low | | I _{RESET} = 1mA | | | 0.2 | V |
| RESET Output Leakage Current | | V _{RESET} = V _{CC} = 5.5V, T _A = +25°C | | | 0.1 | μA |
| THERMAL SHUTDOWN | | | | | | |
| Thermal-Shutdown Threshold | | Temperature rising | | 166 | | °C |
| Thermal-Shutdown Hysteresis | | | | 20 | | °C |

Note 2: All the limits are 100% tested at $T_A = +25^{\circ}\text{C}$. Limits over temperature are guaranteed by design.

Note 3: $V_{\text{RT/SYNC}} = I_{\text{RT_BIAS}} \times R_{\text{RT/SYNC}}$. For more details, see the [Switching Frequency and Clock Synchronization](#) section.

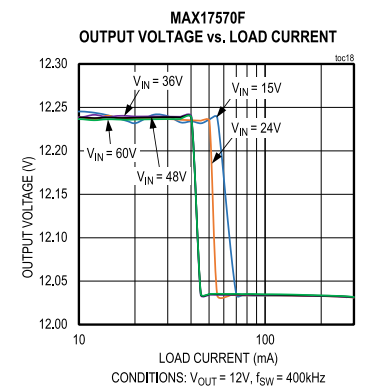
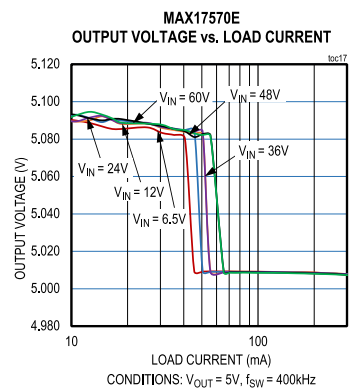
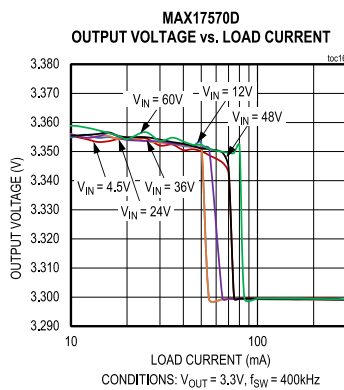
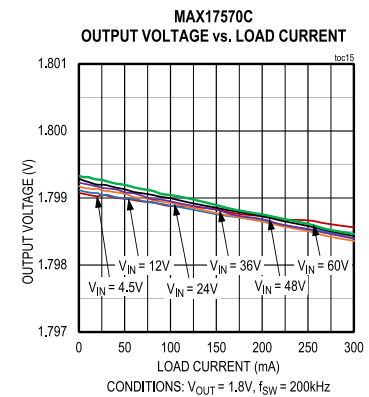
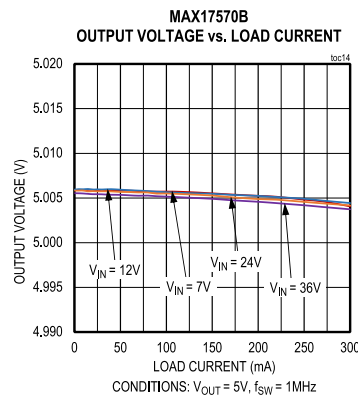
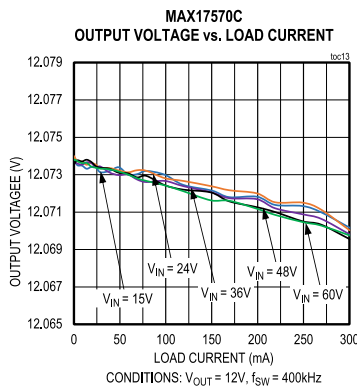
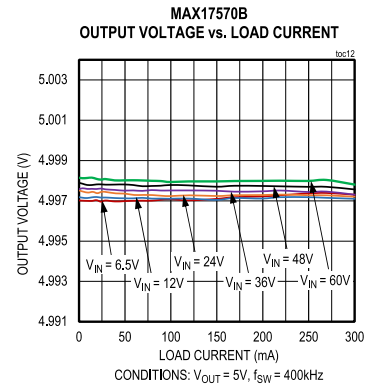
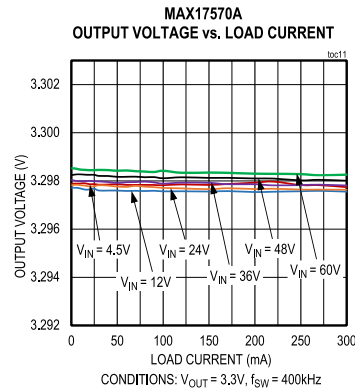
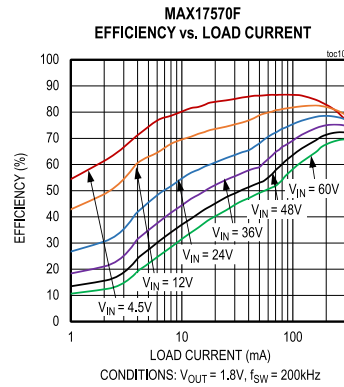
Typical Operating Characteristics

($V_{IN} = V_{EN/UVLO} = 24V$, $C_{IN} = C_{VCC} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



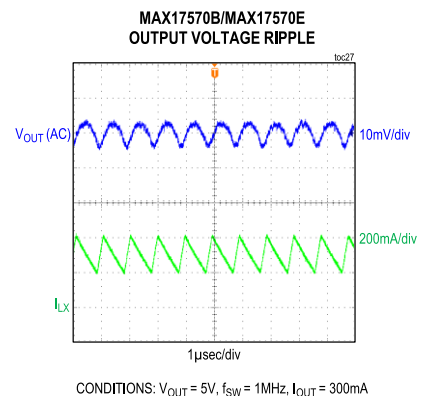
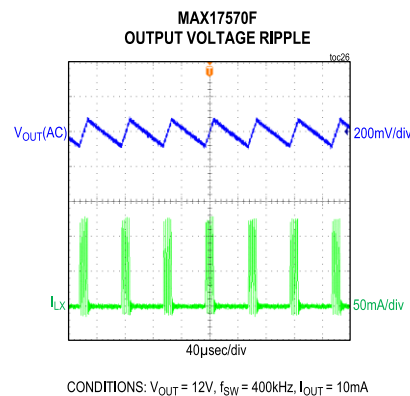
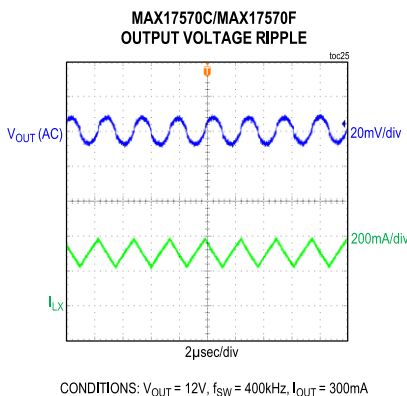
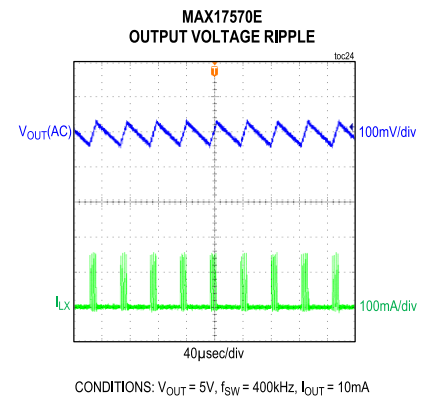
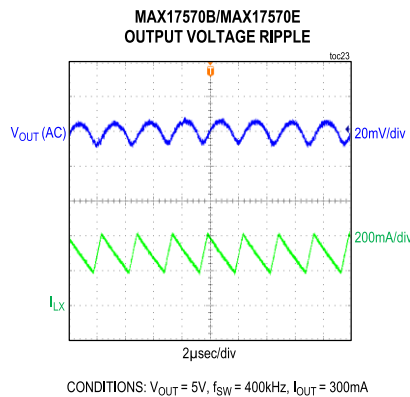
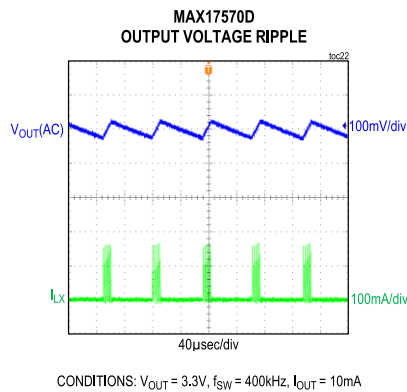
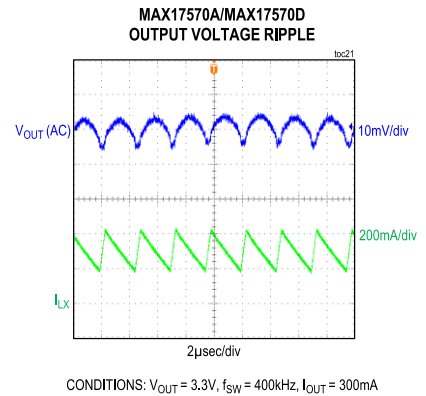
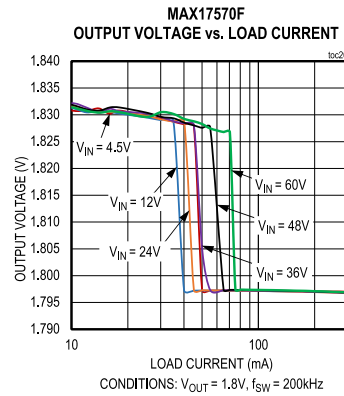
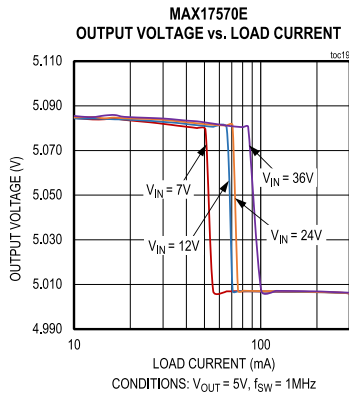
Typical Operating Characteristics (continued)

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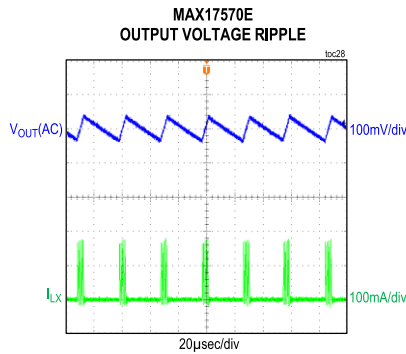
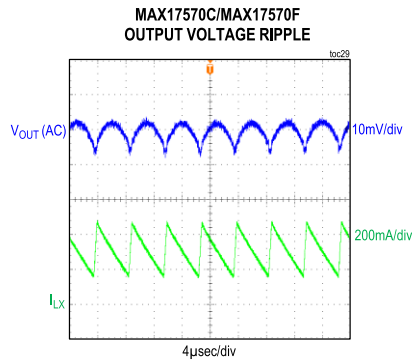
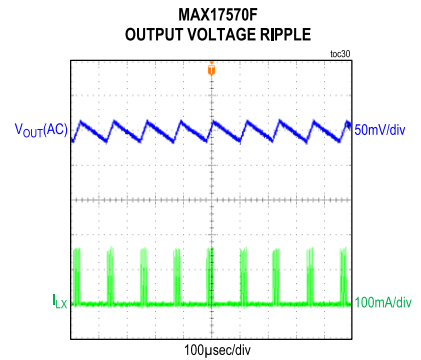
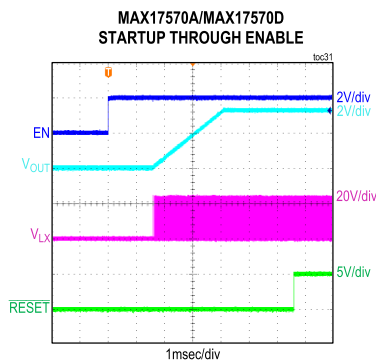
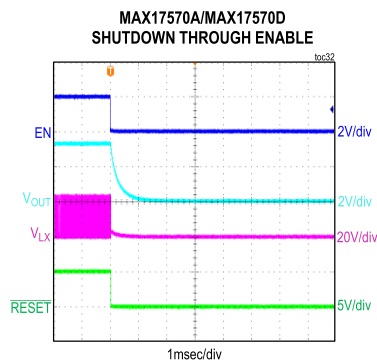
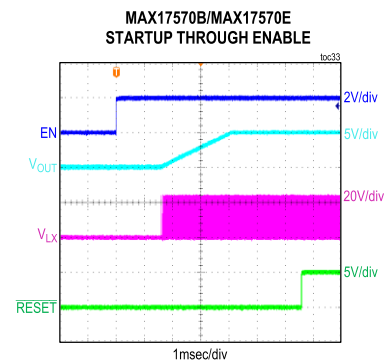
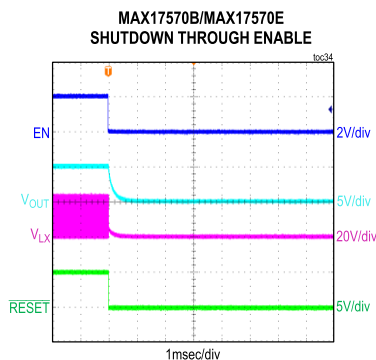
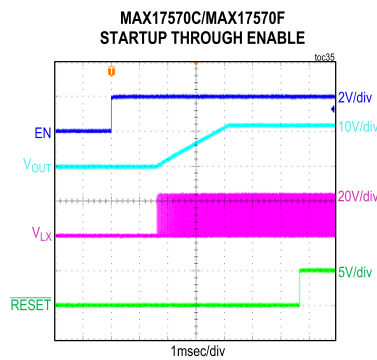
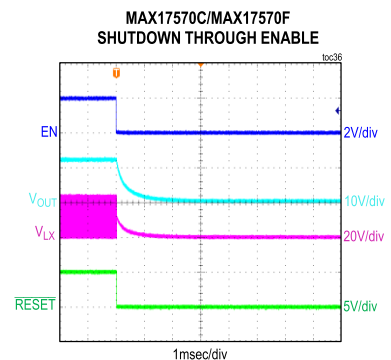


Typical Operating Characteristics (continued)

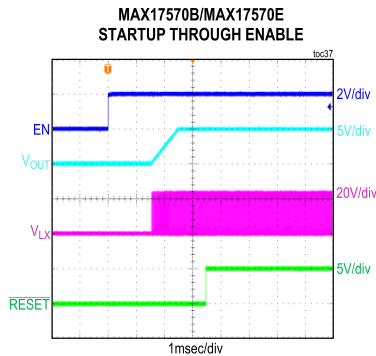
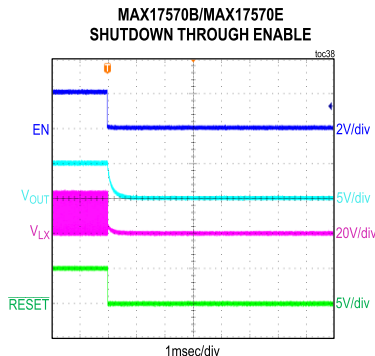
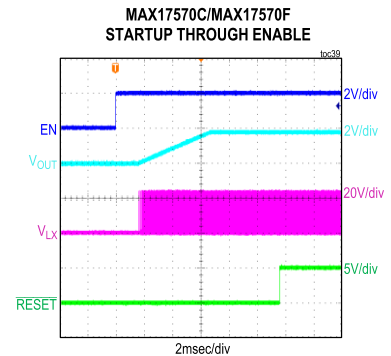
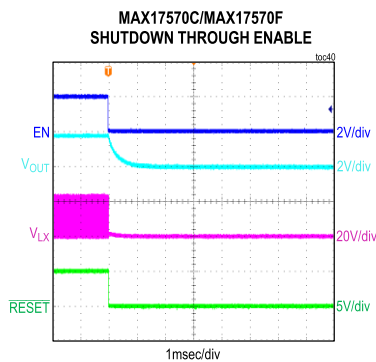
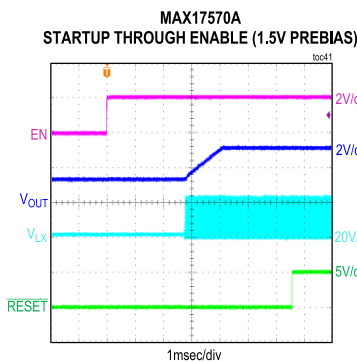
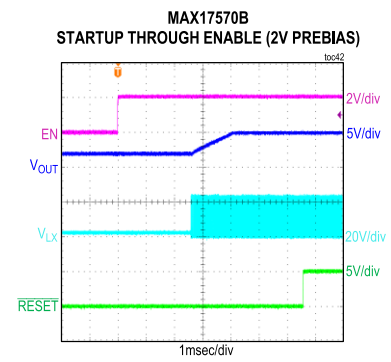
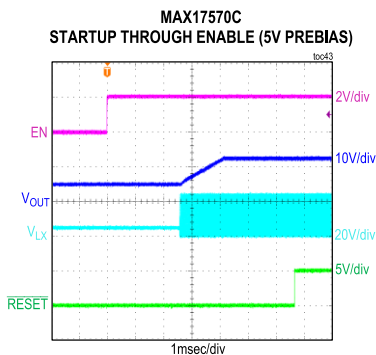
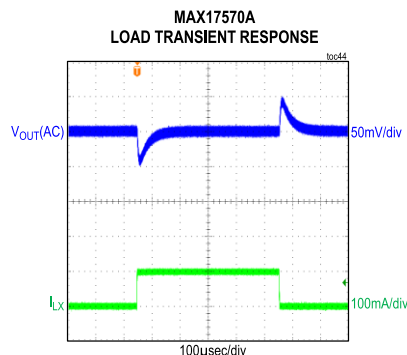
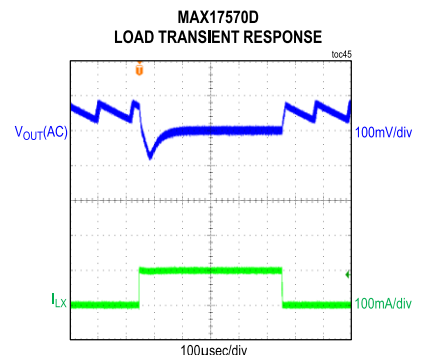
($V_{IN} = V_{EN/UVLO} = 24V$, $C_{IN} = C_{VCC} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

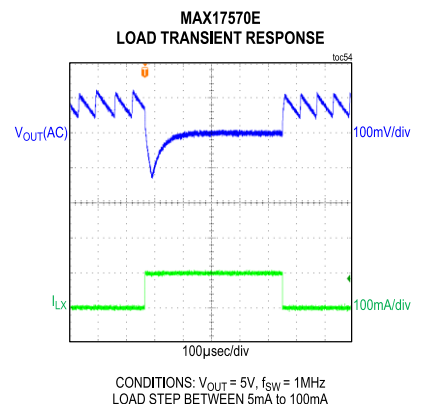
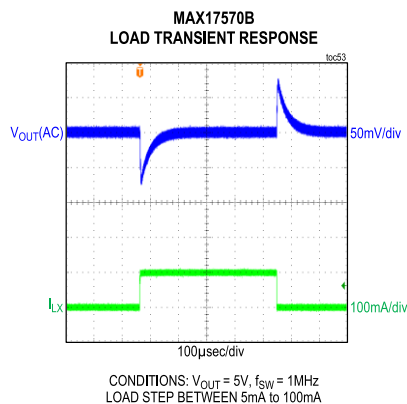
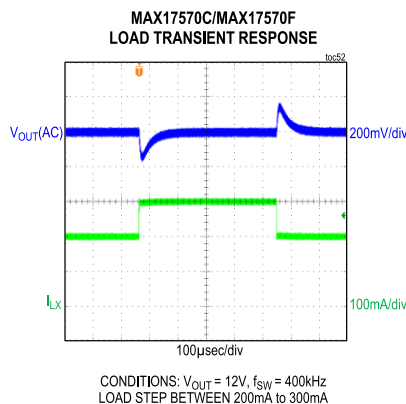
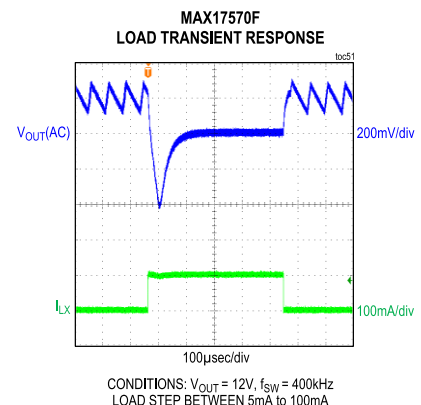
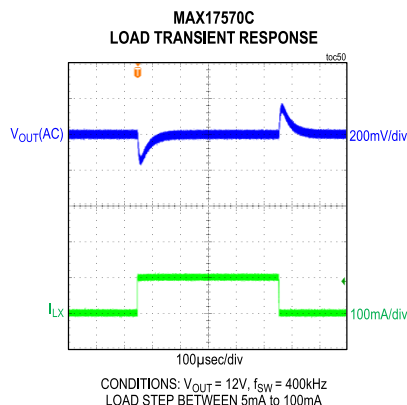
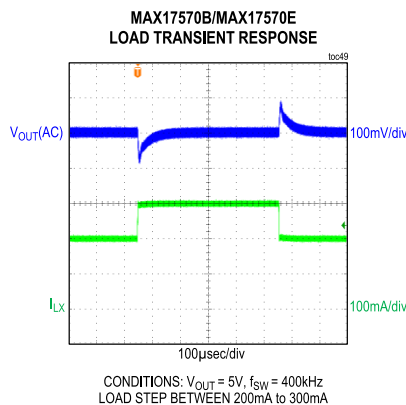
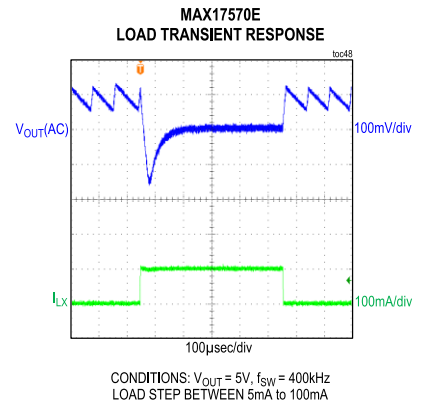
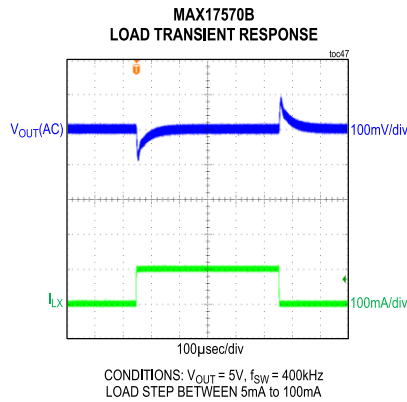
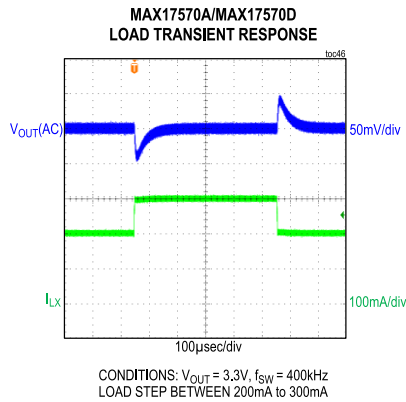
(V_{IN} = V_{EN/UVLO} = 24V, C_{IN} = C_{VCC} = 1μF, T_A = +25°C, unless otherwise noted.)CONDITIONS: V_{OUT} = 5V, f_{SW} = 1MHz, I_{OUT} = 10mACONDITIONS: V_{OUT} = 1.8V, f_{SW} = 200kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 1.8V, f_{SW} = 200kHz, I_{OUT} = 10mACONDITIONS: V_{OUT} = 3.3V, f_{SW} = 400kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 3.3V, f_{SW} = 400kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 5V, f_{SW} = 400kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 5V, f_{SW} = 400kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 12V, f_{SW} = 400kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 12V, f_{SW} = 400kHz, I_{OUT} = 300mA

Typical Operating Characteristics (continued)

(V_{IN} = V_{EN/UVLO} = 24V, C_{IN} = C_{VCC} = 1μF, T_A = +25°C, unless otherwise noted.)CONDITIONS: V_{OUT} = 5V, f_{SW} = 1MHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 5V, f_{SW} = 1MHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 1.8V, f_{SW} = 200kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 1.8V, f_{SW} = 200kHz, I_{OUT} = 300mACONDITIONS: V_{OUT} = 3.3V, f_{SW} = 400kHz, I_{OUT} = 10mACONDITIONS: V_{OUT} = 5V, f_{SW} = 400kHz, I_{OUT} = 10mACONDITIONS: V_{OUT} = 12V, f_{SW} = 400kHz, I_{OUT} = 10mACONDITIONS: V_{OUT} = 3.3V, f_{SW} = 400kHz
LOAD STEP BETWEEN 5mA TO 100mACONDITIONS: V_{OUT} = 3.3V, f_{SW} = 400kHz
LOAD STEP BETWEEN 5mA TO 100mA

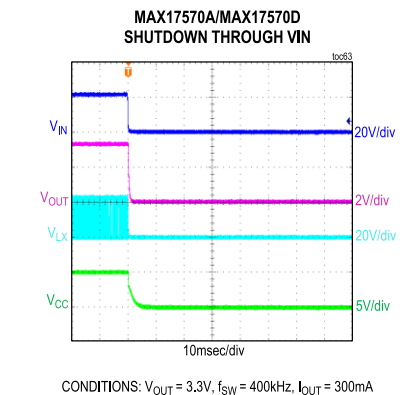
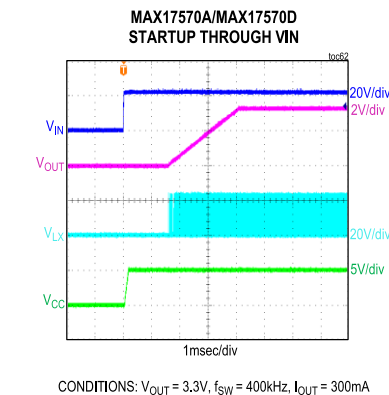
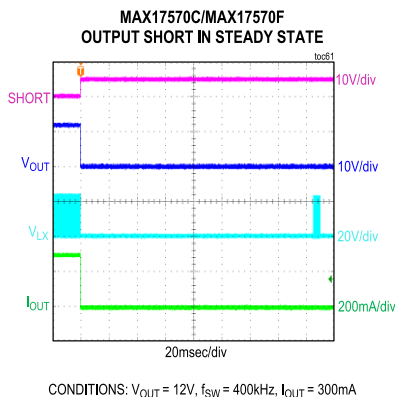
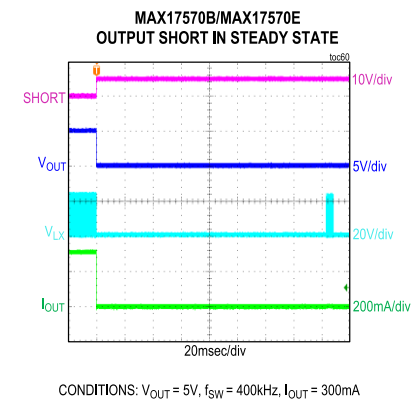
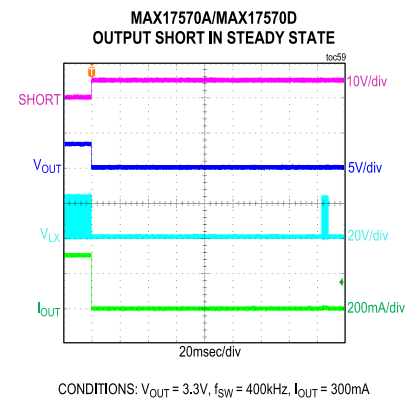
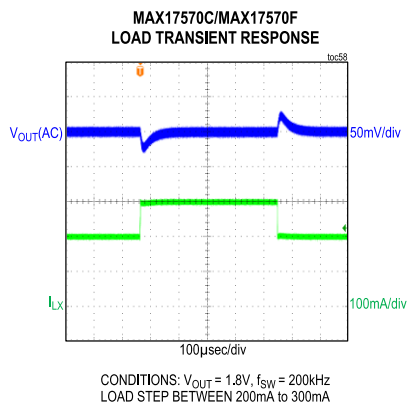
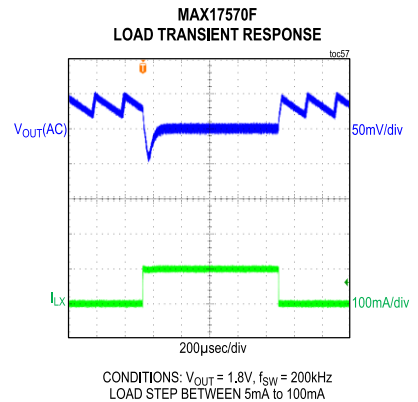
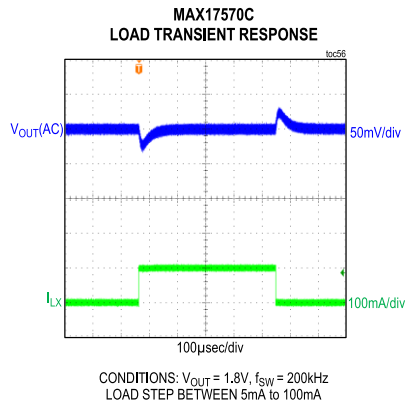
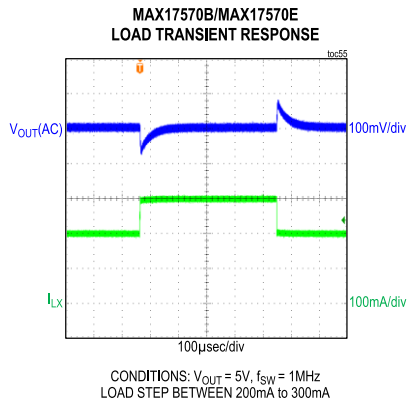
Typical Operating Characteristics (continued)

(VIN = VEN/UVLO = 24V, CIN = CVCC = 1μF, TA = +25°C, unless otherwise noted.)



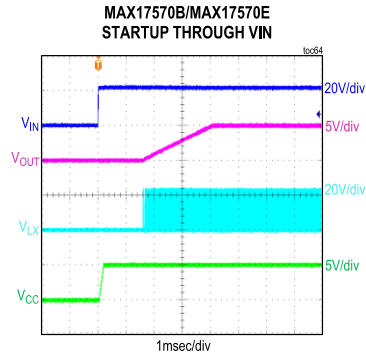
Typical Operating Characteristics (continued)

(VIN = VEN/UVLO = 24V, CIN = CVCC = 1μF, TA = +25°C, unless otherwise noted.)

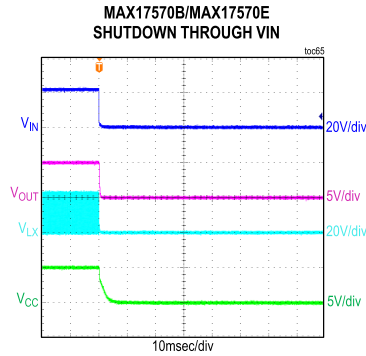


Typical Operating Characteristics (continued)

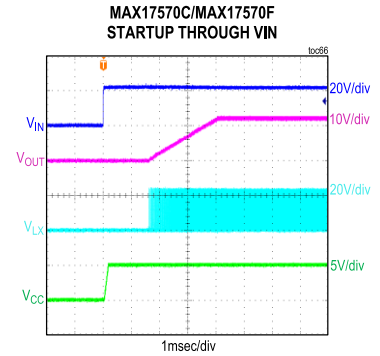
($V_{IN} = V_{EN/UVLO} = 24V$, $C_{IN} = C_{VCC} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



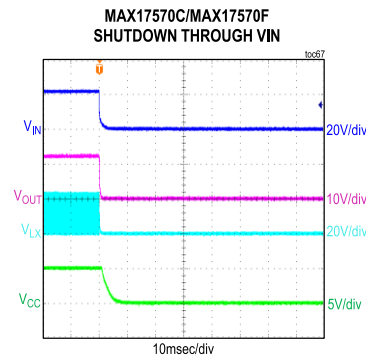
CONDITIONS: $V_{OUT} = 5V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$



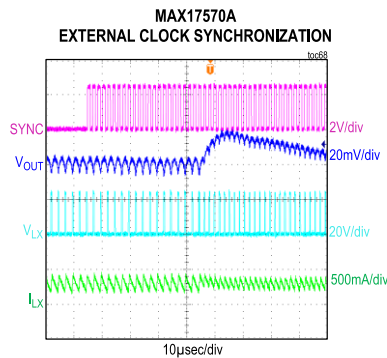
CONDITIONS: $V_{OUT} = 5V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$



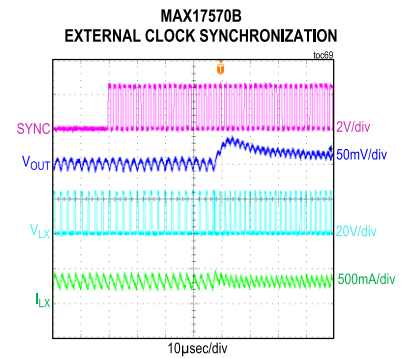
CONDITIONS: $V_{OUT} = 12V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$



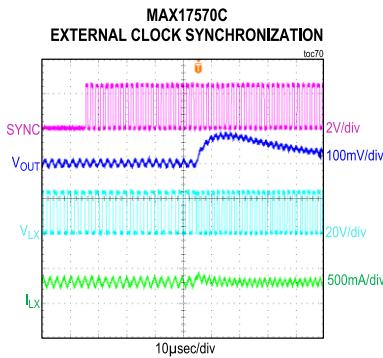
CONDITIONS: $V_{OUT} = 12V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$



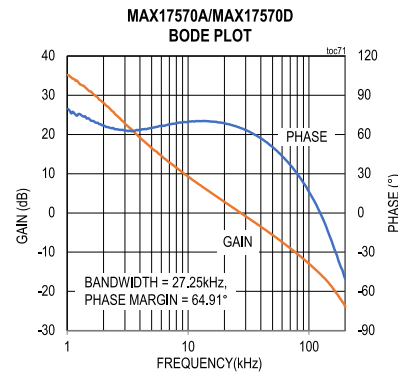
CONDITIONS: $V_{OUT} = 3.3V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$,
 $f_{SYNC} = 560kHz$



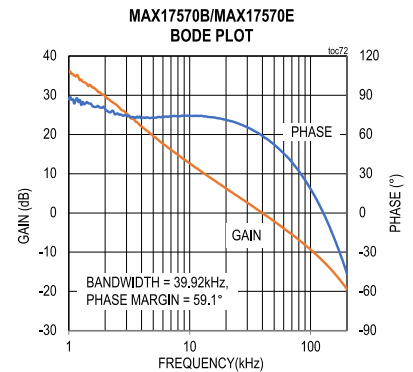
CONDITIONS: $V_{OUT} = 5V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$,
 $f_{SYNC} = 560kHz$



CONDITIONS: $V_{OUT} = 12V$, $f_{SW} = 400kHz$, $I_{OUT} = 300mA$,
 $f_{SYNC} = 560kHz$



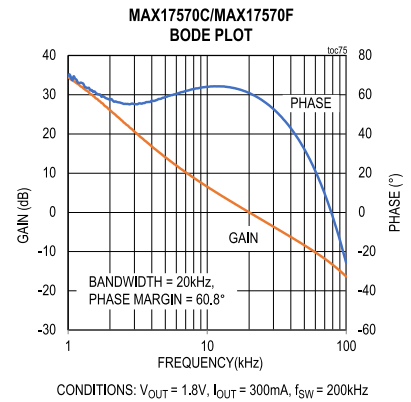
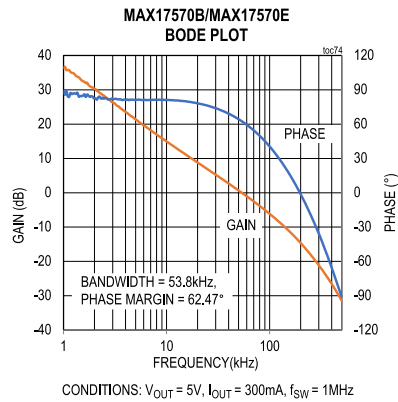
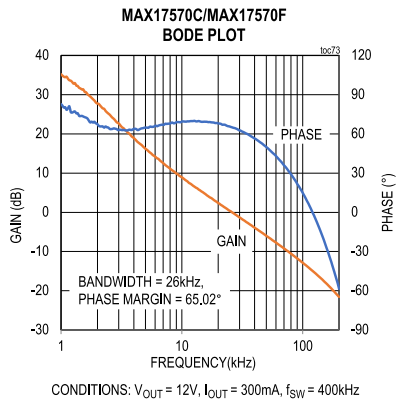
CONDITIONS: $V_{OUT} = 3.3V$, $I_{OUT} = 300mA$, $f_{SW} = 400kHz$



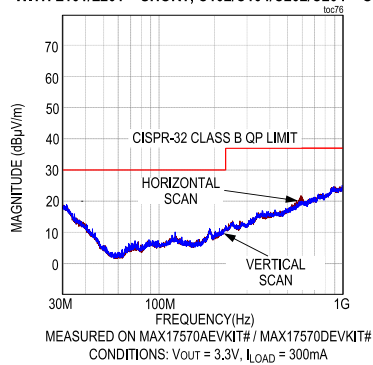
CONDITIONS: $V_{OUT} = 5V$, $I_{OUT} = 300mA$, $f_{SW} = 400kHz$

Typical Operating Characteristics (continued)

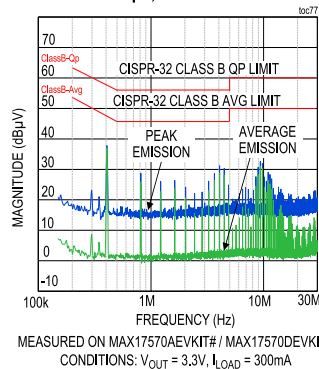
($V_{IN} = V_{EN/UVLO} = 24V$, $C_{IN} = C_{VCC} = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



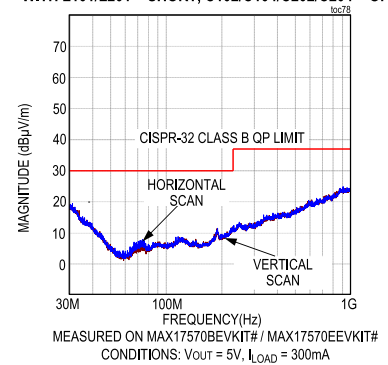
**MAX17570A/MAX17570D RADIATED EMISSIONS PLOT
WITH L101/L201 = SHORT, C102/C104/C202/C204 = OPEN**



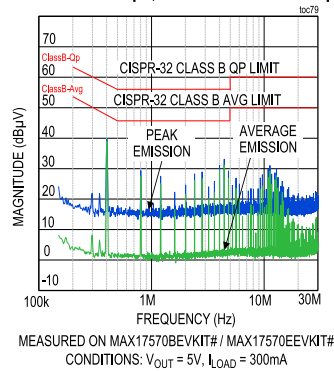
**MAX17570A/MAX17570D CONDUCTED EMISSIONS PLOT
WITH L101/L201 = 22μH, C102/C104/C202/C204 = 1μF**



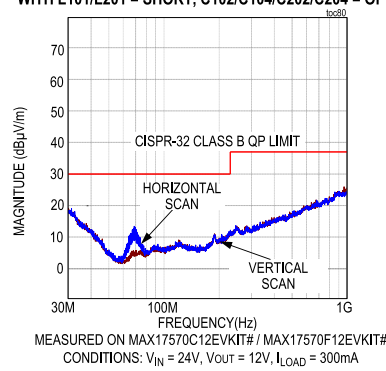
**MAX17570B/MAX17570E RADIATED EMISSIONS PLOT
WITH L101/L201 = SHORT, C102/C104/C202/C204 = OPEN**



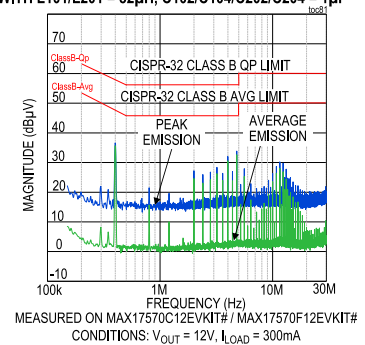
**MAX17570B/MAX17570E CONDUCTED EMISSIONS PLOT
WITH L101/L201 = 33μH, C102/C104/C202/C204 = 1μF**



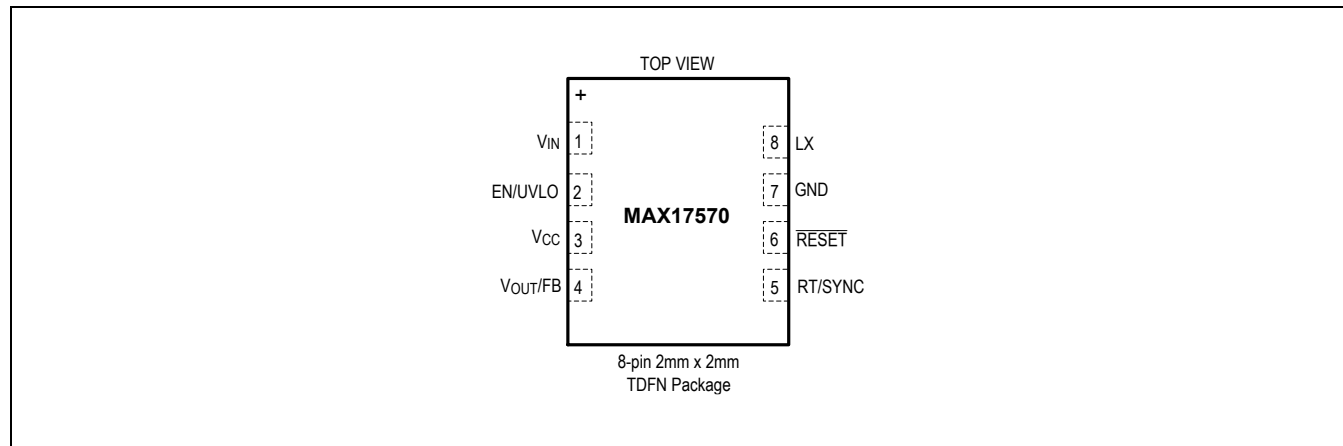
**MAX17570C/MAX17570F RADIATED EMISSIONS PLOT
WITH L101/L201 = SHORT, C102/C104/C202/C204 = OPEN**



**MAX17570C/MAX17570F CONDUCTED EMISSIONS PLOT
WITH L101/L201 = 82μH, C102/C104/C202/C204 = 1μF**



Pin Configurations



Pin Descriptions

| PIN | NAME | FUNCTION |
|-----|----------------------|---|
| 1 | V _{IN} | Switching Regulator Power Input. Connect a X7R 1μF ceramic capacitor from V _{IN} to GND for bypassing. |
| 2 | EN/UVLO | Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to V _{IN} for always on operation. Connect a resistor-divider between V _{IN} and EN/UVLO to GND to program the input voltage at which the device is enabled and turns on. |
| 3 | V _{CC} | Internal LDO Power Output. Bypass V _{CC} to GND with a minimum 1μF capacitor. |
| 4 | V _{OUT} /FB | Feedback Input. For fixed output voltage versions, connect V _{OUT} /FB directly to the output. For the adjustable output voltage version, connect V _{OUT} /FB to a resistor-divider between V _{OUT} and GND to adjust the output voltage from 0.9V to 0.97 x V _{IN} . |
| 5 | RT/SYNC | Oscillator Timing Resistor Input. Connect a resistor from RT to GND to program the switching frequency. Frequency can be programmed from 200kHz to 1MHz. The RT/SYNC can be used to synchronize the converter to an external clock. SYNC function is not available in the PFM parts (MAX17570D/E/F). For more details, see the Switching Frequency and Clock Synchronization section. |
| 6 | RESET | Open-Drain Reset Output. Pull up RESET to an external power supply with an external resistor. RESET goes low when the output voltage drops below 92% of the set nominal regulated voltage. RESET goes high impedance 1024 cycles after the output voltage rises above 95% of its regulation value. For threshold values, see the Electrical Characteristics table. |
| 7 | GND | Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. For more details, see the PCB Layout Guidelines section. |
| 8 | LX | Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown. |

Functional Diagram

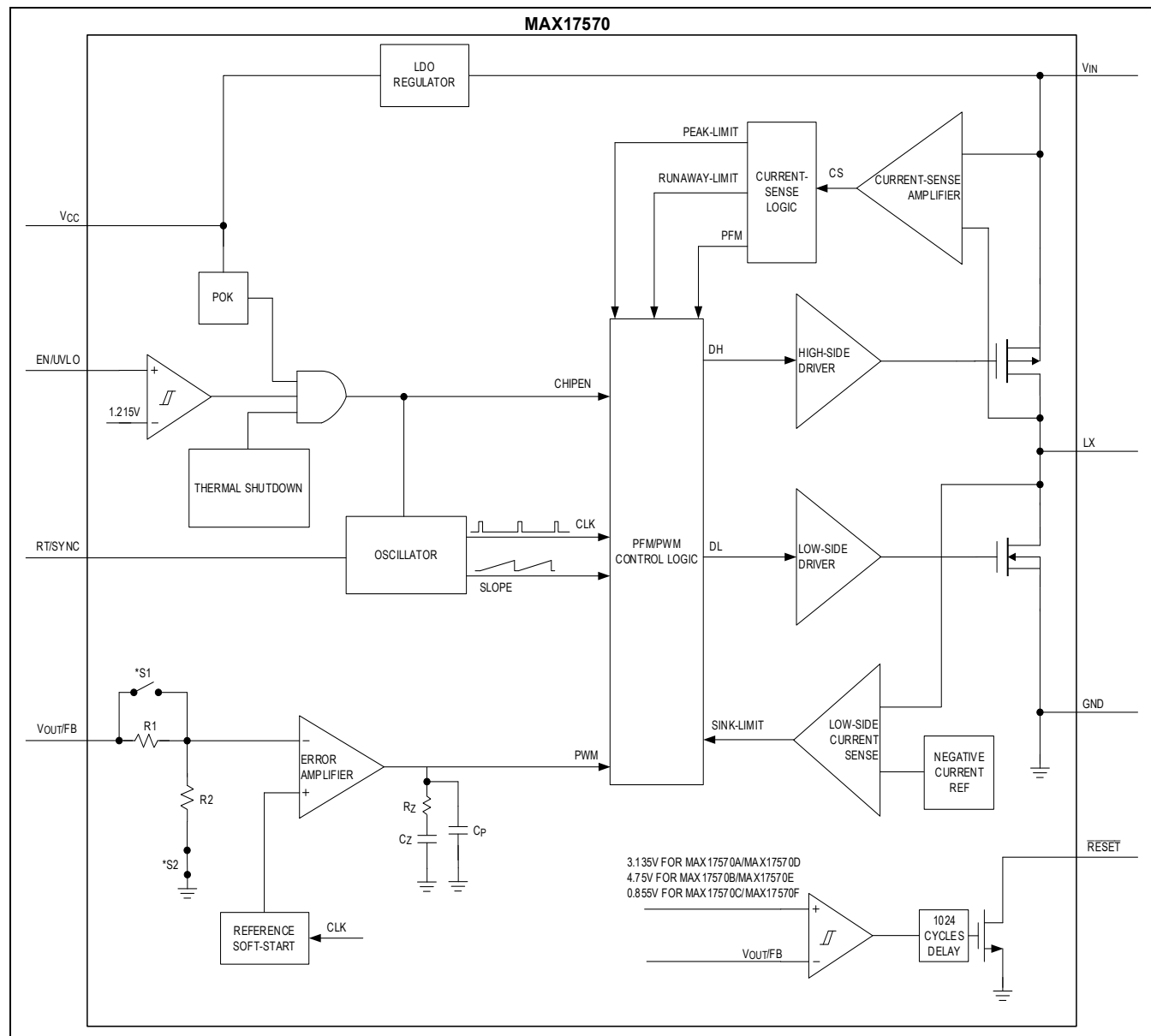


Table 1. Regulator Switch and Resistance Characteristics

| REGULATOR PART NUMBER | S1 | S2 | R1 (k Ω) | R2 (k Ω) |
|-----------------------|-------|-------|------------------|------------------|
| MAX17570A/D | OPEN | CLOSE | 206 | 77 |
| MAX17570B/E | OPEN | CLOSE | 352 | 77 |
| MAX17570C/F | CLOSE | OPEN | OPEN | OPEN |

Detailed Description

The MAX17570 is a high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a wide 4.5V to 60V input voltage range. The converter delivers output current up to 300mA at 3.3V (MAX17570A, MAX17570D), 5V (MAX17570B, MAX17570E), and adjustable output voltages (MAX17570C, MAX17570F). When EN/UVLO and V_{CC} UVLO are satisfied, an internal power-up sequence soft-starts the error-amplifier reference, resulting in a clean monotonic output-voltage soft-start independent of the load current. The V_{OUT}/FB pin monitors the output voltage through a resistor-divider. \overline{RESET} pin transitions to a high-impedance state 1024 cycles after the output voltage reaches 95% of regulation. By pulling the EN/UVLO pin to low, the device enters the shutdown mode and consumes only 2.2 μ A (typ) of standby current.

The MAX17570A/B/C operate in pulse-width modulation (PWM) mode at all loads and the MAX17570D/E/F operate in PFM mode at light loads. In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency sensitive applications and provides fixed switching frequency at all loads. In PFM mode, converter disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 150mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both high-side and low-side FETs are turned off and the part enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply.

DC-DC Switching Regulator

The device uses an internally compensated, fixed-frequency, current-mode control scheme (see the [Functional Diagram](#)). On the rising edge of an internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current-limit feature limits the inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Switching Frequency and Clock Synchronization

The switching frequency of the MAX17570 can be programmed from 200kHz to 1MHz with a resistor connected from the RT/SYNC pin to the GND. Calculate the value of the resistor at RT/SYNC pin (R_{RT}) for a required switching frequency (f_{SW}) using the following equation:

$$R_{RT/SYNC} = \frac{375}{\frac{16400}{f_{SW}} - 2.1}$$

Where $R_{RT/SYNC}$ is in k Ω and f_{SW} is in kHz. Leave the RT/SYNC pin open for a default f_{SW} of 400kHz. For $R_{RT/SYNC}$ resistor values for a few common switching frequencies, see [Table 2](#).

Table 2. Switching Frequency vs. R_{RT} Resistor

| SWITCHING FREQUENCY (kHz) | R_{RT} RESISTOR (k Ω) |
|---------------------------|---------------------------------|
| 400 | Open |
| 400 | 9.65 |
| 200 | 4.7 |
| 1000 | 26.4 |

The RT/SYNC pin can be used to synchronize the internal oscillator of the device to an external clock for the MAX17570A/B/C as shown in [Figure 1](#). The SYNC functionality is not available in PFM parts (MAX17570D/E/F). The

external clock frequency must be between $1.1 \times f_{SW}$ and $1.4 \times f_{SW}$, where f_{SW} is the switching frequency programmed by the resistor connected at the RT/SYNC pin. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to an external clock frequency after 16 internal oscillator cycles if at least 8 external clock cycles are applied. The pulse width of the external clock should be more than 100ns (t_{SYNC}) and the allowable duty cycle (D_{SYNC}) range is 10% to 90%.

The external clock signal is AC-coupled onto the RT/SYNC pin. The amplitude of the external clock ($V_{SYNC_PK_PK}$) should be chosen based on the following equations:

For $20\% \leq D_{SYNC} \leq 80\%$:

$$V_{SYNC_PK_PK} > 1.3V \text{ and } C_{SYNC} = \frac{45}{(V_{SYNC_PK_PK} - 1)}$$

For $10\% \leq D_{SYNC} < 20\%$:

$$V_{SYNC_PK_PK} > \frac{0.26}{D_{SYNC}},$$

$$C_{SYNC} = \frac{45}{(5 \times D_{SYNC} \times V_{SYNC_PK_PK}) - 1}$$

For $80\% < D_{SYNC} \leq 90\%$:

$$V_{SYNC_PK_PK} > \frac{0.26}{1 - D_{SYNC}},$$

$$C_{SYNC} = \frac{45}{(5 \times (1 - D_{SYNC}) \times V_{SYNC_PK_PK}) - 1}$$

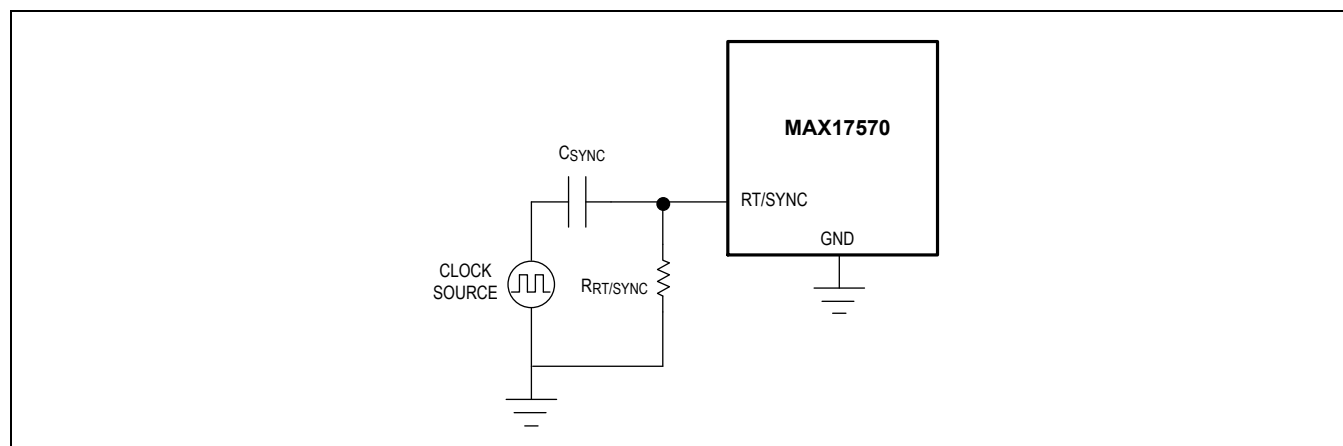


Figure 1. Synchronization to an External Clock

Internal 5V Linear Regulator

An internal regulator provides a 5V nominal supply to power the internal functions and to drive the power MOSFETs. The output of the linear regulator (V_{CC}) should be bypassed with a $1\mu F$ capacitor to GND. The V_{CC} regulator dropout voltage is typically 150mV. An undervoltage lockout circuit that disables the DC-DC synchronous converter when V_{CC} falls below 3.8V (typ). The 400mV (approximately) V_{CC} UVLO hysteresis prevents chattering on power-up and power-down.

Enable Input (EN/UVLO), Soft-Start

When EN/UVLO voltage is above 1.215V (typ), the device's internal error-amplifier reference voltage starts to ramp up. The duration of the soft-start ramp is 512 cycles at half the programmed switching frequency, allowing a smooth increase of the output voltage. The SS-Time variation with switching frequency is given by following equation:

$$\text{SS Time} = \frac{1024}{f_{\text{sw}}}$$

Where:

SS Time = Soft-Start Time in msec

f_{sw} = Switching Frequency in kHz

Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces V_{IN} quiescent current to below 2.2µA. EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between V_{IN} and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not required, connect EN/UVLO to V_{IN} (for EN/UVLO rising and falling threshold voltages, see the [Electrical Characteristics](#) table).

Reset Output (RESET)

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. When output rises above 95% of its nominal set value $\overline{\text{RESET}}$ goes to high impedance after 1024 cycles at the programmed switching frequency and pulls low when the output voltage falls below 92% of the set nominal regulated voltage. $\overline{\text{RESET}}$ asserts low during the hiccup timeout period.

Startup into a Prebiased Output

The device is capable of soft-start into a prebiased output, without discharging the output capacitor. Such feature is useful in applications where digital integrated circuits with multiple rails are powered.

Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{\text{INMIN}} = \frac{V_{\text{OUT}} + (I_{\text{OUT(MAX)}} \times (R_{\text{DCR(MAX)}} + R_{\text{DS-ONL(MAX)}}))}{1 - f_{\text{SW(MAX)}} \times t_{\text{OFF-MIN(MAX)}}} + I_{\text{OUT}} \times (R_{\text{DS-ONH(MAX)}} - R_{\text{DS-ONL(MAX)}})$$

$$V_{\text{INMAX}} = \frac{V_{\text{OUT}}}{t_{\text{ON-MIN(MAX)}} \times f_{\text{SW(MAX)}}}$$

Where:

V_{OUT} = Steady-state output voltage

$I_{\text{OUT(MAX)}}$ = Maximum load current

$R_{\text{DCR(MAX)}}$ = DC resistance of the inductor

$f_{\text{SW(MAX)}}$ = Switching frequency (maximum)

$t_{\text{OFF-MIN(MAX)}}$ = Worst case minimum controllable switch off-time (145ns)

$t_{\text{ON-MIN(MAX)}}$ = Worst case minimum controllable switch on-time (130ns)

$R_{\text{DS-ONH(MAX)}}$ = Worst case on-state resistances of high-side internal MOSFET

$R_{\text{DS-ONL(MAX)}}$ = Worst case on-state resistances of low-side internal MOSFET

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 0.56A (typ). A runaway current limit on the high-side switch current at 0.66A (typ) protects the device under high input voltage and short-circuit conditions when there is insufficient output voltage available to restore the inductor current that is built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 65% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32768 cycles at half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions. Care should be taken in board layout and system wiring to prevent violation of the absolute maximum rating of the V_{OUT}/FB pin under short-circuit conditions. Under such conditions, it is possible for the ceramic output capacitor to oscillate with the board or wiring inductance between the output capacitor or short-circuited load, thereby causing the absolute maximum rating of V_{OUT}/FB (-0.3V) to be exceeded. The parasitic board or wiring inductance should be minimized and the output voltage waveform under short-circuit operation should be verified to ensure the absolute maximum rating of V_{OUT}/FB is not exceeded.

Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 166°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by 20°C.

Applications Information

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough to ensure that saturation cannot occur below the maximum current-limit value. The required inductance for a given application can be determined from the following equation:

$$L = 3.7 \times \frac{V_{OUT}}{f_{SW}}$$

Where:

V_{OUT} = Output voltage

f_{SW} = Switching frequency in Hz

L = Inductance in H.

Once the L value is known, the next step is to select the right core material. Ferrite and powdered iron are commonly available core materials. Ferrite cores have low core losses and are preferred for high-efficiency designs. Powdered iron cores have more core losses and are relatively cheaper than ferrite cores.

Setting the Input Undervoltage Lockout Level

The devices offer an adjustable input undervoltage lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see [Figure 2](#)). Connect the center node of the divider to EN/UVLO. Choose $R1$ to be 3.3M Ω maximum, and then calculate $R2$ as follows:

$$R2 = \frac{R1 \times 1.215}{V_{INU} - 1.215}$$

Where V_{INU} is the voltage at which the device is required to turn on. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1k Ω is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

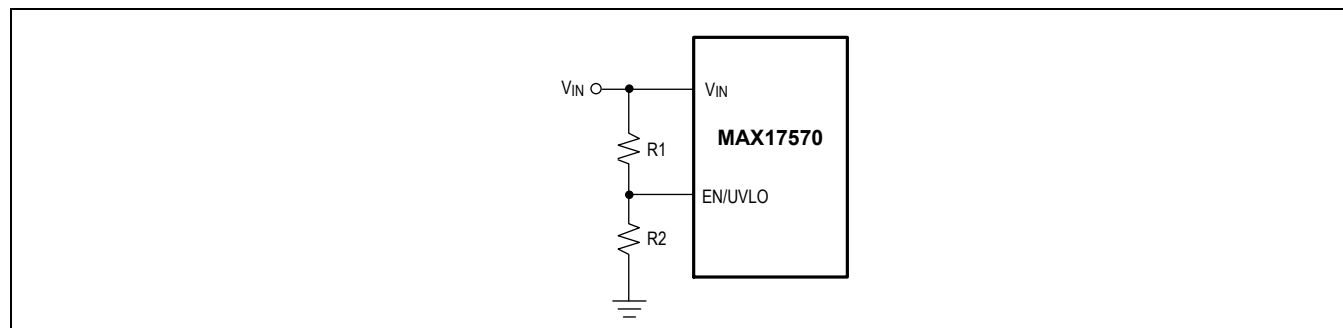


Figure 2. Adjustable EN/UVLO Network

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$C_{IN} = I_{OUT(MAX)} \times D \times \frac{1 - D}{\eta \times f_{SW} \times \Delta V_{IN}}$$

Where:

$D = V_{OUT}/V_{IN}$ is the duty ratio of the converter

f_{SW} = Switching frequency in Hz

ΔV_{IN} = Allowable input voltage ripple

η = efficiency

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended for the device. The output capacitor has two functions. It filters the square wave generated by the device along with the output inductor. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. Usually, the output capacitor is sized to support a step load of 33% of the maximum output current in the application, such that the output voltage deviation is less than 3%. Required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{1.16}{V_{OUT} \times f_C}$$

Where:

C_{OUT} = Output capacitance in F

V_{OUT} = Output voltage

f_C = Desired crossover frequency in Hz. f_C is chosen to be the lowest value between 1/12th of the switching frequency and 50kHz

Derating of ceramic capacitors with DC voltage at appropriate AC voltage (equal to the steady-state output voltage ripple) must be considered while selecting the output capacitor.

Adjusting the Output Voltage

The MAX17570C/F output voltage can be programmed from 0.9V to $0.97 \times V_{IN}$. Set the output voltage by connecting a resistor-divider from output to FB to GND (see [Figure 3](#)). For the output voltages less than 6V, choose R6 in the 50k Ω to 150k Ω range. For the output voltages greater than 6V, choose R6 in the 25k Ω to 75k Ω range and calculate R5 with the following equation.

$$R5 = R6 \left[\frac{V_{OUT}}{0.9} - 1 \right]$$

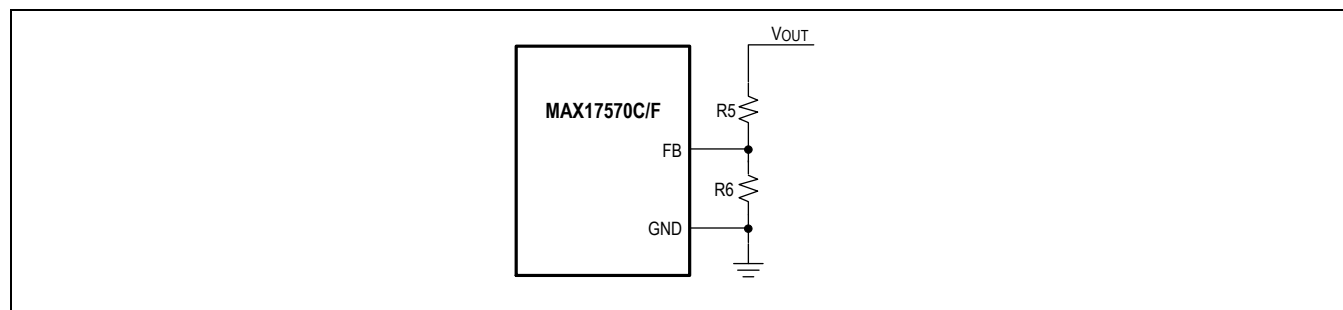


Figure 3. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{\text{LOSS}} = \left[P_{\text{OUT}} \times \left(\frac{1}{\eta} - 1 \right) \right] - (I_{\text{OUT}}^2 \times R_{\text{DCR}})$$

$$P_{\text{OUT}} = V_{\text{OUT}} \times I_{\text{OUT}}$$

Where:

P_{OUT} = Output power

η = Efficiency of the converter

R_{DCR} = DC resistance of the inductor

V_{OUT} = Output voltage

I_{OUT} = Output current

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{\text{LOSS}})$$

Where θ_{JA} is the junction-to-ambient thermal impedance of the package. Junction temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow the guidelines below for good PCB layout:

- Place the input ceramic capacitor as close as possible to the V_{IN} and GND pins.
- Connect the negative terminal of the V_{CC} bypass capacitor to the GND pin with shortest possible trace or ground plane.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Place the V_{CC} decoupling capacitor as close as possible to the V_{CC} pin.
- Ensure that all feedback connections are short and direct.
- Route the high-speed switching node (LX) away from the V_{OUT}/FB , $\overline{\text{RESET}}$, and RT pins.

For a sample PCB layout that ensures the first-pass success, refer to the MAX17570 evaluation kit layouts available at www.maximintegrated.com/MAX17570.

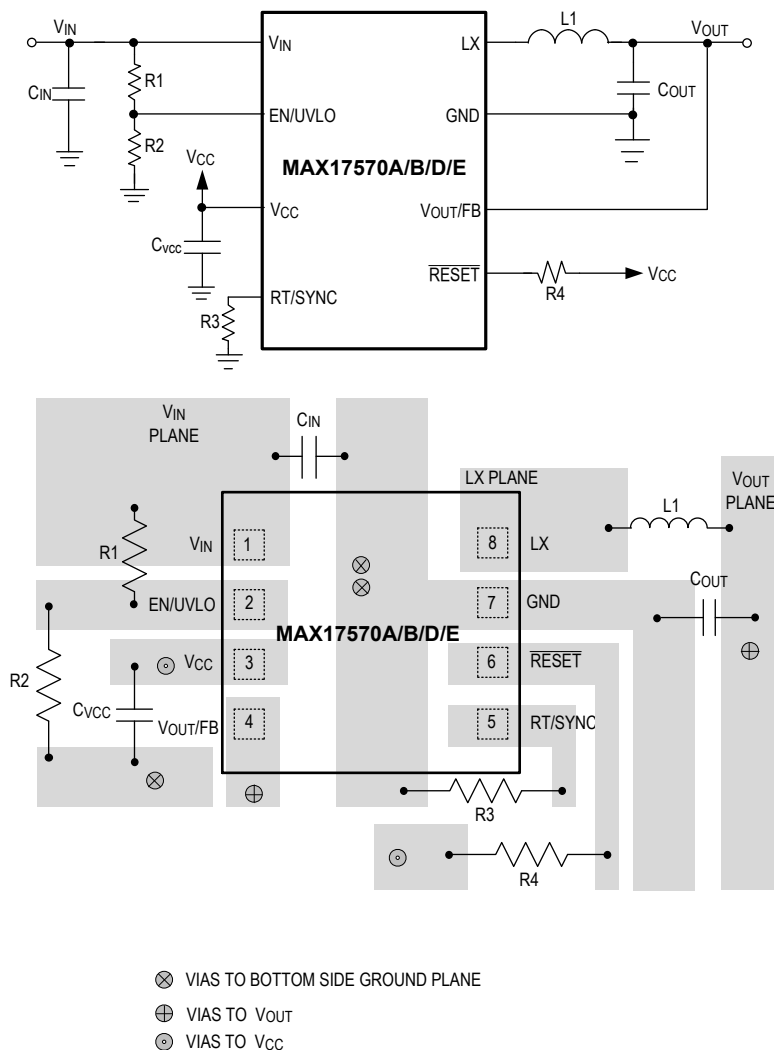


Figure 4. Layout Guidelines for MAX17570A/B/D/E

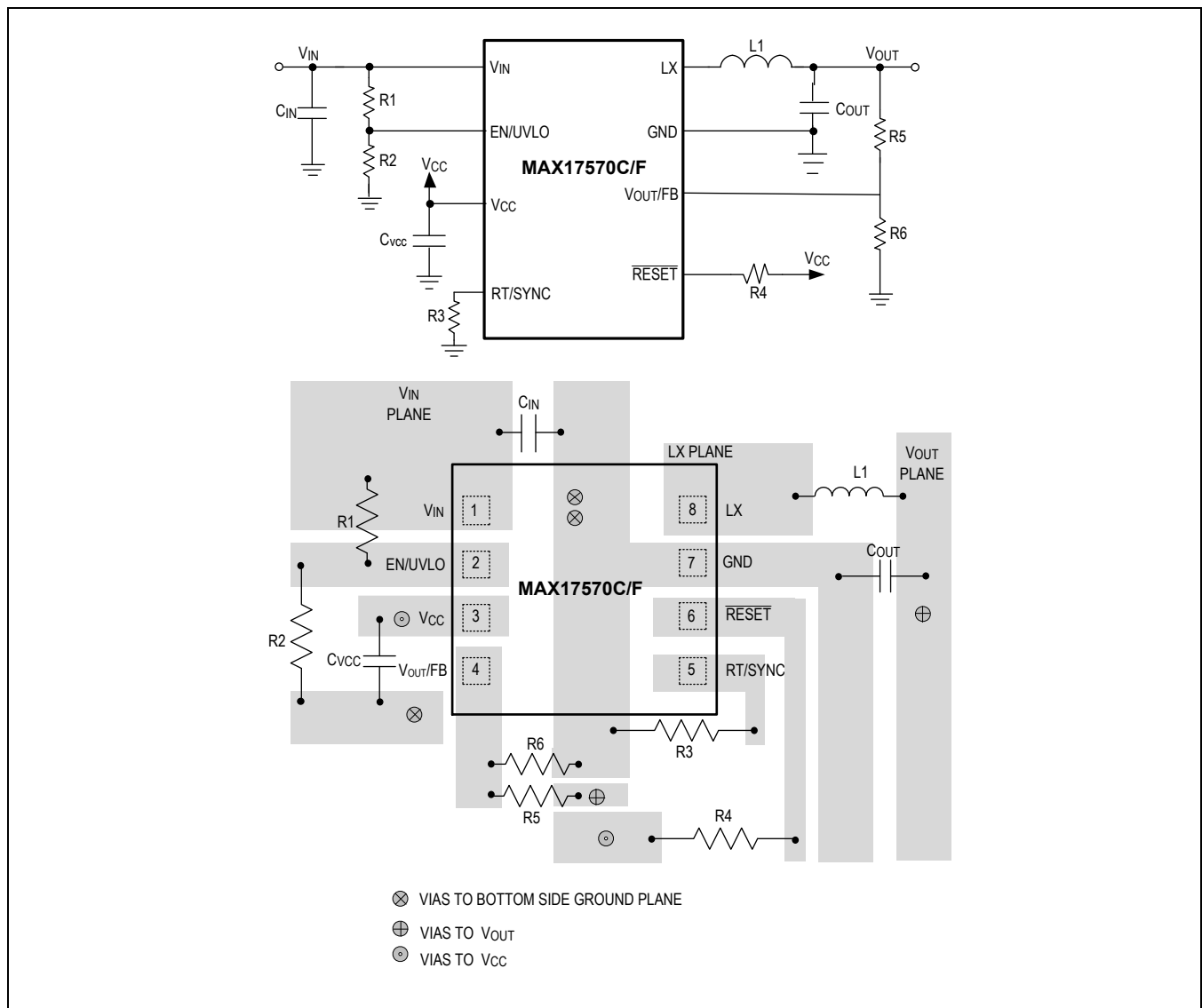


Figure 5. Layout Guidelines for MAX17570C/F

Typical Application Circuits

Typical Application Circuit for 3.3V Fixed, 400kHz

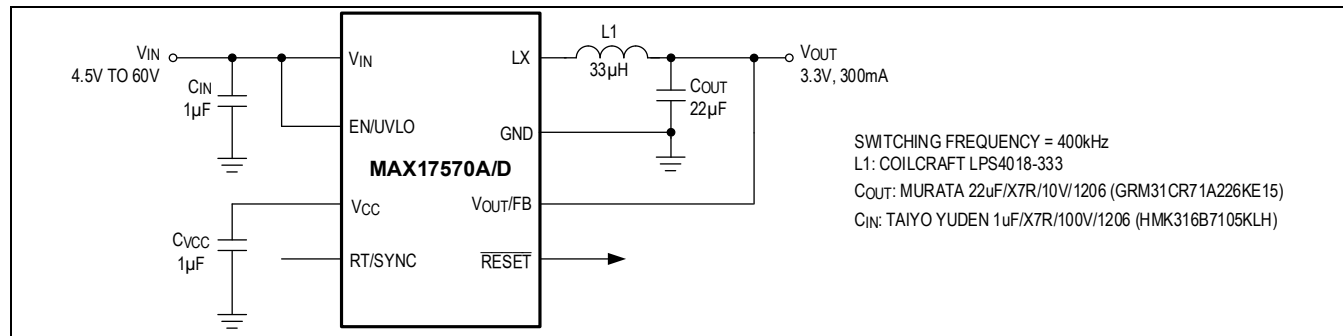


Figure 6. 3.3V Output with 400kHz Switching Frequency

Typical Application Circuit for 5V Fixed, 400kHz

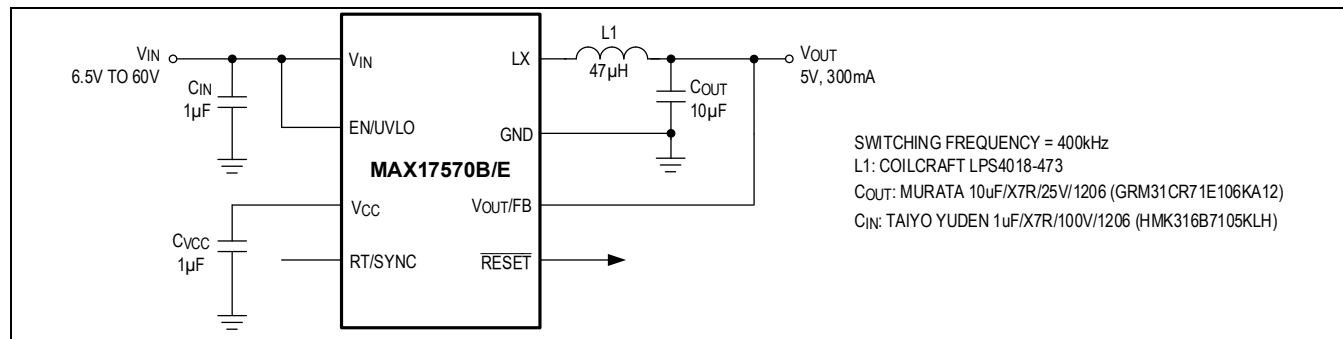


Figure 7. 5V Output with 400kHz Switching Frequency

Typical Application Circuit for 12V Adjustable, 400kHz

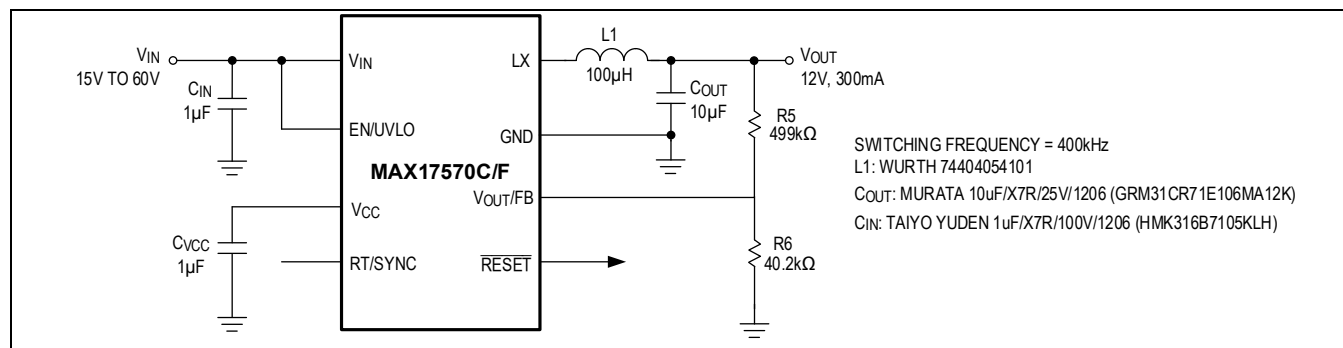


Figure 8. 12V Output with 400kHz Switching Frequency

Typical Application Circuit for 5V Fixed, 1MHz

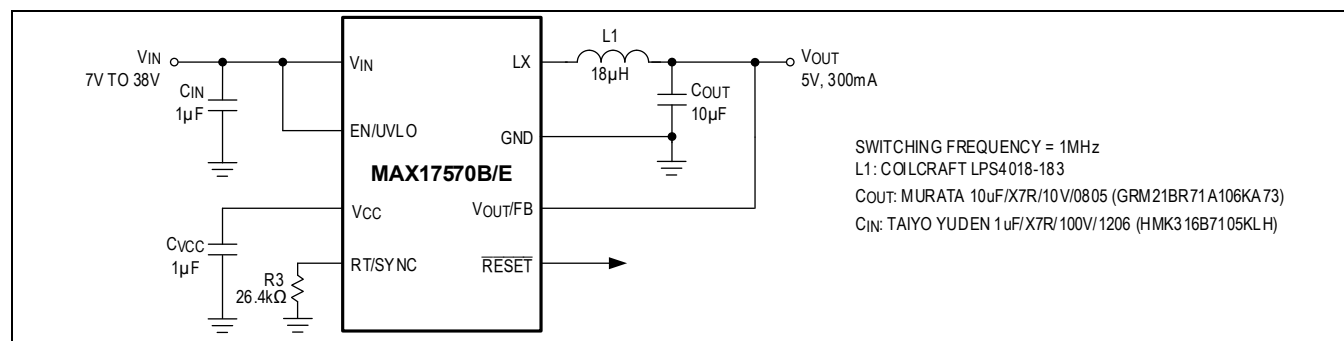


Figure 9. 5V Output with 1MHz Switching Frequency

Typical Application Circuit for 1.8V Adj, 200kHz

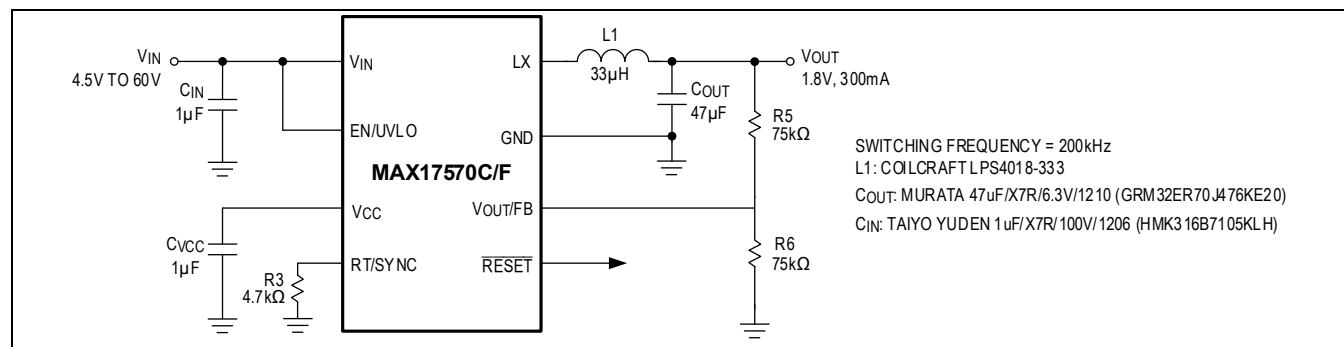


Figure 10. 1.8V Output with 200kHz Switching Frequency

Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE | V _{OUT} | MODE OF OPERATION |
|----------------|-----------------|----------------------|------------------|-------------------|
| MAX17570AATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 3.3 | PWM |
| MAX17570AATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 3.3 | PWM |
| MAX17570BATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 5 | PWM |
| MAX17570BATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 5 | PWM |
| MAX17570CATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | Adjustable | PWM |
| MAX17570CATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | Adjustable | PWM |
| MAX17570DATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 3.3 | PFM |
| MAX17570DATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 3.3 | PFM |
| MAX17570EATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 5 | PFM |
| MAX17570EATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | 5 | PFM |
| MAX17570FATA+ | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | Adjustable | PFM |
| MAX17570FATA+T | -40°C to +125°C | 8-pin TDFN 2mm x 2mm | Adjustable | PFM |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|---|------------------|
| 0 | 6/23 | Release for market intro | — |
| 1 | 7/23 | Updated TOC12, TOC17, TOC18, TOC41, TOC42, TOC43, TOC61, and TOC67 in <i>Typical Operating Characteristics</i> section | 7, 10, 12, 13 |

