Click here to ask an associate for production status of specific part numbers.

MAX15258

High-Voltage Multiphase Boost Controller with I²C Digital Interface

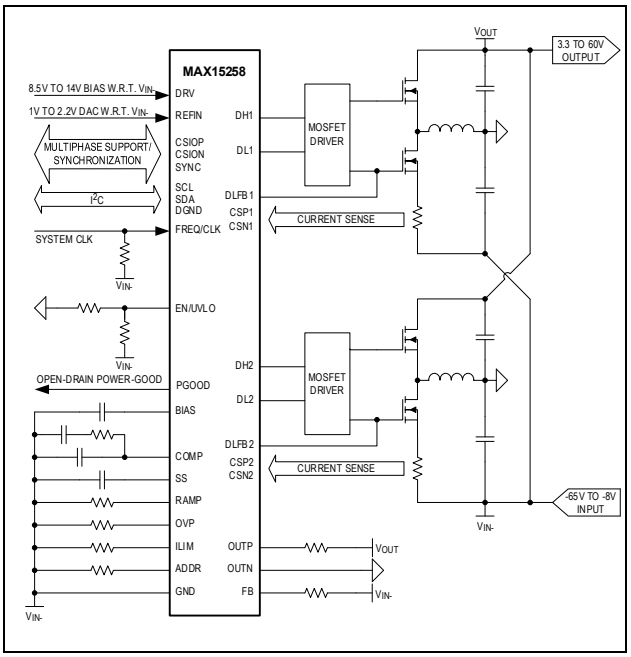
Product Highlights

- Wide Operating Range
  - 8V to 76V Input Voltage Range for Boost and -8V to -76V Input Voltage Range for Inverting-Buck-Boost Configuration
  - 3.3V to 60V Output Voltage Range on the Top of Input Voltage
  - Single-/Dual-/Triple-/Quad-Phase Operation
  - -40°C to +125°C Temperature Range
- I²C Digital Interface
  - Programmable Internal V_{REF}
  - Programmable Overcurrent Fault Limit
  - Readback for V_{IN}, V_{OUT}, and Phase Current Reporting
  - Fault Status
- Integration Reduces Design Footprint
  - Multiphase Multiple Controller Synchronization and Interleave
  - Output Voltage Sense Level Shifter

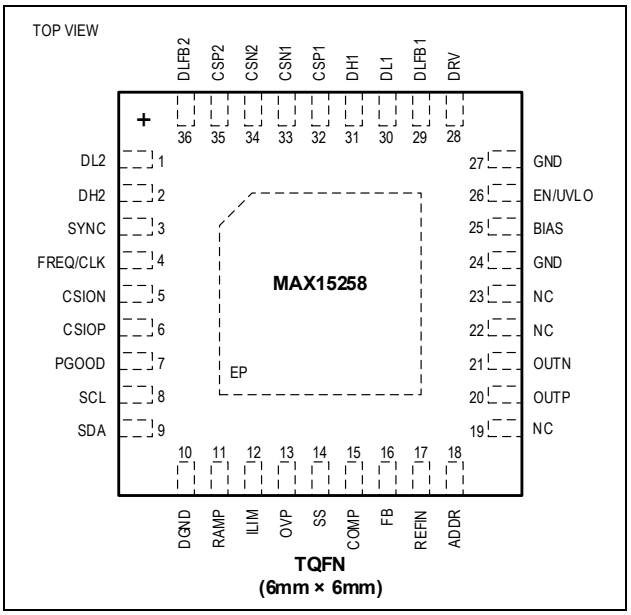
Key Applications

- Communications
- Industrial
- Multiphase Boost

Simplified Application Diagram



Pin Configuration



***Ordering Information* appears at the end of the data sheet.**

19-101557; Rev 1; 9/22

Absolute Maximum Ratings

OUTP, OUTN to GND ..... -0.3V to +80V
CSP_, CSN_ to GND ..... -0.3V to +0.3V
CSP_ to CSN_ ..... -0.3V to +0.3V
DH_, DL_ to GND ..... -0.3V to V_{BIAS} + 0.3V
DLFB_ to GND ..... -0.3V to V_{DRV} + 0.3V
DRV to GND ..... -0.3V to +16V
BIAS to GND ..... -0.3V to +6V
DRV to BIAS ..... -0.3V to +16V
FB, PGOOD, REFIN to GND ..... -0.3V to +6V
EN/UVLO, FREQ/CLK to GND ..... -0.3V to +6V
COMP, SS, ILIM to GND ..... -0.3V to V_{BIAS} + 0.3V
OVP, RAMP, SYNC to GND ..... -0.3V to V_{BIAS} + 0.3V
CSIOP, CSION to GND ..... -0.3V to V_{BIAS} + 0.3V
ADDR, SCL, SDA to GND ..... -0.3V to V_{BIAS} + 0.3V
DGND to GND ..... -0.3V to +0.3V
Maximum Current out of BIAS 100mA
Operating Temperature Range ..... -40°C to +125°C
Continuous Power Dissipation (T_A = +70°C) TQFN
(derate 35.7mW/°C above +70°C) 2.86W
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T3666+4C
Outline Number	*21-100560*
Land Pattern Number	*90-100199*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.
Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.
For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
DRV Operating Range	V_{DRV}		8.5		14	V
DRV Quiescent Current	I_{DRV}	Device switching, 2 phases, 10pF load at DH_ and DL_		10.3	16	mA
DRV Shutdown Current		EN/UVLO = GND		5.25	8	mA
DRV Undervoltage-Lockout Threshold	$V_{DRV(UVLO)}$	V_{DRV} rising	8.14	8.25	8.4	V
		V_{DRV} falling	8.04	8.15	8.27	
BIAS LINEAR REGULATOR						
BIAS LDO Output Voltage	V_{BIAS}	I_{BIAS} = 5mA	4.9	5	5.1	V
BIAS LDO Current Limit			35	58	88	mA
BIAS Undervoltage-Lockout Threshold	$V_{BIAS(UVLO)}$	V_{BIAS} rising	4.3	4.45	4.6	V
		V_{BIAS} falling	4.15	4.3	4.45	
CONTROLLER ENABLE						
EN/UVLO Adjustable Undervoltage-Lockout Threshold	V_{UVLO}	V_{UVLO} rising	0.98	1	1.025	V
		V_{UVLO} falling	0.88	0.9	0.925	
EN/UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to V_{BIAS}	-1		+1	µA
FEEDBACK VOLTAGE LEVEL SHIFTER (OUTP, OUTN)						
OUTP Current Range	I_{OUTP}	OUTP = OUTN > 8V, with high-voltage (HV) feedback (FB) level shifter enabled	0.05		3	mA
OUTN Bias Current	I_{OUTN}	OUTP = OUTN > 8V, with HV FB level shifter enabled		200	400	µA
OUTP, OUTN Leakage Current		OUTP = OUTN = 48V, with HV FB level shifter disabled		58	80	µA
OUTN Undervoltage-Lockout Threshold	OUTN UVLO	Minimum OUTN voltage for HV FB operation	7.05	7.2	7.35	V
		OUTN UVLO hysteresis	6.9	7	7.1	
HV FB Voltage-Buffer Operating Range	V_{OUTP}, V_{OUTN}		8		76	V
CONTROLLER LOOP						
FB Regulation Threshold (Preset Mode)	V_{FB}	REFIN = BIAS, VREF_COMMAND = 0x0000h	1.984	2	2.016	V
FB-to-REFIN Offset Voltage (Tracking Mode)		V_{FB} - V_{REFIN}, V_{REFIN} = 1V to 2.2V	-6		+6	mV
REFIN Input Voltage Range	V_{REFIN}	(*Note 2*)	1		2.2	V

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Preset Mode REFIN Threshold Rising		100mV hysteresis (typ)	2.34	2.36		V
FB Input Leakage Current	I_{FB}	V_{FB} = 0 to 2.2V, OUTP = OUTN = BIAS	-1		+1	µA
REFIN Input Leakage Current	I_{REFIN}	V_{REFIN} = 0.4V to 2.2V	-1		+1	µA
CSP_ to CSN_ Differential Voltage Range	$D_{VCS\_}$	$V_{CSP\_}$ - $V_{CSN\_}$	-200		+200	mV
Current-Sense Common-Mode Voltage Range	$V_{CSP\_}$, $V_{CSN\_}$	With respect to GND (*Note 3*)	-300		+300	mV
CSP_, CSN_ Current-Sense Amplifier Gain	$A_{CS\_}$		4.15	4.4	4.6	V/V
CSP_, CSN_ Input Leakage Current	$I_{CSP\_}$, $I_{CSN\_}$	$V_{CSP\_}$, $V_{CSN\_}$ = ±100mV, with respect to GND	-1		+1	µA
Error Amplifier Transconductance	G_{MEA}		0.8	1.15	1.5	mS
RAMP Amplitude Adjustable Range	V_{RAMP}		120		730	mV
Internal Slope Compensation Ramp Voltage to V_{RAMP} Ratio		V_{RAMP} = 0.3V	1.8	2	2.25	V/V
RAMP Bias Current	I_{RAMP}	V_{RAMP} = 0V	9.6	10	10.4	µA
SWITCHING FREQUENCY						
Preset PWM Switching Frequency	f_{SW}	R_{FREQ} = OPEN	293	300	305	kHz
Adjustable PWM Switching Frequency	f_{SW}	R_{FREQ} = 20kΩ	105	115	125	kHz
		R_{FREQ} = 25kΩ	140	148	154	
		R_{FREQ} = 100kΩ (R_{FREQ} < 100kΩ)	570	600	625	
PWM Switching Frequency Range	f_{SW}	FREQ/CLK externally applied	120		1000	kHz
FREQ/CLK Frequency Detection Range	f_{CLK}		0.36		4	MHz
FREQ/CLK Logic Level	V_{CLK}	Logic-high (rising)		1.8	1.9	V
		Logic-low (falling)	1.5	1.6		
FREQ/CLK Bias Current	I_{CLK}	$V_{FREQ/CLK}$ = GND	9.75	10	10.2	µA
FREQ/CLK to PWM Switching Frequency Ratio	f_{CLK}/f_{SW}	1-/2-/4-phase operation		4		kHz/kHz
		3-phase operation		3		
SYNCHRONIZATION						
SYNC Logic Threshold	V_{SYNC}	Logic-high (rising)		1.58	1.95	V
		Logic-low (falling)	0.9	1.15		
SYNC Input Resistance	R_{SYNC}			5		MΩ

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Range	f_{SYNC}		120		2000	kHz
SYNC Output Voltage Level	V_{SYNC}	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} - 0.4			V
		Logic-low, I_{SINK} = 10mA			0.2	
OUTPUT FAULT PROTECTION						
ILIM Adjustable Range	V_{ILIM}		0.2		1	V
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} = 0V, OC_FAULT_LIMIT = 0x00h	16	20	23	mV
		OC_FAULT_LIMIT = 0x01h		20		
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} > 1.25V, OC_FAULT_LIMIT = 0x00h	94	100	106	mV
		OC_FAULT_LIMIT = 0xFFh		100		
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Negative Peak Current Limit		V_{ILIM} > 1.25V, OC_FAULT_LIMIT = 0x00h	-90	-80	-66	mV
		OC_FAULT_LIMIT = 0xFFh		-80		
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Negative Peak Current Limit		V_{ILIM} = 0V, OC_FAULT_LIMIT = 0x00h	-20	-16	-10	mV
		OC_FAULT_LIMIT = 0x01h		-16		
CSP_ to CSN_ Minimum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} = 0V, OC_FAULT_LIMIT = 0x00h	21	26	31	mV
		OC_FAULT_LIMIT = 0x01h		26		
CSP_ to CSN_ Maximum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} > 1.25V, OC_FAULT_LIMIT = 0x00h	120	133	145	mV
		OC_FAULT_LIMIT = 0xFFh		133		
ILIM Source Current			9.7	10	10.3	µA
CSP_ to CSN_ Cycle-by-Cycle Positive Peak Current-Limit Threshold Accuracy		0.25V < V_{ILIM} < 0.95V, OC_FAULT_LIMIT = 0x00h	-10		+10	%
		V_{ILIM} = 500mV, OC_FAULT_LIMIT = 0x00h	-3		+3	
CSP_ to CSN_ Negative Overcurrent Protection Threshold Accuracy		V_{ILIM} = 500mV, OC_FAULT_LIMIT = 0x00h	-16		+16	%
V_{ILIM} to |CSP_ - CSN_| Cycle-by-Cycle Positive Peak Current-Limit Threshold Ratio		V_{ILIM} = 500mV, OC_FAULT_LIMIT = 0x00h		10		V/V

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum REFIN and SS Voltage for Valid FB OV Fault		Rising, 80mV hysteresis (typ)	1	1.02	1.04	V
FB Overvoltage Default Threshold (Preset Mode)	FB OV	Measured with respect to target voltage (REFIN = BIAS, VREF_COMMAND = 0x0000h), V_{FB} falling, 3% hysteresis	9	10	11.3	%
FB Overvoltage Threshold (Tracking Mode)	FB OV	Measured with respect to target voltage (REFIN = 1V, VREF_COMMAND = 0x0000h), V_{FB} falling, 3% hysteresis	9	10	11	%
OVP Selector Output Source Current		Resistor connected to GND	9.6	10	10.3	µA
Fault Propagation Delay		EN/UVLO falling to SS falling		32		µs
		EN/UVLO rising to SS rising		12		
		Cumulative cycle-by-cycle peak current limit or negative overcurrent protection events for hiccup		31		events
		FB OV		128		PWM CLK cycles
Hiccup Timeout Duration				32,768		PWM CLK cycles
Thermal Shutdown	T_{SHDN}	15°C hysteresis		165		°C
PGOOD						
PGOOD Threshold (Preset Mode)		PGOOD rising (REFIN = BIAS, VREF_COMMAND = 0x0000h)	1.86	1.88	1.9	V
		PGOOD falling (REFIN = BIAS, VREF_COMMAND = 0x0000h)	1.8	1.82	1.84	
PGOOD Threshold (Tracking Mode)		PGOOD rising	92.5	94	95	%
		PGOOD falling	90	91	92	
PGOOD Falling and Rising Delay				64		PWM CLK cycles
PGOOD Output Low Voltage	V_{PGOOD}	I_{SINK} = 3mA		20	40	mV
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN, V_{PGOOD} = 5V			1	µA
SOFT-START (SS)						
SS Amplifier Transconductance	$G_{M(SS)}$		0.1	0.2	0.3	mS
SS Current Capability	I_{SS}	Source	4.48	5	5.4	µA
		Sink	-5.4	-5	-4.8	
SS Pull-Down Resistance	R_{SS}	Discharge		4.3	7	Ω

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.2V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SS Undervoltage-Lockout Threshold	$V_{UVLO(SS)}$	SS rising (10mV hysteresis, typ)		53		mV
PWM OUTPUT						
DH_ Output Voltage Level	$V_{DH\_}$	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} - 0.4			V
		Logic-low, I_{SINK} = 10mA			0.2	
DL_ Output Voltage Level	$V_{DL\_}$	Logic-high, I_{SOURCE} = 20mA	V_{BIAS} - 0.4			V
		Logic-low, I_{SINK} = 20mA			0.2	
DH_ Minimum On-Time	$t_{ON\_DH\_}$		75	100	135	ns
DH_ Minimum Off-Time	$t_{OFF\_DH\_}$			55	160	ns
DL_ Minimum On-Time	$t_{ON\_DL\_}$			40	60	ns
DLFB_ Leakage Current	I_{LK}	$V_{DLFB\_}$ = 9V	-1		+1	µA
DLFB_ Logic Threshold	$V_{DLFB\_}$	Logic-high (rising)	0.75	0.8	0.85	V
		Logic-low (falling)	0.45	0.5	0.55	
CURRENT SHARING (MULTIPHASE APPLICATIONS ONLY)						
CSION Output Common-Mode Voltage	V_{CSION}	With respect to GND		1.228		V
CSIO_ Differential Input Resistance	$R_{CSIO\_}$			4		kΩ
I²C DIGITAL INTERFACE						
SDA, SCL Logic Threshold	V_{BUS_IL}	Logic-low (falling)			1.5	V
	V_{BUS_IH}	Logic-high (rising)	2.7			
SDA, SCL Leakage Current		V_{SCL}, V_{SDA} = 0V, V_{BIAS}			1	µA
SDA, SCL Pin Capacitance					2	pF
SDA Output Logic-Low		Sinking 20mA			0.2	V
ADDR Selector Output Source Current		Resistor connected to GND	9.7	10	10.3	µA
I²C TELEMETRY						
System ADC Resolution				10		bits
System ADC Update Rate				3.2		ms
Telemetry Error	READ_FB	READ_FB vs. measurement at FB pin, V_{FB} = 2V	-2.5		+2.5	%
	READ_OUTN	READ_OUTN vs. measurement at OUTN pin, V_{OUTN} = 48V	-2		+2	
	READ_IPH_	$V_{CSP\_ - CSN\_}$ = 50mV, duty cycle = 50%	-10		+10	

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

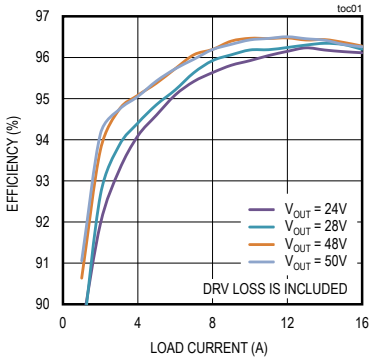
Note 2: Operating REFIN below 1V is not recommended due to disabled FB overvoltage-fault protection.

Note 3: Guaranteed by design, not production tested.

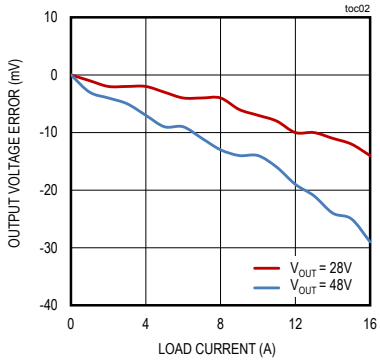
Typical Operating Characteristics

(T_A = +25°C, V_{IN-} = -48V, V_{OUT} = 48V, unless otherwise noted. See the *Typical Application Circuits*.)

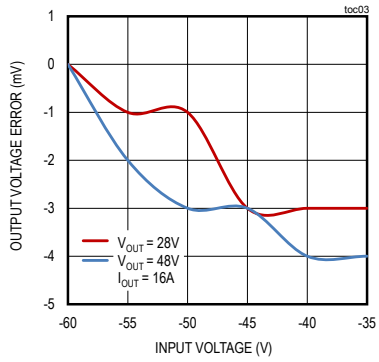
EFFICIENCY vs. OUTPUT LOAD



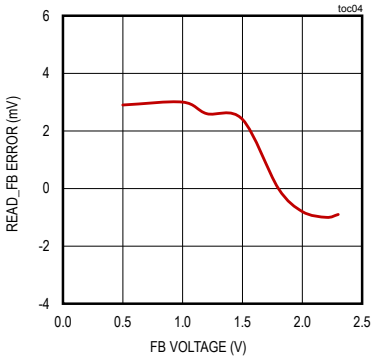
LOAD REGULATION



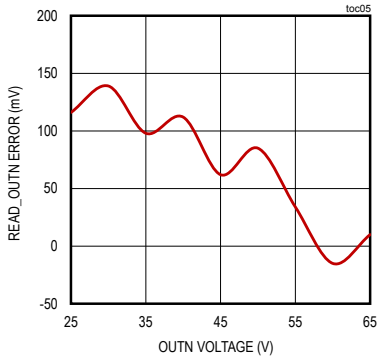
LINE REGULATION



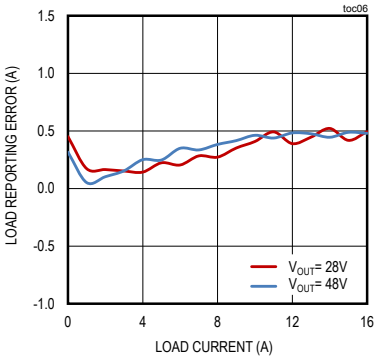
READ_FB vs. FB VOLTAGE



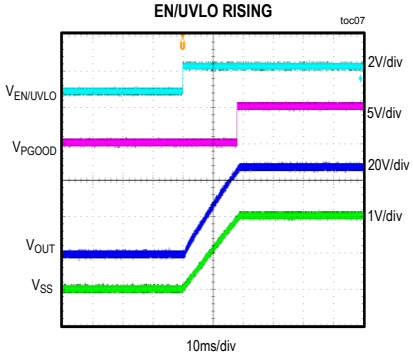
READ_OUTN vs. OUTN VOLTAGE



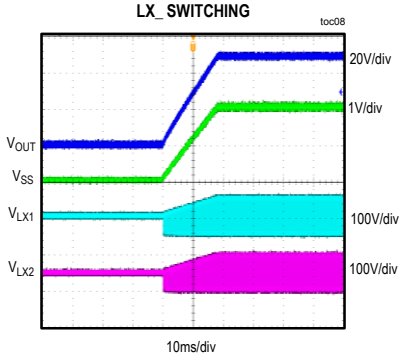
LOAD REPORTING vs. LOAD



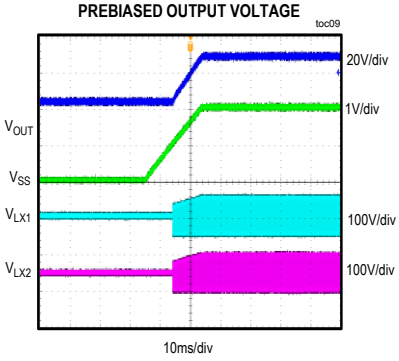
STARTUP WAVEFORM EN/UVLO RISING



STARTUP WAVEFORM LX_ SWITCHING

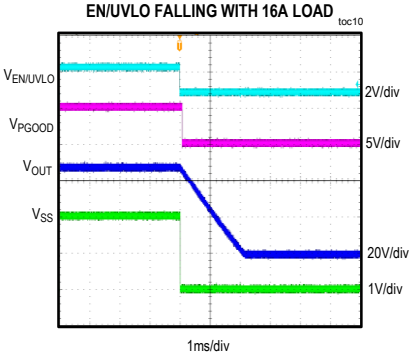


STARTUP WAVEFORM WITH PREBIASED OUTPUT VOLTAGE

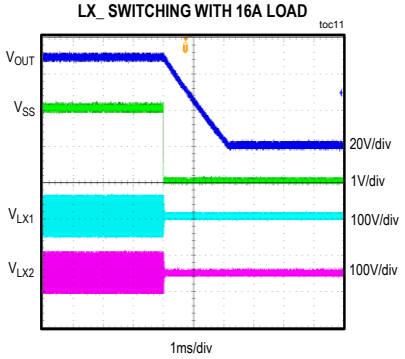


(T_A = +25°C, V_{IN-} = -48V, V_{OUT} = 48V, unless otherwise noted. See the *Typical Application Circuits*.)

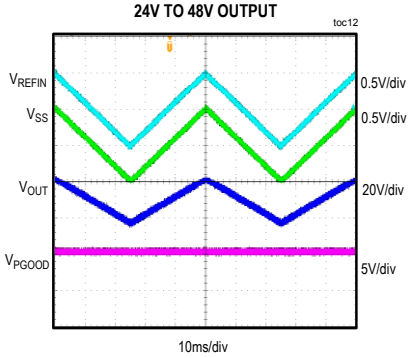
SHUTDOWN WAVEFORM EN/UVLO FALLING WITH 16A LOAD



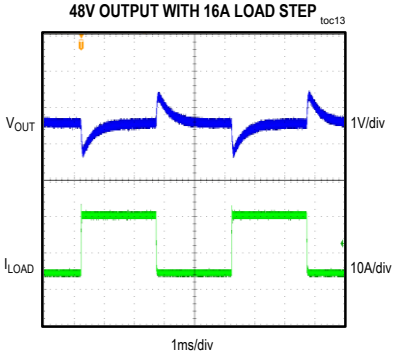
SHUTDOWN WAVEFORM LX_ SWITCHING WITH 16A LOAD



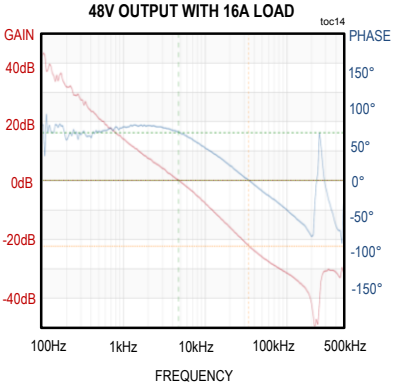
DYNAMIC REFIN RAMP RESPONSE 24V TO 48V OUTPUT



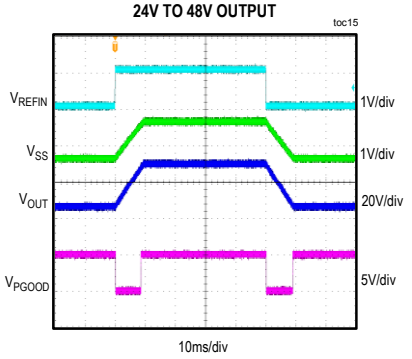
LOAD-TRANSIENT WAVEFORM 48V OUTPUT WITH 16A LOAD STEP



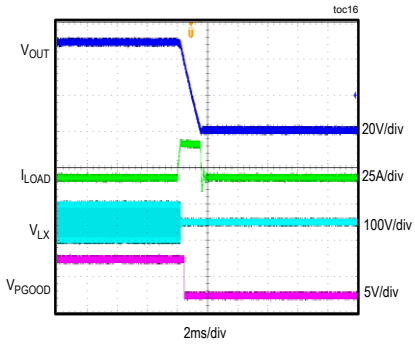
BODE PLOT 48V OUTPUT WITH 16A LOAD



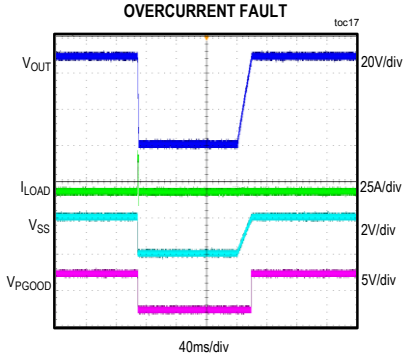
DYNAMIC REFIN STEP RESPONSE 24V TO 48V OUTPUT



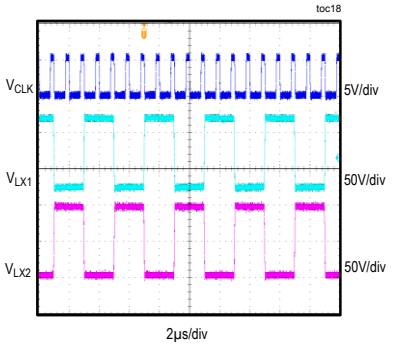
OUTPUT OVERCURRENT WAVEFORM



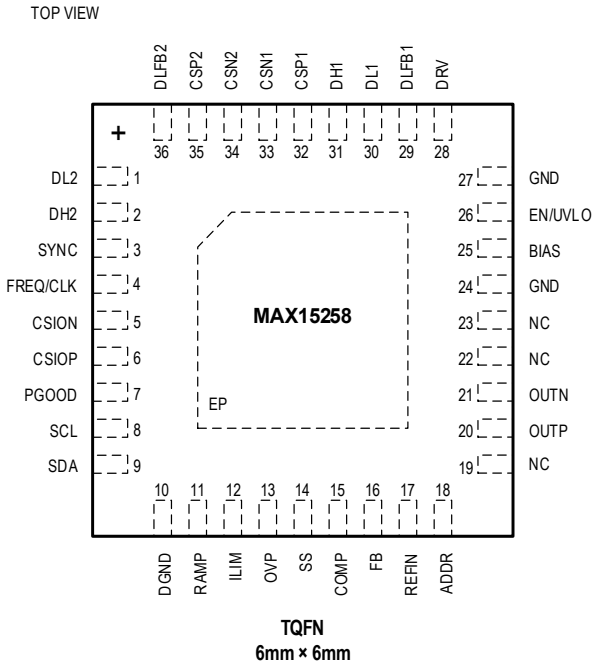
AUTO-RETRY AFTER OVERCURRENT FAULT



CLOCK SYNCHRONIZATION



Pin Configurations

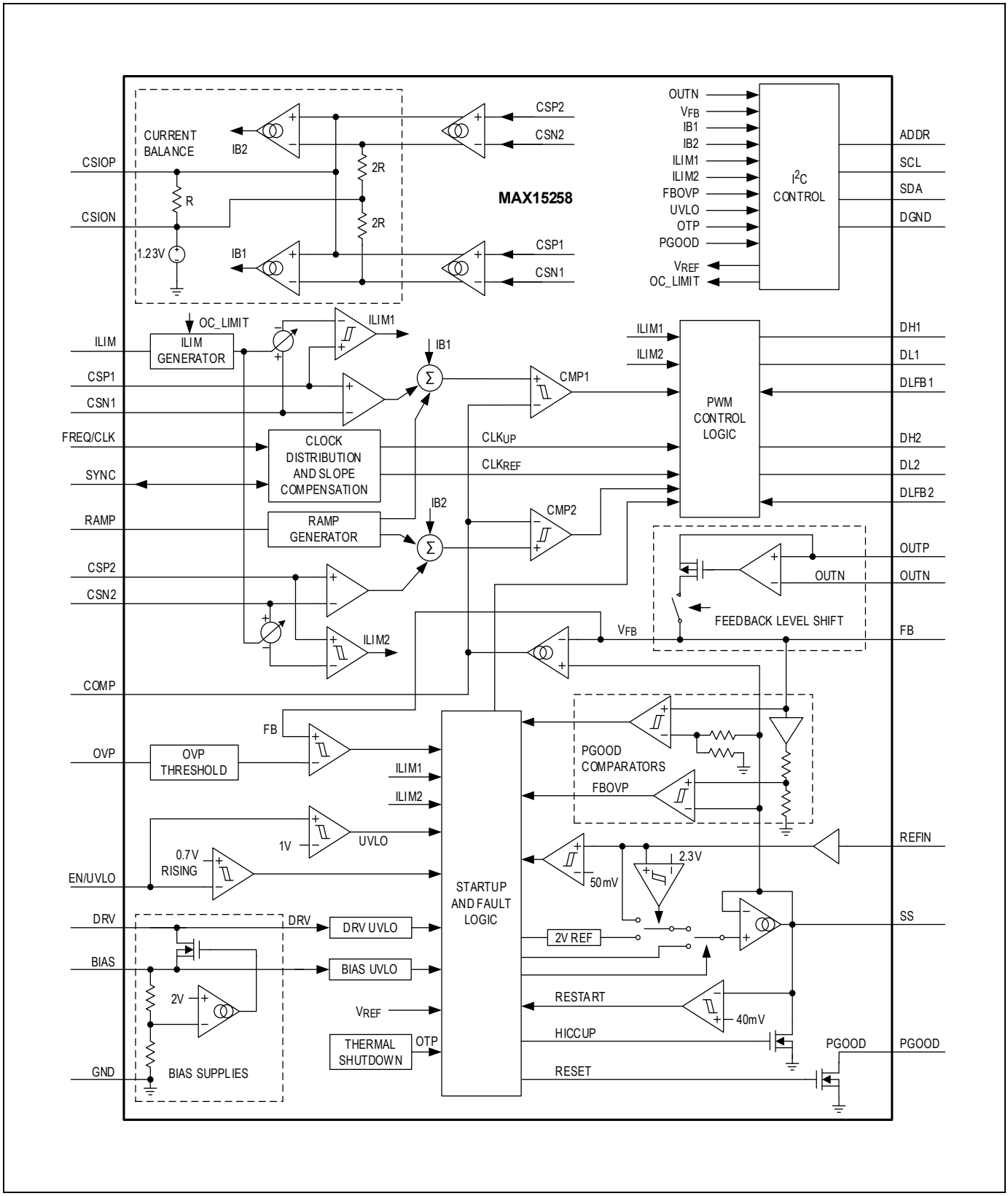


Pin Descriptions

PIN	NAME	FUNCTION
1	DL2	Logic Output for Low-Side MOSFET Gate Driver for the Second Phase. Connect DL2 to the low-side input pin of the second-phase external MOSFET driver.
2	DH2	Logic Output for High-Side MOSFET Gate Driver for the Second Phase. Connect DH2 to the high-side input pin of the second-phase external MOSFET driver.
3	SYNC	Multiphase Synchronization Pin. For single-IC operation, leave this pin unconnected. Tie this pin together when two ICs are stacked-up in controller/target operation mode.
4	FREQ/CLK	Frequency Selection/Clock Synchronization Input. The MAX15258 supports switching frequencies from 120kHz to 1MHz. Set the switching frequency by either selecting the appropriate external resistor to use the internal oscillator frequency, or by synchronizing the regulator to an external system clock (see *Table 2*). Leave the FREQ/CLK pin unconnected to select the preset 300kHz switching frequency, or place a resistor between FREQ/CLK and GND to set the following: $f_{SW} = (R_{FREQ}/100k\Omega) \times 600kHz$.
5	CSION	Negative Input of Controller/Target Current-Sense Signal. The MAX15258 uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15258 ICs are stacked up in controller/target operation mode.
6	CSIOP	Positive Input of Controller/Target Current-Sense Signal. The MAX15258 uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15258 ICs are stacked up in controller/target operation mode.
7	PGOOD	Open-Drain Power-Good Output. The MAX15258 pulls PGOOD low when the output voltage exceeds the OVP threshold during soft-start and shutdown (EN/UVLO pulled low). The PGOOD output goes high-impedance when the controller completes soft-start and remains in regulation.
8	SCL	I^2C Clock
9	SDA	I^2C Data
10	DGND	Ground for Digital Circuit. Connect this pin directly to the GND pin.
11	RAMP	Slope Compensation Input. A resistor connected from RAMP to GND programs the amount of slope compensation. See the *Adjustable Slope Compensation (RAMP)* section.
12	ILIM	CSP_ - CSN_ Cycle-by-Cycle/Hiccup Current-Limit Threshold Selector. Connect a resistor from ILIM to GND to select the protection value. The ILIM configuration is overridden by writing a nonzero value to OC_FAULT_LIMIT.

13	OVP	Program Pin. Connect a resistor from OVP to GND to configure FB overvoltage protection, FB level shifter selection, and multiphase selection (see *Table 1*).
14	SS	Soft-Start Control. The capacitance (C_{SS}) between SS and GND sets the startup period. An internal pull-down MOSFET holds SS low until the controller begins the startup sequence.
15	COMP	Compensation Amplifier Output. COMP is the output of the internal transconductance error amplifier. Connect a Type II compensation network, as shown in the *Typical Application Circuits*. (Also see the *Compensation Design Guidelines* section).
16	FB	Feedback Input. When the FB level shifter is enabled, connect a resistor from FB to GND. When the FB level shifter is disabled, connect FB to the center of a resistor-divider between the output and GND. When two MAX15258 ICs are stacked-up in controller/target operation mode, connect FB of the target to BIAS.
17	REFIN	External Reference Input. REFIN sets the FB regulation voltage when supplied with a voltage between 1V and 2.2V. Connect the REFIN pin to BIAS to select the internal 2.0V reference voltage. The REFIN configuration is overridden by writing a nonzero value to VREF_COMMAND.
18	ADDR	I^2C Address Program Pin. Connect a resistor from ADDR to GND to select the I^2C address (see *Table 3*).
19, 22, 23	NC	Not Connected
20	OUTP	Positive Differential Output Voltage Sense Input. The MAX15258 can operate in inverting buck-boost mode and sense output voltage differentially using its internal FB level shifter. Connect a sense resistor between OUTP and the positive node of the output, as shown in the *Typical Application Circuits*. In applications with the FB level shifter disabled, tie OUTP and OUTN together, then connect to V_{IN+} for input voltage reporting.
21	OUTN	Negative Differential Output Voltage Sense Input. The MAX15258 can operate in inverting buck-boost mode and sense output voltage differentially using its internal FB level shifter. Connect OUTN to the negative node of output, as shown in the *Typical Application Circuits*. The OUTN voltage is monitored by READ_OUTN for voltage reporting. In applications with the FB level shifter disabled, tie OUTN and OUTP together, then connect to V_{IN+} for input voltage reporting.
24, 27	GND	Analog Ground
25	BIAS	5V Linear Regulator Output and Controller Bias Supply. Bypass to GND with a 2.2µF or greater ceramic capacitor.
26	EN/UVLO	Enable Control/Adjustable Undervoltage Lockout Input for Startup/Shutdown Power Sequencing. Connect EN/UVLO to the center of a resistor-divider between the input and GND to adjust the undervoltage lockout voltage level, as shown in the *Typical Application Circuits*.
28	DRV	Supply Voltage Input. Provide a 8.5V to 14V supply for internal bias generation.
29	DLFB1	External MOSFET Status Feedback Pin for the First Phase. Connect DLFB1 to the center of a resistor-divider between the gate of the first-phase, low-side MOSFET and GND. See the *MOSFET Gate Control* section.
30	DL1	Logic Output for Low-Side MOSFET Gate Driver for the First Phase. Connect DL1 to the low-side input pin of the first-phase external MOSFET driver.
31	DH1	Logic Output for High-Side MOSFET Gate Driver for the First Phase. Connect DH1 to the high-side input pin of the first-phase external MOSFET driver.
32	CSP1	Positive Low-Side Differential Current-Sense Input for the First Phase. The MAX15258 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSP1 to the MOSFET side of the current-sense resistor.
33	CSN1	Negative Low-Side Differential Current-Sense Input for the First Phase. The MAX15258 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSN1 to the ground side of the current-sense resistor.
34	CSN2	Negative Low-Side Differential Current-Sense Input for the Second Phase. The MAX15258 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSN2 to the ground side of the current-sense resistor.
35	CSP2	Positive Low-Side Differential Current-Sense Input for the Second Phase. The MAX15258 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSP2 to the MOSFET side of the current-sense resistor.
36	DLFB2	External MOSFET Status Feedback Pin for the Second Phase. Connect DLFB2 to the center of a resistor-divider between the gate of the second-phase low-side MOSFET and GND. See the *MOSFET Gate Control* section.
—	EP	Exposed Pad. Connect to GND.

Functional Diagrams



Detailed Description

The MAX15258, a high-voltage, multiphase boost controller with a I2C digital interface, is designed to support up to two MOSFET drivers and four external MOSFETs in single-phase or dual-phase boost/inverting-buck-boost configurations. Two devices can be stacked up for triple-phase or quad-phase operation. When configured as inverting-buck-boost converter, the MAX15258 has an internal high-voltage FB level shifter to differentially sense the output voltage. The output voltage can be dynamically set through the 1V to 2.2V REFIN or I2C digital interface.

The switching frequency is controlled either through an external resistor setting the internal oscillator or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1MHz switching frequencies. When two devices are stacked up as controller-target for triple-phase or quad-phase operation, the SYNC pins of two devices are connected to ensure clock synchronization and phase interleaving. The controller has a dedicated enable/input undervoltage-lockout (EN/UVLO) pin to configure for flexible power sequencing.

The MAX15258 has a dedicated RAMP pin to adjust internal slope compensation. The device features adjustable overcurrent protection. The device incorporates current-sense amplifiers to accurately measure the current of each phase across external sense resistors to implement accurate phase current sharing. The controller is also protected against output overvoltage, input undervoltage, and thermal shutdown.

High-Voltage Internal FB Level Shifter

The MAX15258 can support both boost and inverting-buck-boost applications. When configured in inverting-buck-boost operation, the GND pin of the device must be connected to the negative input voltage terminal (V_{IN-}), so that the ground of the IC is different than the ground of output capacitor and load. Output voltage cannot be controlled using a simple resistor-divider. The MAX15258 has a dedicated internal FB level shifter to differentially sense the output voltage. The internal FB level shifter can be enabled or disabled by connecting a resistor from the OVP pin to GND (see the *Overvoltage Protection (OVP)* section). When the internal FB level shifter is enabled, connect OUTN to the ground node of the output capacitor and OUTP to the output terminal using a resistor R_{FB1}. FB is connected to GND (V_{IN-}) using a resistor R_{FB2}. The output voltage is set by these two resistors:

$$V_{OUT} = \frac{R_{FB1}}{R_{FB2}} \times V_{REF}$$

V_{REF} is the reference voltage for FB regulation, which can be set by either applying a voltage between 1V and 2.2V on the REFIN pin or VREF_COMMAND through the I2C digital interface. When VREF_COMMAND = 0, REFIN input takes the control of V_{REF}, and connecting REFIN pin to BIAS could select the internal preset 2.0V reference voltage. Writing a nonzero value to VREF_COMMAND passes the V_{REF} control to VREF_COMMAND. By default, the value of VREF_COMMAND is 0.

When the FB level shifter is enabled, the OUTN pin has a UVLO threshold that controls the power sequencing. If the voltage on OUTN falls below 7.0V (typ), the controller disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor through a 4.3Ω pull-down MOSFET.

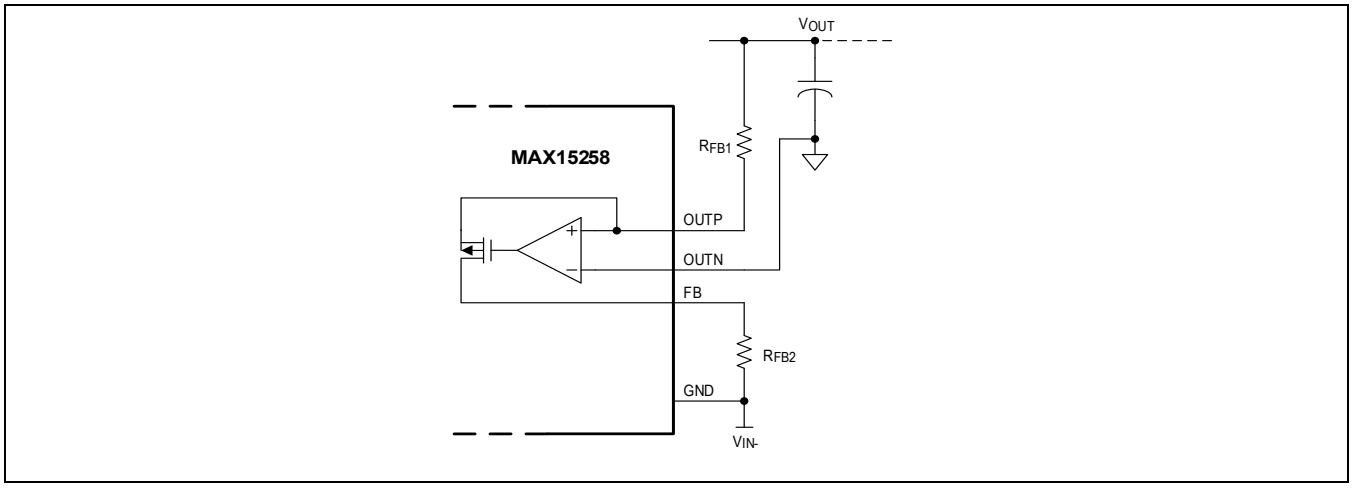


Figure 1. Using Internal FB Level Shifter

For inverting-buck-boost applications where V_{IN} is higher than 76V, the MAX15258 can still be used, but an external level shifter is required. The internal FB level shifter must be disabled. An example of using external FB level shifter is shown in *Figure 2*. Two matched PNP transistors are used. The output voltage is given by:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times V_{REF}$$

When operating in boost mode, the internal FB level shifter is disabled. Then the FB pin must be connected to the center of a resistor-divider from the output to GND, as shown in *Figure 3*. When the resistor-divider is used, the output voltage is given by:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times V_{REF}$$

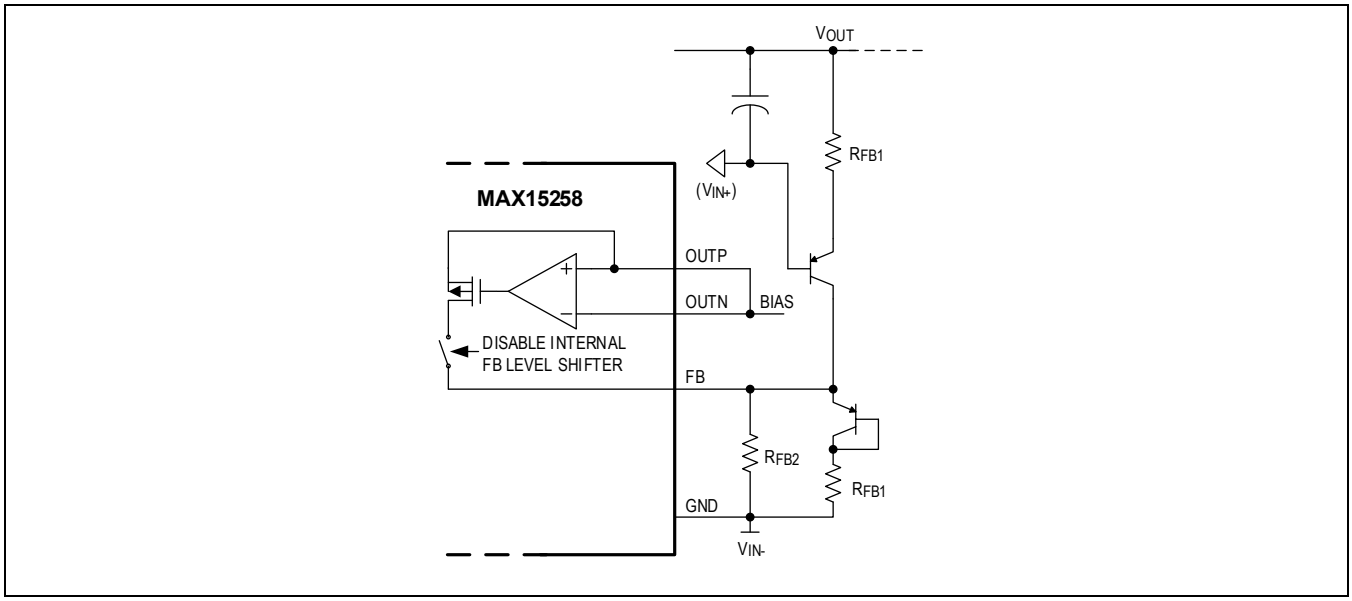


Figure 2. Using External FB Level Shifter

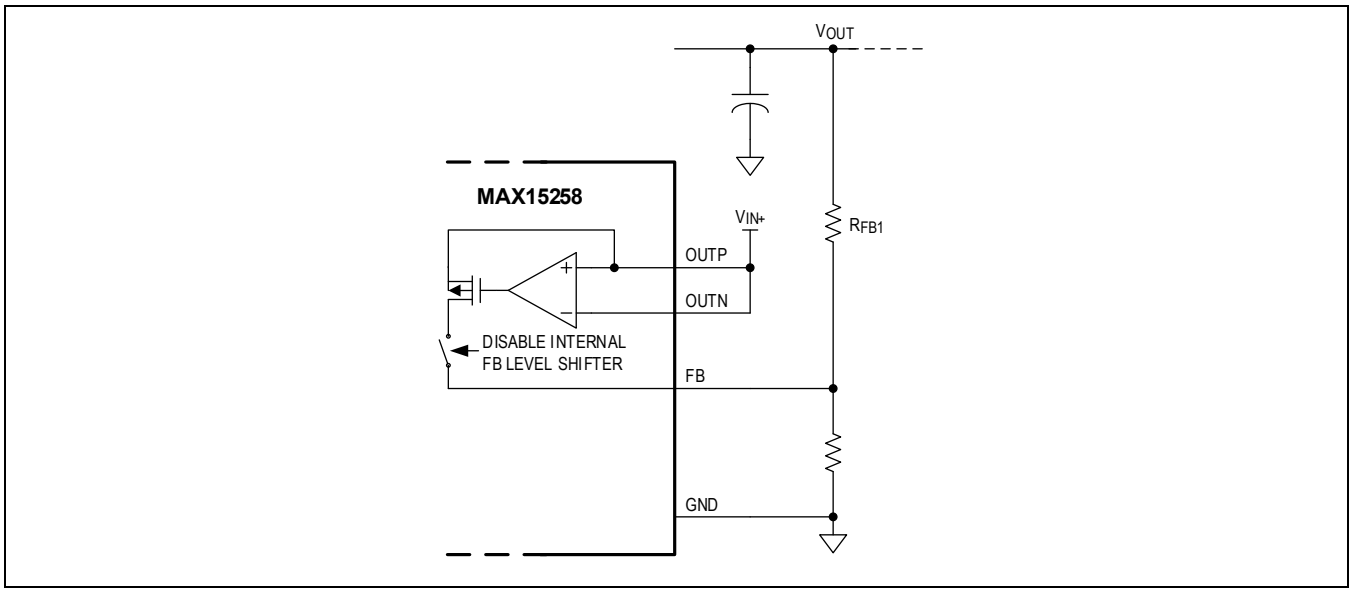


Figure 3. Using External FB Resistor-Divider

OUTN voltage is monitored by READ_OUTN for voltage reporting. In applications with the FB level shifter disabled, tie OUTN and OUTP together, then connect to V_{IN+} for input voltage reporting.

Peak-Current-Mode Control Loop

The controller relies on a fixed-frequency, peak-current-mode architecture to regulate the output. A detailed block diagram of the control loop is shown in *Figure 4*. A sense resistor is required between the source of the low-side MOSFET and GND for current sensing. The sense resistor should be selected so that the maximum differential voltage across CSP_ and CSN_ does not exceed the cycle-by-cycle peak current-limit threshold (see the *Overcurrent Protection (OCP)* section). The differential voltage across CSP_ and CSN_ is amplified 4.4 times by a current-sense amplifier. A high-frequency RC noise filter is suggested across the sense resistor. The RC time constant should not exceed 30ns.

The error between the output voltage feedback (V_{FB}) and reference voltage (V_{SS}) is fed to the input of an error amplifier. The output of the error amplifier (COMP) is required to connect to a Type II compensation network for control loop stability (see the *Compensation Design Guidelines* section). A slope compensation ramp generator is also used. The slope of the compensation ramp can be adjusted by connecting a resistor between RAMP and GND (see the *Adjustable Slope Compensation (RAMP)* section).

The controller drives on the low-side MOSFET (DL_ driven high) on each rising clock edge. The controller pulls DL_ low and drives DH_ high when the PWM comparator detects that the sum of the current-sense amplifier output ($V_{CS\_}$), the slope compensation ramp, and the phase current imbalance signal exceeds the COMP voltage.

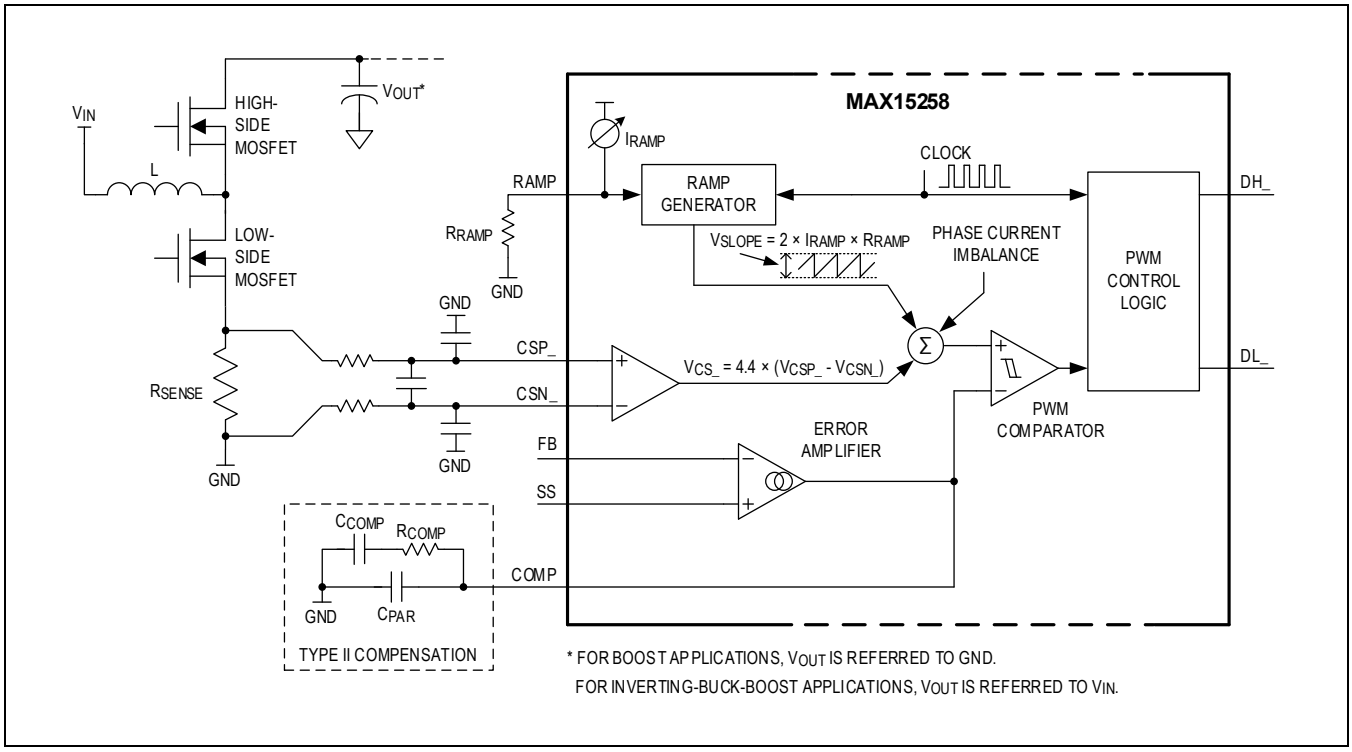


Figure 4. Peak-Current-Mode Control Loop

Compensation Design Guidelines

The MAX15258 utilizes a fixed-frequency, peak current-mode control scheme to provide easy compensation and fast-transient response. It is by design for boost or inverting buck-boost converters to have a right half plane (RHP) zero in their small signal control-to-output transfer function. For boost converters, the location of RHP zero is calculated by:

$$f_{RHP} = \frac{V_{OUT} \times (1 - D)^2}{2 \times \pi \times I_{OUT(MAX)} \times L}$$

where:

$I_{OUT(MAX)}$ = Maximum load current per phase

D = duty cycle = $1 - V_{IN}/V_{OUT}$

L = value of the inductor

For inverting-buck-boost converters, the location of RHP zero is calculated by:

$$f_{RHP} = \frac{V_{OUT} \times (1 - D)^2}{2 \times \pi \times I_{OUT(MAX)} \times L \times D}$$

where:

D = duty cycle = $V_{OUT}/(|V_{IN}| + V_{OUT})$

For stable operation, it is required that the bandwidth of control loop (BW) be sufficiently lower than f_{RHP} and the switching frequency (f_{SW}):

BW ≤ minimum($f_{RHP}/7$, $f_{SW}/10$)

A Type II compensation network is required to be connected between COMP and GND (R_{COMP}, C_{COMP}, and C_{PAR} in *Figure 4*) to provide sufficient phase margin and gain margin to the control loop. The value of the compensation network can be selected by:

$$R_{COMP} = \frac{16 \times \pi \times BW \times R_{SENSE} \times C_{OUT} \times V_{OUT}}{N \times (1 - D) \times G_{MEA} \times V_{REF}}$$

$$C_{COMP} = \frac{5}{\pi \times R_{COMP} \times BW}$$

$$C_{PAR} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{SW}}$$

where:

R_{SENSE} = value of the sense resistor

C_{OUT} = value of the output capacitor

N = number of phases

G_{MEA} = error amplifier transconductance (1.15mS, typ)

Adjustable Slope Compensation (RAMP)

When the MAX15258 operates at a duty cycle greater than 50%, additional slope compensation is required to ensure stability and prevent subharmonic oscillations that occur naturally in peak-current-mode controlled converters operating in continuous-conduction mode (CCM). The MAX15258 provides RAMP input to select the internal slope compensation ramp within a range of 240mV to 1500mV. It is recommended that discontinuous-conduction mode (DCM) designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

As shown in *Figure 4*, by connecting a resistor (R_{RAMP}) between RAMP and GND, the amplitude of the slope compensation ramp is calculated as:

$$V_{SLOPE} = 2 \times V_{RAMP} = 2 \times I_{RAMP} \times R_{RAMP}$$

where:

I_{RAMP} = current sourced from RAMP to GND (10µA, typ)

To guarantee stable and jitter-free operation, it is suggested to select the RAMP resistor such that:

$$R_{RAMP} \geq \frac{5 \times (V_{OUT(MAX)} - V_{IN(MIN)}) \times R_{SENSE}}{I_{RAMP} \times f_{SW} \times L}$$

where:

$V_{OUT(MAX)}$ = maximum output voltage referred to GND

$V_{IN(MIN)}$ = minimum input voltage referred to GND

R_{SENSE} = value of the sense resistor

f_{SW} = switching frequency

L = value of the inductor

DRV Supply and Bias Regulator (BIAS)

The controller requires an external 8.5V to 14V DRV supply. The DRV supply powers the internal linear regulator that generates a regulated 5V bias supply to power the internal analog and digital control circuitry as shown in the *Functional Diagrams*. Bypass the BIAS pin with a 2.2µF or greater ceramic capacitor to maintain noise immunity and stability. The

BIAS regulator provides up to 35mA of load current and the controller requires up to 5mA, so the remaining load capability can be used to support pull-up resistors.

The controller has an undervoltage-lockout threshold on DRV. The undervoltage-protection circuits inhibit switching until DRV rises above 8.25V (typ).

If DRV drops below its undervoltage threshold, the controller determines that there is insufficient supply voltage to make valid control decisions. To protect the regulator and the output, the controller immediately pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 4.3Ω discharge MOSFET, placing the regulator into a high-impedance output state so the output capacitance passively discharges through the load current.

The BIAS linear regulator powers up as long as DRV exceeds its undervoltage-lockout threshold.

EN/UVLO and Soft-Start/Shutdown

The EN/UVLO pin allows the input voltage operating range to be externally adjusted for power-sequence control. Connect EN/UVLO to the center of a resistor-divider between the input and GND to adjust the undervoltage lockout voltage level, as shown in the *Typical Application Circuits*. In the case where the DRV voltage threshold of the external MOSFET driver is higher than the undervoltage lockout threshold of the DRV pin, the EN/UVLO pin should also be pulled to GND before the external MOSFET driver is enabled. At power-up, once the voltage of EN/UVLO is higher than 1V (typ) and the internal reference stabilizes, the controller starts the initialization period where the OVP pin configuration is checked. During this initialization period, the controller pulls SS low through a 4.3Ω discharge MOSFET. As long as initialization is complete, the controller starts the soft-start sequence by charging the SS capacitor with a constant 5µA current source until the SS voltage reaches the target reference voltage. The drivers start switching once SS exceeds 53mV and the controller detects that the FB voltage is below the SS voltage. The controller enables the overvoltage fault-protection circuitry when SS exceeds 1V. For proper startup, especially in applications with the external REFIN voltage applied, make sure that the external REFIN voltage exceeds 100mV before the controller is enabled.

At power-down, once the voltage of EN/UVLO is below 0.9V (typ), the controller pulls SS low, stops switching, and enters a low-power shutdown state (see *Figure 5*).

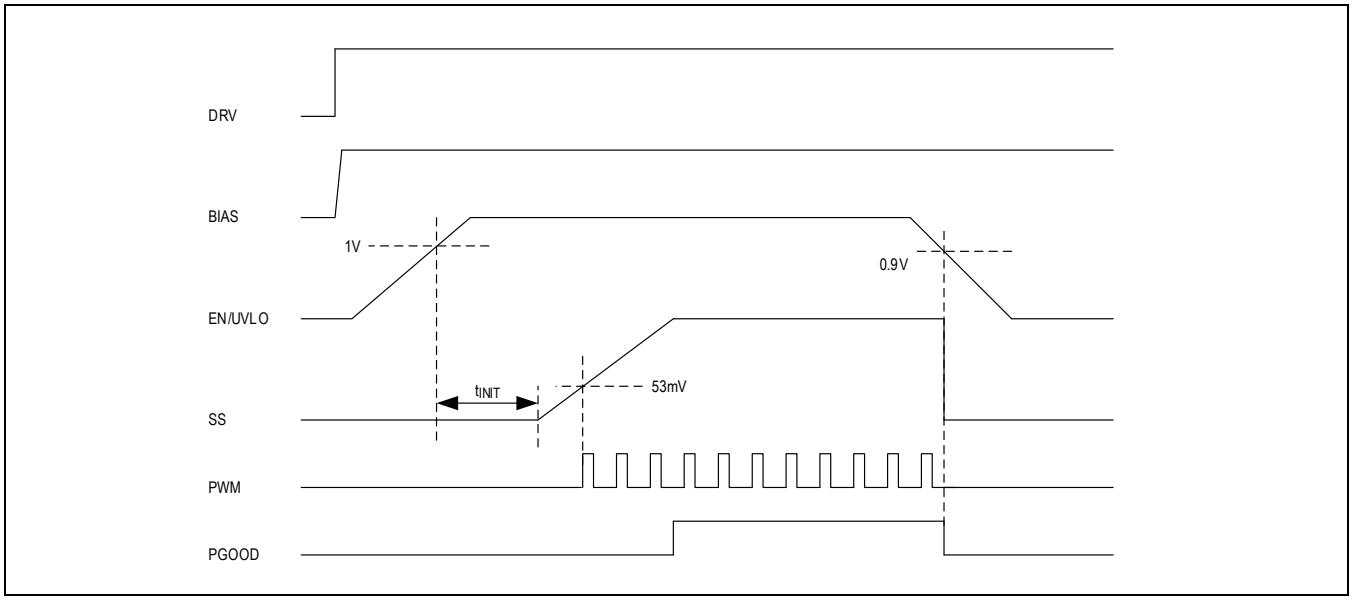


Figure 5. Soft-Start and Shutdown Sequence with EN/UVLO

Overcurrent Protection (OCP)

A current-sense resistor is connected between the source of the low-side MOSFET and GND. The MAX15258 detects the current-sense signal (CSP_ to CSN_) and compares it with the cycle-by-cycle peak current-limit threshold during low-side on-time. When the current exceeds the cycle-by-cycle peak current-limit threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET to allow the inductor current to be discharged until the end of that switching cycle. Each phase has an independent up-down counter to accumulate the number of consecutive peak current-limit events. If the counter exceeds 31, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

There is a secondary fast positive overcurrent protection (FPOCP) threshold, which is 33% higher than the cycle-by-cycle peak current-limit threshold. If the inductor peak current exceeds the FPOCP threshold, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

The device also has a negative overcurrent protection (NOCP) threshold, which is -80% of the cycle-by-cycle peak current-limit threshold. When the low-side MOSFET is turned on and the inductor current is below the NOCP threshold, the device will command to keep the low-side MOSFET on to allow the inductor current to be charged by the input voltage until the end of that switching cycle. Each phase has an independent up-down counter to accumulate the number of consecutive NOCP events. If the counter exceeds 31, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

The cycle-by-cycle peak current-limit threshold is set by either a resistor at ILIM pin or OC_FAULT_LIMIT through the I^2C digital interface.

With OC_FAULT_LIMIT = 0, the current-limit threshold is set by the resistor at the ILIM pin. A 10µA source current flows into this resistor and generates a voltage level. This voltage level is internally scaled by a factor of 0.10 to set the cycle-by-cycle peak current-limit threshold. The minimum and maximum settable current-limit levels (V_{OCP}) are 20mV and 100mV. The cycle-by-cycle peak current-limit level is given by:

$V_{OCP} = 0.10 \times 10\mu A \times R_{ILIM}$

Writing a nonzero value to OC_FAULT_LIMIT passes the V_{OCP} control to OC_FAULT_LIMIT. By default, the value of OC_FAULT_LIMIT is 0.

The maximum peak inductor current is set by both V_{OCP} and the current-sense resistor (R_{SENSE}):

$$I_{PEAK(MAX)} = \frac{V_{OCP}}{R_{SENSE}}$$

Overvoltage Protection (OVP)

The MAX15258 has an OVP comparator to monitor the FB voltage. The device can be configured to disable OVP or select OVP threshold of 110% by connecting a resistor from the OVP pin to GND. FB OVP is also disabled when the voltage on the SS pin is below 1V. Once OVP is enabled, the drivers start switching, and the voltage on the SS pin is higher than 1V, the FB overvoltage comparator trips if the feedback voltage exceeds the SS voltage by 110% for more than 128 PWM clock cycles. If the overvoltage comparator is triggered, the controller pulls PGOOD low, discharges the SS capacitor, and disables the drivers. The controller immediately restarts once the fault condition has been removed. When OVP is disabled, the PGOOD will remain high when the FB voltage is higher than the reference voltage.

The resistor from the OVP pin to GND is also used to enable or disable the FB level shifter and select single- or dual-phase operation. See *Table 1* for details.

Table 1. FB OVP Settings, Phase and FB Level Shifter Configuration

R_{OVP} (1% RESISTOR)	FB OVP THRESHOLD	FB LEVEL SHIFTER	PHASE CONFIGURATION
GND	110%	Disabled	Dual-phase or quad-phase operation
33.2kΩ	110%	Enabled	
51.1kΩ	Disabled	Disabled	
69.8kΩ	Disabled	Enabled	
95.3kΩ	110%	Disabled	Single-phase operation
118kΩ	110%	Enabled	
140kΩ	Disabled	Disabled	
162kΩ	Disabled	Enabled	
182kΩ	110%	Disabled	Triple-phase operation
205kΩ	110%	Enabled	
226kΩ	Disabled	Disabled	
OPEN	Disabled	Enabled	

Thermal Shutdown (T_{SHDN})

The controller features a thermal fault-protection circuit. When the junction temperature rises above +165°C, the internal thermal sensor triggers the fault protection, disables the drivers, and discharges the SS capacitor. The controller remains disabled until the junction temperature cools by 15°C. Once the device has cooled down, the controller automatically restarts using the soft-start sequence.

Switching Frequency (FREQ/CLK)

The controller supports 120kHz to 1MHz switching frequencies. Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. To adjust the switching frequency, either place an external resistor from FREQ/CLK to GND or drive FREQ/CLK with an external system clock (see *Table 2*). The resistively programmable switching frequency is determined by:

$$f_{SW} = \frac{R_{FREQ}}{100k\Omega} \times 600kHz$$

Table 2. Phase and Controller/Target Configuration

NUMBER OF PHASES	NUMBER OF MAX15258 DEVICES	FB OF TARGET CONNECTED TO BIAS	CLK FREQUENCY
1	1	N/A	$4 \times f_{SW}$
2	1	N/A	$4 \times f_{SW}$
3	2	Yes	$3 \times f_{SW}$
4	2	Yes	$4 \times f_{SW}$

Phase and Controller/Target Configurations

The MAX15258 can be configured in single-phase, dual-phase, triple-phase or quad-phase operation modes. When supporting triple-phase or quad-phase operation, two MAX15258 ICs are used as controller and target. The controller identifies the number of phases by the resistor at the OVP pin (selecting the same R_{OVP} is required for controller IC and target IC). This identification is used to determine how the controller responds to the multiphase clock signal generated by the primary phase.

For proper synchronization between two devices, connect the SYNC, COMP, CSIOP, and CSION of the controller and target devices together. See the *Typical Application Circuits* for the connections of FB, REFIN, SS, OUTP, and OUTN of the target device.

In a triple-phase converter, the two phases of the MAX15258 controller interleave by 240°, while the MAX15258 target phase 1 operates with a 120° phase shift compared to the controller. The second phase of the target remains unused (*Figure 6*).

In a quad-phase converter, the two phases of the MAX15258 controller or target interleave by 180°, while controller and target operate with 90° phase shift (*Figure 7*).

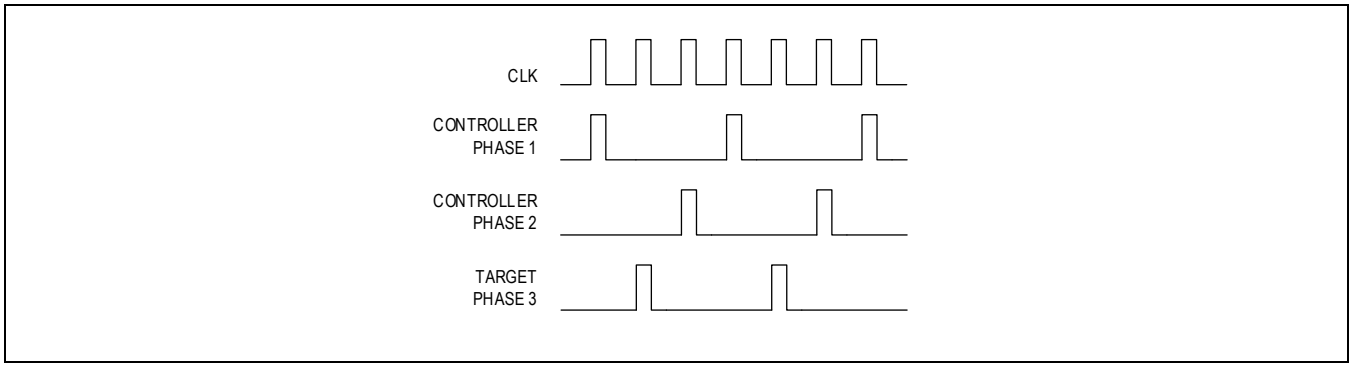


Figure 6. Triple-Phase Synchronization (Controller/Target)

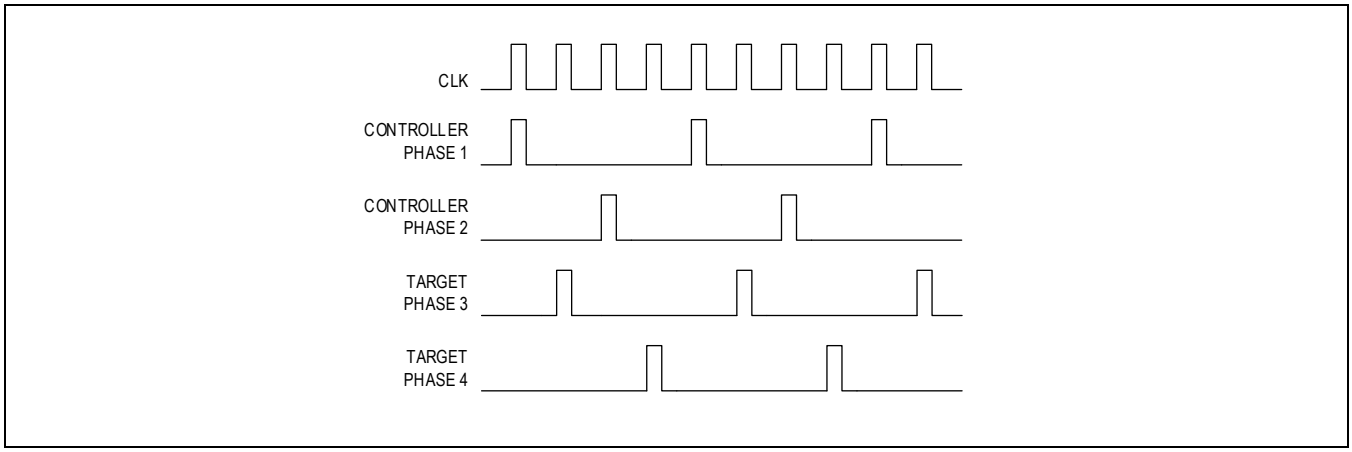


Figure 7. Quad-Phase Synchronization (Controller/Target)

Multiphase Current Balance

The MAX15258 monitors the low-side MOSFET current of each phase for active phase current balancing in multiphase operations. The current imbalance is applied to the cycle-by-cycle current sensing circuitry as feedback, helping regulate so that the load current is evenly shared between the two phases (see the *Functional Diagrams*).

In triple-phase or quad-phase operation, the device uses the differential CSIO_ connections to communicate the average per-chip current between the controller and target. The current-mode controller and target devices regulate their current so that all phases share the load current equally.

MOSFET Gate Control

The MAX15258 must be used with external MOSFET drivers to drive power MOSFETs for typical high-voltage applications. The device has dedicated DLFB_ pins to detect the gate voltage of the low-side MOSFETs to ensure no-shoot-through between the high- and low-side MOSFETs due to the mismatch delays caused by the external MOSFET driver. The DLFB_ pins have a rising threshold of 0.8V (typ) and falling threshold of 0.5V (typ). A resistor-divider can be used from the gate of the low-side MOSFET to the DLFB_ pins to match the MOSFET gate threshold voltage and the DLFB_ threshold (see the *Typical Application Circuits*) to allow robust operation with a wide range of MOSFETs while minimizing dead-time power losses.

I²C Digital Interface

The MAX15258 operates as a target device that sends and receives data through I²C digital interface. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors, typically 4.7kΩ, are required on these lines.

I²C Address Selection

The MAX15258 has a 7-bit long target address. The bit following the 7-bit target address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The upper four bits of the target address cannot be changed and are always [1010]. The lower three bits can be programmed by connecting a 1% resistor between the ADDR pin and GND to assign the device one of seven unique target addresses (see *Table 3*).

Table 3. Address Configuration

R_{ADDR} (1% RESISTOR)	TARGET ADDRESS (BIN)
GND	1010000
47kΩ	1010001
78.7kΩ	1010010
110kΩ	1010011
143kΩ	1010100
174kΩ	1010101
205kΩ	1010110
OPEN	1010111

Register Map and Description

The MAX15258 contains a bank of volatile registers that stores its configurations and status (see *Table 4*). These registers are supplied by BIAS; when the BIAS voltage drops below 3.6V, all registers will be reset.

Table 4. Register Map Summary

ADDR	REGISTER NAME	TYPE	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	STATUS_BYTE	RO	N/A	CSION	M/S	FB_OV	PH2_OC	PH1_OC	EN/UVLO	OT	PGOOD
01h	CLEAR_FAULTS	WO									
02h	READ_OUTN	RO	N/A	0	0	0	0	0	0	OUTN[9]	OUTN[8]
03h			N/A	OUTN[7]	OUTN[6]	OUTN[5]	OUTN[4]	OUTN[3]	OUTN[2]	OUTN[1]	OUTN[0]
04h	READ_FB	RO	N/A	0	0	0	0	0	0	VFB[9]	VFB[8]
05h			N/A	VFB[7]	VFB[6]	VFB[5]	VFB[4]	VFB[3]	VFB[2]	VFB[1]	VFB[0]
06h	READ_IPH1	RO	N/A	0	0	0	0	0	0	IPH1[9]	IPH1[8]
07h			N/A	IPH1[7]	IPH1[6]	IPH1[5]	IPH1[4]	IPH1[3]	IPH1[2]	IPH1[1]	IPH1[0]
08h	READ_IPH2	RO	N/A	0	0	0	0	0	0	IPH2[9]	IPH2[8]
09h			N/A	IPH2[7]	IPH2[6]	IPH2[5]	IPH2[4]	IPH2[3]	IPH2[2]	IPH2[1]	IPH2[0]
0Ah	OC_FAULT_LIMIT	R/W	00h	OCP[7]	OCP[6]	OCP[5]	OCP[4]	OCP[3]	OCP[2]	OCP[1]	OCP[0]
0Bh	VREF_COMMAND	R/W	00h	0	0	0	0	0	0	VREF[9]	VREF[8]
0Ch			00h	VREF[7]	VREF[6]	VREF[5]	VREF[4]	VREF[3]	VREF[2]	VREF[1]	VREF[0]

VREF_COMMAND

The MAX15258 has an internal 10-bit DAC that allows the internal reference voltage to be set through the VREF_COMMAND register to any value in the range of 0 to 2.238V with 2.18mV/bit resolution.

V_{REF} = VREF_COMMAND<bit15-0> × 2.18mV/bit

By default, the value of VREF_COMMAND is 0, and V_{REF} is determined by the voltage at REFIN pin. Writing a nonzero value to VREF_COMMAND passes the V_{REF} control to VREF_COMMAND. The value of VREF_COMMAND down to 0 is available, but operating VREF_COMMAND below 1V is not recommended due to the disabled FB overvoltage-fault protection and always pulled low PGOOD.

In multiphase operation, VREF_COMMAND is active for the controller IC only, and inactive for the target IC.

OC_FAULT_LIMIT

The OC_FAULT_LIMIT sets a voltage level in the range of 200mV to 997mV with 3.1mV/bit resolution. This voltage level is internally scaled by a factor of 0.10 to set cycle-by-cycle peak current limit in the range of 20mV to 100mV.

V_{OCP} = 0.1 × (OC_FAULT_LIMIT<bit7-0> × 3.1mV/bit + 200mV)

By default, the value of OC_FAULT_LIMIT is 0, and V_{OCP} is determined by the resistor at the ILIM pin. Writing a nonzero value to OC_FAULT_LIMIT passes the V_{OCP} control to OC_FAULT_LIMIT.

In multiphase operation, OC_FAULT_LIMIT of each IC is programmed separately.

Same as the pin-strap configuration at the ILIM pin, the negative overcurrent protection (NOCP) threshold is -80% of the value of OC_FAULT_LIMIT, and the fast positive overcurrent protection (FPOCP) threshold is 33% higher than the value of OC_FAULT_LIMIT.

READ_FB

The READ_FB register returns the voltage at the FB pin, in the range of 0 to 2.56V with 2.5mV/bit resolution. This register refreshes at a 3.2ms rate.

In multiphase operation, the READ_FB register of the target IC returns its maximum voltage, 2.56V, because the FB pin of target IC is shorted to the BIAS pin.

V_{FB} = READ_FB<bit15-0> × 2.5mV/bit

READ_OUTN

The READ_OUTN register returns the voltage at the OUTN pin divided by 30 by an internal resistor-divider.

READ_OUTN is in the range of 0 to 2.56V with 2.5mV/bit resolution. This register refreshes at a 3.2ms rate.

V_{OUTN} = 30 × READ_OUTN<bit15-0> × 2.5mV/bit

READ_IPH1

The READ_IPH1 register returns the average voltage measured between CSP1 and CSN1, scaled up by a factor of 16.

READ_IPH1 ranges from 0 to 2.56V with 2.5mV/bit resolution. This register refreshes at a 3.2ms rate.

The average voltage between the CSP1 and CSN1 pins ($V_{AVG\_CSP1-CSN1}$) and the output current of the first phase are given by:

$$V_{AVG\_CSP1-CSN1} = \frac{READ\_IPH1<bit15\text{-}0> \times 2.5mV/bit}{16}$$

$$I_{OUT\_PH1} = \frac{V_{AVG\_CSP1-CSN1} \times (1 - D)}{R_{SENSE} \times D}$$

where:

R_{SENSE} = value of the sense resistor

D = duty cycle

READ_IPH2

The READ_IPH2 register returns the average voltage measured between CSP2 and CSN2, scaled up by a factor of 16.

READ_IPH2 ranges from 0 to 2.56V with 2.5mV/bit resolution. This register refreshes at a 3.2ms rate.

The average voltage between the CSP2 and CSN2 pins ($V_{AVG\_CSP2-CSN2}$) and the output current of the second phase are given by:

$$V_{AVG\_CSP2-CSN2} = \frac{READ\_IPH2<bit15\text{-}0> \times 2.5mV/bit}{16}$$

$$I_{OUT\_PH2} = \frac{V_{AVG\_CSP2-CSN2} \times (1 - D)}{R_{SENSE} \times D}$$

where:

R_{SENSE} = value of the sense resistor

D = duty cycle

STATUS_BYTE

The STATUS_BYTE register returns 1 byte of information of the device's fault conditions (see *Table 5*).

When a fault is detected, the corresponding bit is set. The fault bit can be cleared by cycling BIAS or CLEAR_FAULTS. The bit will immediately be set again if the fault remains.

Before the soft-start of the output, the EN/UVLO, CSION, and PGOOD signals are pulled low by the controller, and their corresponding bits are set and frozen as a fault. After power-up and the output is in regulation, a CLEAR_FAULTS command to reset these bits is necessary so they can record a future fault.

Table 5. STATUS_BYTE

BIT NUMBER	STATUS BIT NAME	MEANING
7	$\overline{CSION}$	"0" = CSION signal is high, "1" = CSION signal is low.
6	M/$\overline{S}$	"1" = MAX15258 is configured as a controller IC. "0" = MAX15258 is configured as a target IC.
5	FB_OV	FB OV fault has occurred.
4	PH2_OC	Phase2 OC fault (POCP/NOCP/FPOCP) has occurred.
3	PH1_OC	Phase1 OC fault (POCP/NOCP/FPOCP) has occurred.
2	$\overline{EN/UVLO}$	An EN/UVLO fault has occurred. "0" = EN/UVLO signal is high, "1" = EN/UVLO signal is low.
1	OT	An overtemperature fault has occurred.
0	$\overline{PGOOD}$	"0" = PGOOD signal is high-Z, "1" = PGOOD signal is low.

CLEAR_FAULTS

The CLEAR_FAULTS register is used to clear any fault bits that have been set in STATUS_BYTE. If the fault is still present, the fault bit is set again.

Inductor Selection

A larger inductor value results in reduced inductor ripple current, leading to a reduced inductor core loss. However, a larger inductor value results in either a larger physical size or a higher series resistance (DCR) and a lower saturation current rating. Typically, the inductor value is chosen to have current ripple (ΔI_L) around 50% of the average inductor current, which can be calculated by:

$$I_{L(AVE)} = \frac{I_{LOAD(MAX)}}{(1 - D) \times N}$$

where:

N = number of phases

The inductor can be chosen with the following formula:

$$L = \frac{D \times V_{IN}}{f_{SW} \times \Delta I_L}$$

Output Capacitor Selection

The output capacitors are selected to improve stability, output voltage ripple and load transient performance. To meet output voltage ripple (V_{RIPPLE}) requirement, the output capacitor can be selected by:

$$C_{OUT(RIPPLE)} = \frac{D \times I_{LOAD(MAX)}}{N \times f_{SW} \times V_{RIPPLE}}$$

For some applications, it is desired to limit output voltage overshoot and undershoot during load transient. To meet the load-transient requirement, the output capacitor can be selected by:

$$C_{OUT(TRANSIENT)} = \frac{\Delta I_{LOAD}}{3 \times BW \times \Delta V_{OUT}}$$

where:

ΔI_{LOAD} = load current step

BW = control loop bandwidth (see *Compensation Design Guidelines*)

ΔV_{OUT} = desired output voltage overshoot or undershoot

The final output capacitance should be selected as:

$C_{OUT} \geq$ maximum ($C_{OUT(RIPPLE)}$, $C_{OUT(TRANSIENT)}$)

Input Capacitor Selection

The input capacitors are selected to help reduce input voltage ripple (V_{IN_RIPPLE}). For boost converters, the input current is continuous. Neglecting ESR and ESL of the input capacitor, the input capacitor can be selected by:

$$C_{IN} = \frac{\Delta I_L}{8 \times N \times f_{SW} \times V_{IN\_RIPPLE}}$$

For inverting-buck-boost converters, the input current is discontinuous. The input capacitor can be selected by:

$$C_{IN} = \frac{D \times I_{LOAD(MAX)}}{N \times f_{SW} \times V_{IN\_RIPPLE}}$$

PCB Layout Guidelines

PCB layout can dramatically affect the performance of the power converter. A poorly designed board can degrade efficiency, thermal performance, noise control, and even control-loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors, inductor, MOSFETs, sense resistor, and output capacitors should be placed close together to minimize the high-frequency current path. The MOSFET driver should be placed close to the MOSFETs and the switching node (SW) to keep the gate drive, BST, and SW traces short. The MAX15258 should keep some distance from the high dv/dt SW, BST, and gate drive traces. The peripheral RC components should be placed as close

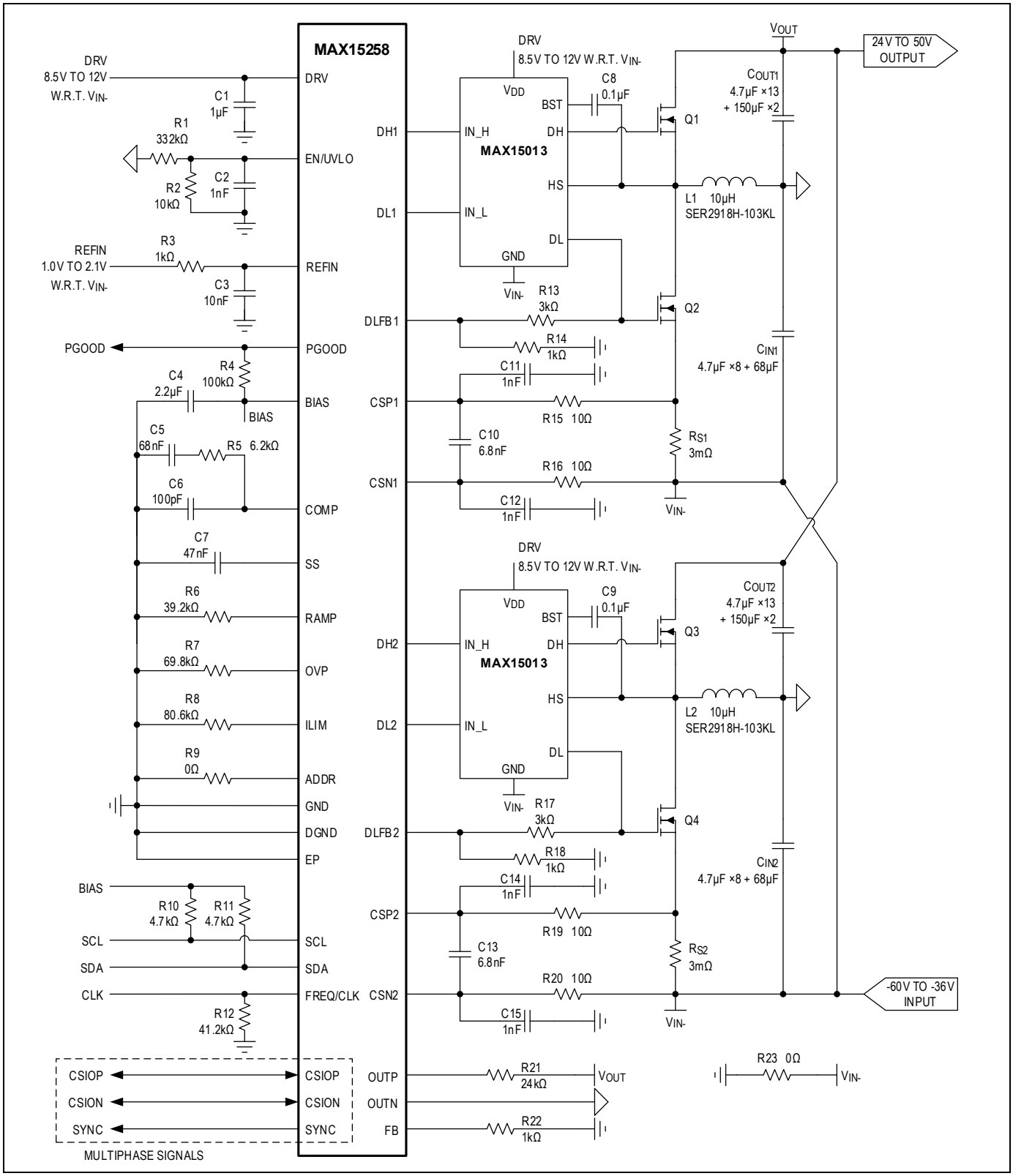
to the controller as possible. Priority should be given to the pins that are sensitive to noise (COMP, SS, REFIN, FB, etc.). It is suggested to place both differential-mode and common-mode filters between the CSP_ pin, CSN_ pin, and sense resistor (see the *Typical Application Circuits*).

For high-power applications, it is suggested to use planes for the power traces V_{IN}, V_{OUT}, and GND. It is important to have enough vias connecting the power planes in different layers. The signal and power grounds must be separated. All of the power components, including the input and output capacitors, MOSFETs, sense resistor, and MOSFET driver, should be connected to the power ground. The MAX15258 and its peripheral RC components must be connected to the signal ground. It is suggested to have an island of signal ground in the closest internal layer underneath the controller. Multiple vias can be used to connect the signal ground island to the exposed pad of the controller and the ground nodes of the noise-sensitive signal (COMP, SS, REFIN, FB, etc.). The signal ground should be tied to the power ground through a short trace or 0Ω resistor close to the power ground node of the sense resistor and input capacitors.

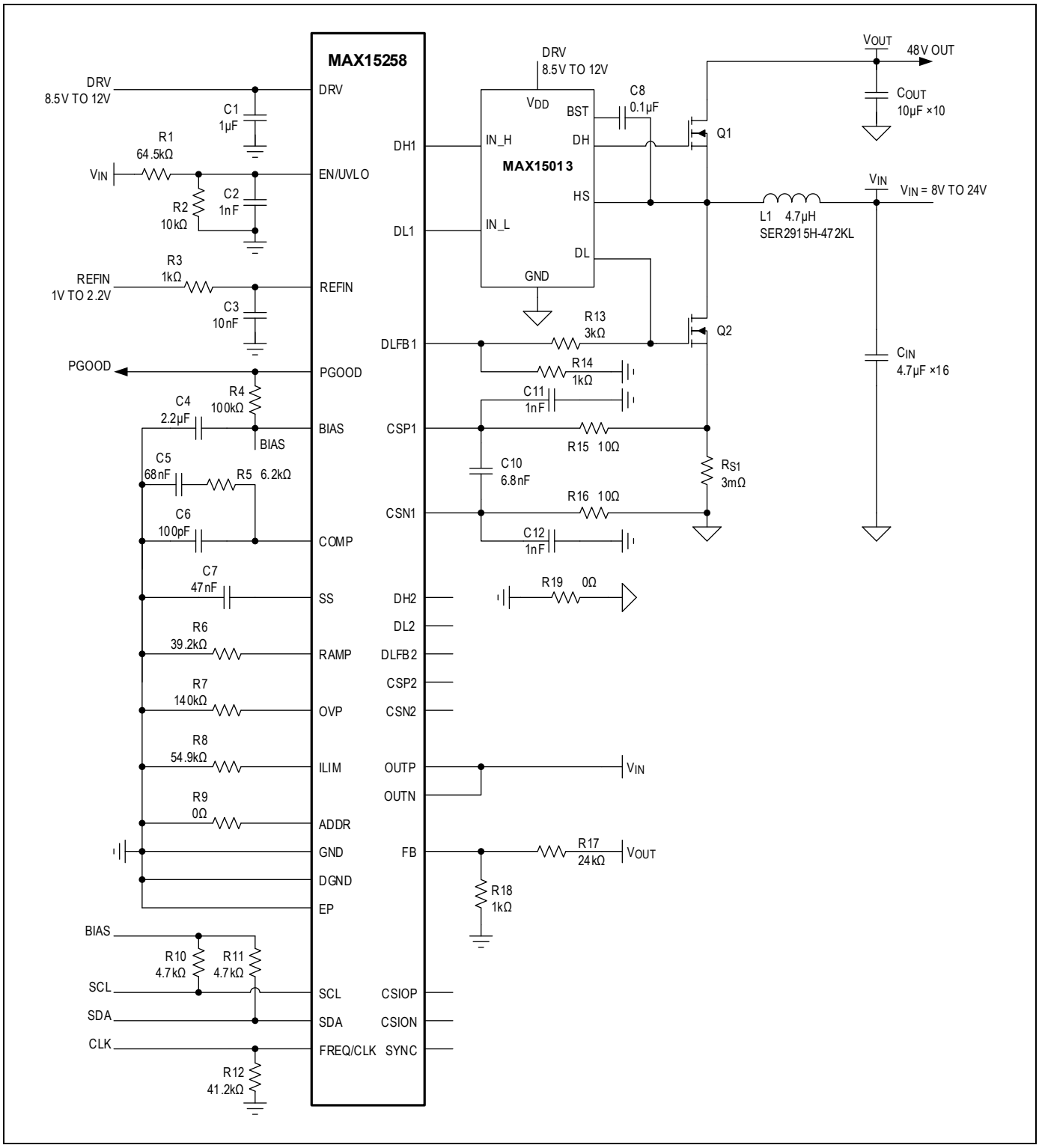
When the FB level shifter is used, the OUTP/OUTN sense lines must be routed differentially directly from the load points. The current sense lines from sense resistor to CSP_ and CSN_ should also be routed differentially. When the controller is configured to multiphase operation, the current sense lines of different phases should be kept apart to avoid signal coupling. Keep all sense lines and other noise-sensitive signals (CSIO_, COMP, SS, REFIN, FB, etc.) away from the noisy traces (SW, BST, gate drives, FREQ/CLK, SYNC, etc.).

Typical Application Circuits

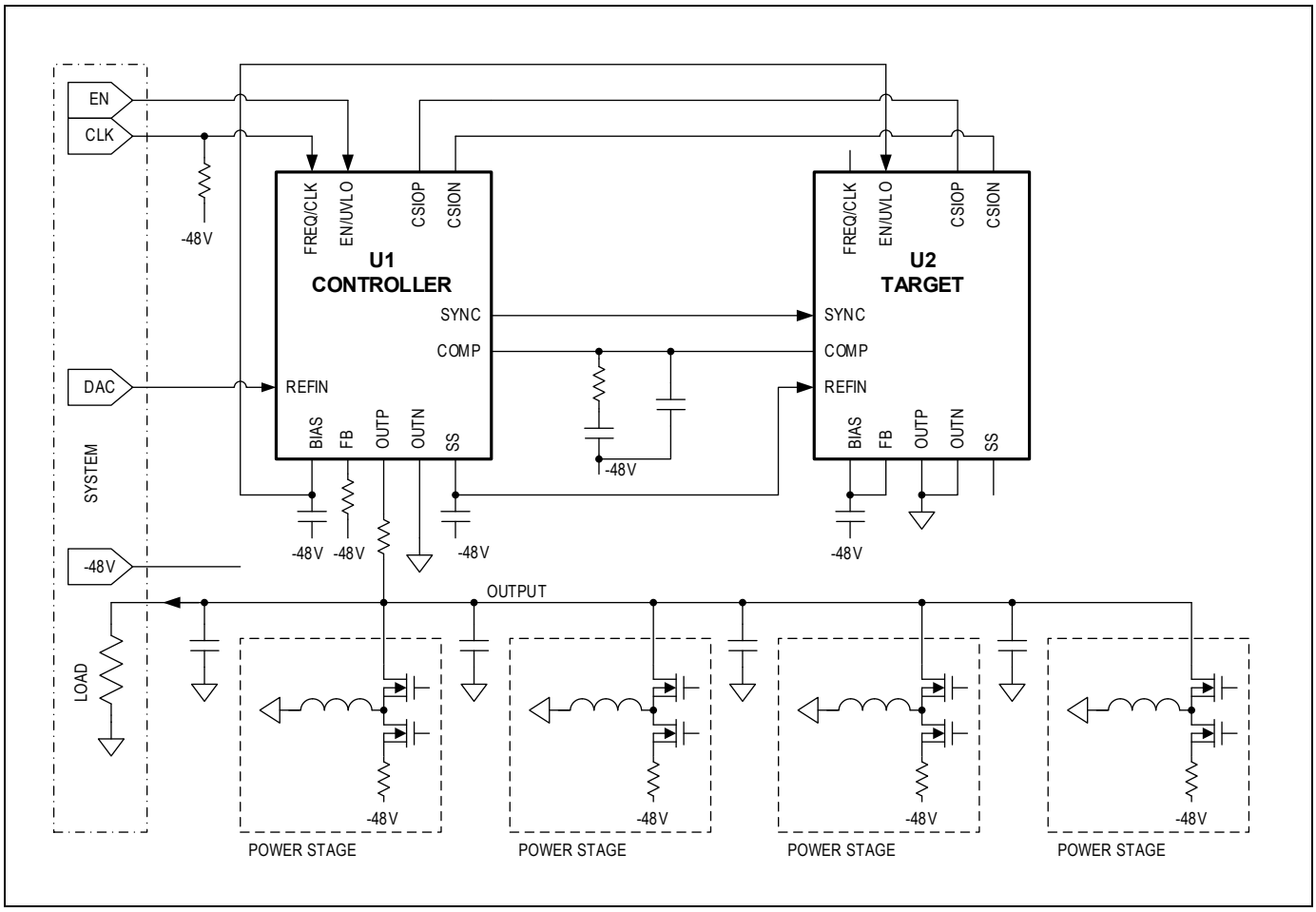
Dual-Phase Inverting-Buck-Boost Converter



Single-Phase Boost Converter



Quad-Phase Interconnects (Inverting-Buck-Boost Converter)



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX15258ATX+	-40°C to +125°C	36 TQFN-EP*
MAX15258ATX+T	-40°C to +125°C	36 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/22	Initial release	—
1	9/22	Updated Electrical Characteristics table, Pin Descriptions, and Detailed Description	5, 11, 12, 16, 18, 21