MAX15159

High-Voltage Multiphase Boost/Flyback Controller with No-Opto Feedback

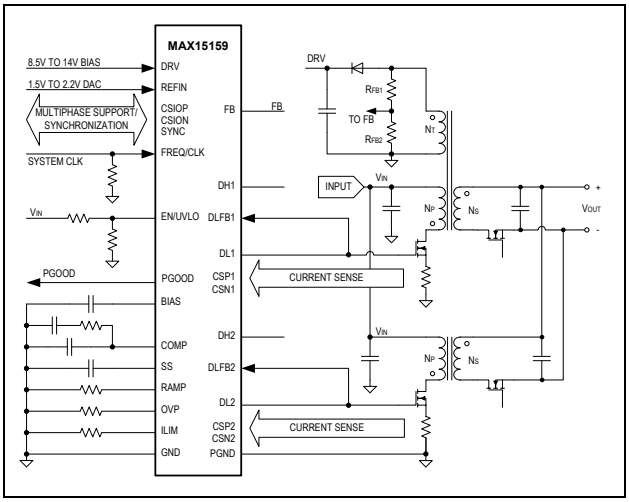
Product Highlights

- Wide Operating Range
  - 8V to 120V Input Voltage Range for Boost and Flyback Configuration, -8V to -120V Input Voltage Range for Inverting Buck-Boost Configuration
  - Single-/Dual-/Triple-/Quad-Phase Operation
  - 120kHz to 1MHz Switching Frequency Range
  - -40ºC to +125ºC Temperature Range
- Integration Reduces Design Footprint
  - Feedback Sample and Hold to Support No-Opto Feedback in Isolated Flyback Converter
  - Low-Side MOSFET Driver Integrated
  - Multiphase Synchronization and Interleaved Operation
  - Active Phase Current Balance Control
- Robust Fault Protection Improves Reliability
  - Adjustable Input Undervoltage Lockout (UVLO)
  - Adjustable Cycle-by-Cycle Peak Current Limit and Fast Overcurrent Protection (OCP)
  - Thermal Shutdown

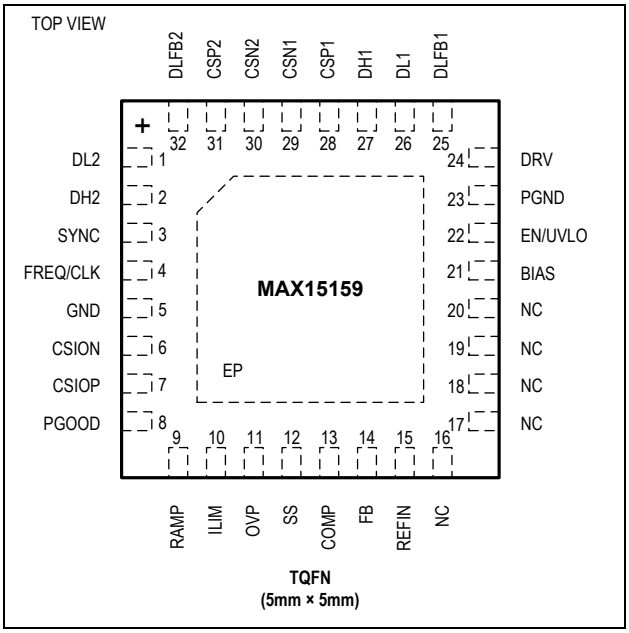
Key Applications

- Communication
- Industrial
- Multiphase Flyback
- IEEE802.3bt Powered Device

Simplified Application Diagram



Pin Configuration



***Ordering Information* appears at the end of the data sheet.**

19-101704; Rev 0; 5/23

Absolute Maximum Ratings

CSP_, CSN_ to GND ..... -0.3V to +0.3V

CSP_ to CSN_ ..... -0.3V to +0.3V

DH_ to GND ..... -0.3V to V_{BIAS} + 0.3V

DL_ to PGND ..... -0.3V to V_{DRV} + 0.3V

DLFB_ to GND ..... -0.3V to V_{DRV} + 0.3V

DRV to GND ..... -0.3V to +16V

BIAS to GND ..... -0.3V to +6V

DRV to BIAS ..... -0.3V to +16V

FB to GND ..... -6V to +6V

PGOOD, REFIN to GND ..... -0.3V to +6V

EN/UVLO, FREQ/CLK to GND ..... -0.3V to +6V

COMP, SS, ILIM to GND ..... -0.3V to V_{BIAS} + 0.3V

OVP, RAMP, SYNC to GND ..... -0.3V to V_{BIAS} + 0.3V

CSIOP, CSION to GND ..... -0.3V to V_{BIAS} + 0.3V

PGND to GND ..... -0.3V to +0.3V

Maximum Current out of BIAS 100mA

Operating Temperature Range ..... -40°C to +125°C

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C) 2.76W

Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T3255+4C
Outline Number	*21-0140*
Land Pattern Number	*90-0012*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	29 °C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.7 °C/W

Electrical Characteristics

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.5V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
DRV Operating Range	V_{DRV}		8.5		14	V
DRV Quiescent Current	I_{DRV}	Device switching, 2 phases, DH_ and DL_ unloaded		20	29	mA
DRV Shutdown Current	I_{DRV_SHDN}	EN/UVLO = GND		4.5	7	mA
DRV Undervoltage Lockout Threshold	$V_{DRV(UVLO)}$	V_{DRV} rising	8.1	8.25	8.4	V
		V_{DRV} falling	8	8.12	8.25	
BIAS LINEAR REGULATOR						
BIAS LDO Output Voltage	V_{BIAS}	I_{BIAS} = 5mA	4.9	5	5.1	V
BIAS LDO Current Limit	I_{BIAS}	V_{BIAS} = 3V	35	56	80	mA
BIAS Undervoltage Lockout Threshold	$V_{BIAS(UVLO)}$	V_{BIAS} rising, 230mV hysteresis	4.4	4.5	4.7	V
CONTROLLER ENABLE						
EN/UVLO Adjustable Undervoltage Lockout Threshold	V_{UVLO}	V_{UVLO} rising	0.98	1	1.03	V
		V_{UVLO} falling	0.88	0.9	0.93	
EN/UVLO Input Leakage Current	I_{UVLO}	V_{UVLO} = 0V to V_{BIAS}	-1		+1	µA
CONTROLLER LOOP						
FB Regulation Threshold (Preset Mode)	V_{FB}	REFIN = BIAS	1.985	2	2.015	V
FB-to-REFIN Offset Voltage (Tracking Mode)	V_{FB_OFS}	V_{REFIN} = 1.5V to 2.2V	-5		+5	mV
REFIN Input Voltage Range	V_{REFIN}	(*Note 2*)	1.5		2.2	V
Preset Mode REFIN Threshold Rising		100mV hysteresis (typ)	2.33	2.36	2.4	V
FB Input Leakage Current	I_{FB}	V_{FB} = 0V to 2.2V	-1.5		+1.5	µA
REFIN Input Leakage Current	I_{REFIN}	V_{REFIN} = 1.5V to 2.2V	-1		+1	µA
FB S/H Time	T_{SH}	FB sample time starts on the DLFB1 falling edge		210	320	ns
CSP_ to CSN_ Differential Voltage Range	$D_{VCS\_}$	$V_{CSP\_}$ - $V_{CSN\_}$	-200		+200	mV
Current-Sense Common-Mode Voltage Range	$V_{CSP\_}$, $V_{CSN\_}$	With respect to GND (*Note 3*)	-300		+300	mV

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.5V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSP_, CSN_ Current-Sense Amplifier Gain	$A_{CS\_}$		4.1	4.4	4.7	V/V
CSP_, CSN_ Input Leakage Current	$I_{CSP\_}$, $I_{CSN\_}$	$V_{CSP\_}$, $V_{CSN\_}$ = ±300mV with respect to GND	-3		+3	µA
Error Amplifier Transconductance	G_{MEA}		0.8	1.15	1.5	mS
RAMP Pin Amplitude Adjustable Range	V_{RAMP}		130		730	mV
Internal Slope Compensation Ramp Voltage to V_{RAMP} Ratio		V_{RAMP} = 0.3V		2		V/V
RAMP Bias Current	I_{RAMP}	V_{RAMP} = 0V	9.7	10	10.3	µA
SWITCHING FREQUENCY						
Preset PWM Switching Frequency	f_{SW}	R_{FREQ} = OPEN, V_{OVP} = 0V	293	300	307	kHz
Adjustable PWM Switching Frequency	f_{SW}	R_{FREQ} = 20kΩ, V_{OVP} = 0V	108	115	123	kHz
		R_{FREQ} = 25kΩ, V_{OVP} = 0V	138	145	153	
		R_{FREQ} = 100kΩ, V_{OVP} = 0V	580	602	622	
PWM Switching Frequency Range	f_{SW}	FREQ/CLK externally applied	120		1000	kHz
FREQ/CLK Frequency Detection Range	f_{CLK}		0.48		4	MHz
FREQ/CLK Logic Level	V_{CLK}	Logic-high (rising)		1.8	1.9	V
		Logic-low (falling)	1.5	1.6		
FREQ/CLK Input Bias Current	I_{CLK}	$V_{FREQ/CLK}$ = GND	-10.2	-10	-9.8	µA
FREQ/CLK to PWM Switching Frequency Ratio	f_{CLK}/f_{SW}	1-/2-/4-phase operation		4		kHz/kHz
		3-phase operation		3		
SYNCHRONIZATION						
SYNC Logic Threshold	V_{SYNC}	Logic-high (rising)		1.6	1.95	V
		Logic-low (falling)	0.9	1.2		
SYNC Input Leakage Current	I_{SYNC}	V_{SYNC} = 0V to 4.6V, internal 5MΩ pulldown	-2		+2	µA
SYNC Frequency Range	f_{SYNC}		200		2000	kHz
SYNC Output Voltage Level	V_{SYNC}	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} – 0.4			V
		Logic-low, I_{SINK} = 10mA			0.4	
OUTPUT FAULT PROTECTION						
ILIM Source Current			9.6	10	10.4	µA

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.5V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ILIM} to |CSP_ - CSN_| Cycle-by-Cycle Positive Peak Current-Limit Threshold Ratio				10		V/V
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} = 0V	17	20	23	mV
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Positive Peak Current Limit		V_{ILIM} > 1.25V	94	100	106	mV
CSP_ to CSN_ Minimum Threshold for Cycle-by-Cycle Negative Peak Current Limit		V_{ILIM} > 1.25V	-90	-80	-68	mV
CSP_ to CSN_ Maximum Threshold for Cycle-by-Cycle Negative Peak Current Limit		V_{ILIM} = 0V	-22	-16	-10	mV
CSP_ to CSN_ Minimum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} = 0V	21	26	31	mV
CSP_ to CSN_ Maximum Threshold for Fast Positive Overcurrent Protection		V_{ILIM} > 1.25V	121	133	145	mV
CSP_ to CSN_ Cycle-by-Cycle Positive Peak Current-Limit Threshold Accuracy		0.25V < V_{ILIM} < 0.95V	-10		+10	%
		V_{ILIM} = 500mV	-3		+3	
CSP_ to CSN_ Negative Overcurrent Protection Threshold Accuracy		V_{ILIM} = 500mV	-18		+18	%
FB Overvoltage Default Threshold (Preset Mode)	FB OV	Measured with respect to target voltage (REFIN = BIAS), V_{FB} rising, 3% hysteresis	9	10	11	%
FB Overvoltage Threshold (Tracking Mode)	FB OV	Measured with respect to target voltage (REFIN = 2V), V_{FB} rising, 3% hysteresis	9	10	11	%
OVP Selector Output Source Current		Resistor connected to GND	9.6	10	10.4	µA
		EN/UVLO rising to SS rising		32		µs

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.5V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN/UVLO Propagation Delay		EN/UVLO falling to SS falling	7	13	21	
Fault Propagation Delay		Cumulative cycle-by-cycle peak current limit or negative overcurrent protection events for hiccup		32		events
		FB OV		128		PWM CLK cycles
Hiccup Timeout Duration				32,768		PWM CLK cycles
Thermal Shutdown	T_{SHDN}	15°C hysteresis (*Note 3*)		165		°C
PGOOD						
PGOOD Threshold		PGOOD rising (REFIN = BIAS)	1.86	1.88	1.9	V
		PGOOD falling (REFIN = BIAS)	1.8	1.82	1.84	
PGOOD Falling and Rising Delay				64		PWM CLK cycles
PGOOD Output Low Voltage	V_{PGOOD}	I_{SINK} = 3mA		20	40	mV
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN, V_{PGOOD} = 5V			1	µA
SOFT-START (SS)						
SS Pull-Up Current	I_{SS}	Source	9.6	10	10.4	µA
SS Pull-Down Resistance	R_{SS}	Discharge		5.5	10	Ω
PWM OUTPUT						
DH_ Output Voltage Level	$V_{DH\_}$	Logic-high, I_{SOURCE} = 10mA	V_{BIAS} – 0.3			V
		Logic-low, I_{SINK} = 10mA			0.15	
DL_ Output Voltage Level	$V_{DL\_}$	Logic-high, I_{SOURCE} = 20mA	V_{DRV} – 0.4			V
		Logic-low, I_{SINK} = 20mA			0.1	
DL_ Driver Peak Current	I_{DL_SOURCE}	Source current		1		A
	I_{DL_SINK}	Sink current		2		
DH_ Minimum Off-Time	$T_{OFF\_DH\_}$			85	125	ns
DL_ Minimum On-Time	$T_{ON\_DL\_}$			52	90	ns
DLFB_ Leakage Current	I_{LK}	$V_{DLFB\_}$ = 9V	-1		+1	µA
DLFB_ Logic Threshold	$V_{DLFB\_}$	Logic-high (rising)	0.75	0.8	0.85	V
		Logic-low (falling)	0.45	0.5	0.55	
CURRENT SHARING (MULTIPHASE APPLICATIONS ONLY)						

(V_{DRV} = 9V, $V_{EN/UVLO}$ = 1.5V, REFIN = BIAS, C_{BIAS} = 2.2µF, C_{SS} = 10nF, R_{FREQ} = 100kΩ (600kHz), T_A = T_J = -40°C to +125°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSION Output Voltage	V_{CSION}	With respect to GND		1.24		V
CSIO_ Differential Input Resistance	$R_{CSIO\_}$			3.8		kΩ

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

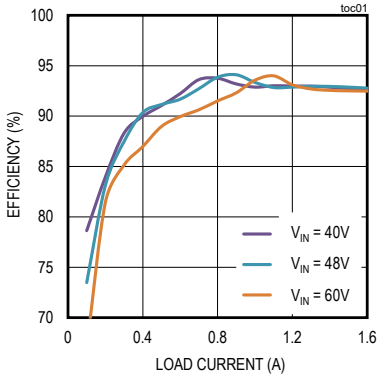
Note 2: Operating REFIN below 1.5V is not allowed. PWM is disabled when REFIN < 1.47V.

Note 3: Guaranteed by design, not production tested.

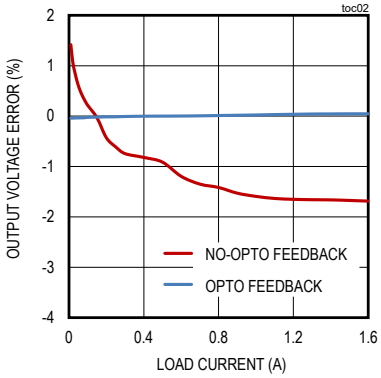
Typical Operating Characteristics

(T_A = +25ºC, V_{IN} = 48V, V_{OUT} = 54V, unless otherwise noted. See the *Typical Application Circuits*.)

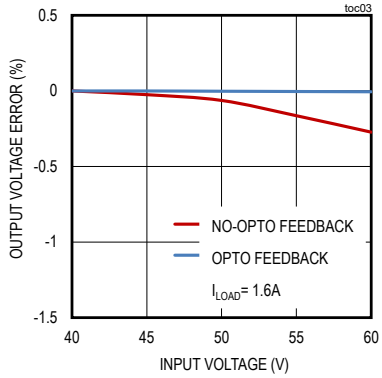
EFFICIENCY



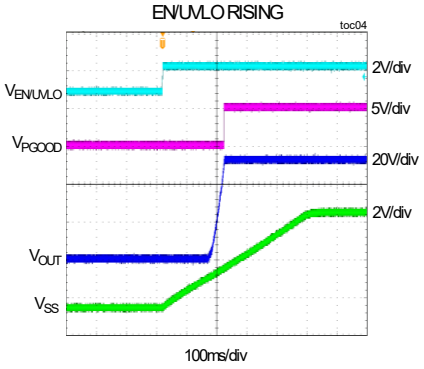
LOAD REGULATION



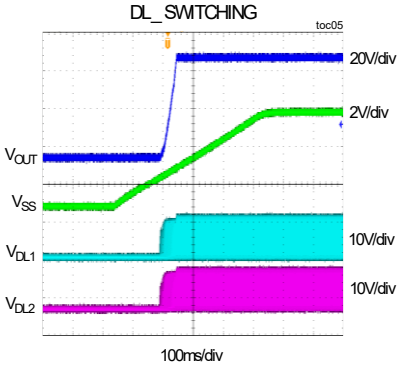
LINE REGULATION



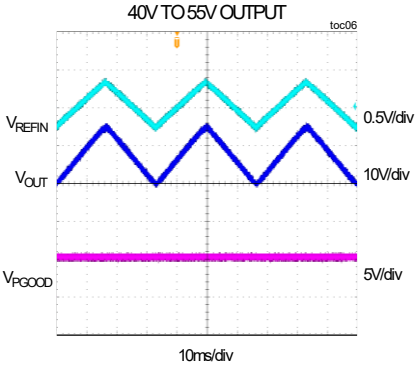
STARTUP WAVEFORM
EN/UVLO RISING



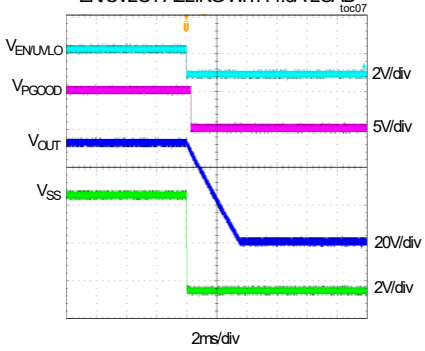
STARTUP WAVEFORM
DL_ SWITCHING



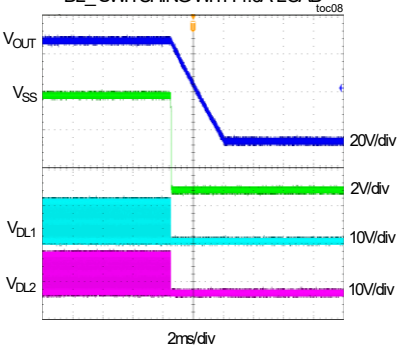
DYNAMIC REFIN RAMP RESPONSE
40V TO 55V OUTPUT



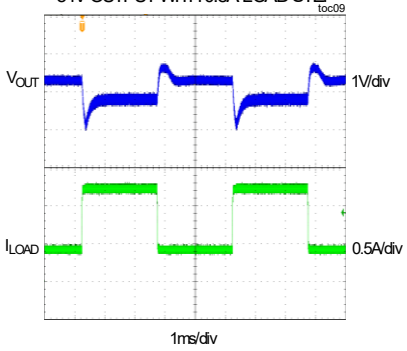
SHUT-DOWN WAVEFORM
EN/UVLO FALLING WITH 1.6A LOAD



SHUT-DOWN WAVEFORM
DL_ SWITCHING WITH 1.6A LOAD

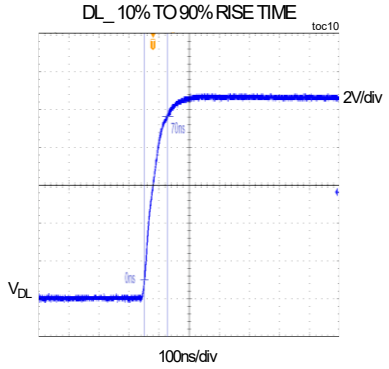


LOAD TRANSIENT WAVEFORM
54V OUTPUT WITH 0.8A LOAD STEP

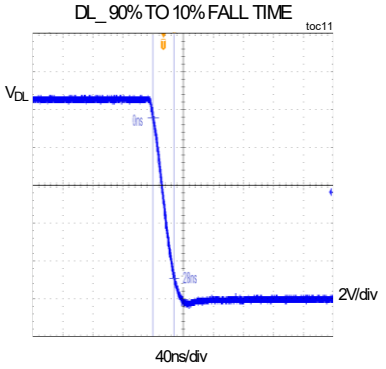


(T_A = +25ºC, V_{IN} = 48V, V_{OUT} = 54V, unless otherwise noted. See the *Typical Application Circuits*.)

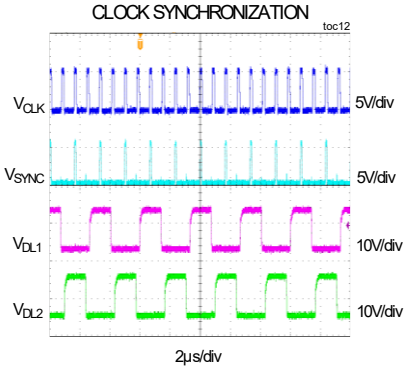
DL_ 10% TO 90% RISE TIME



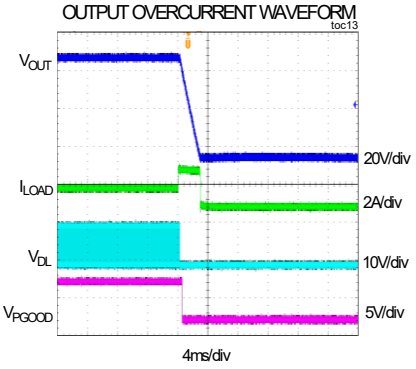
DL_ 90% TO 10% FALL TIME



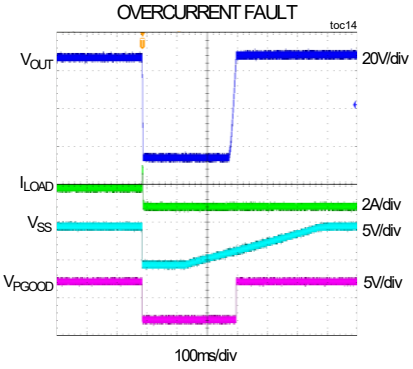
CLOCK SYNCHRONIZATION



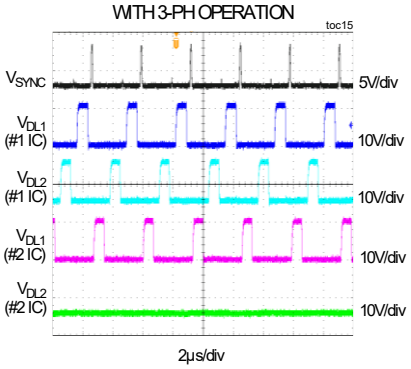
OUTPUT OVERCURRENT WAVEFORM



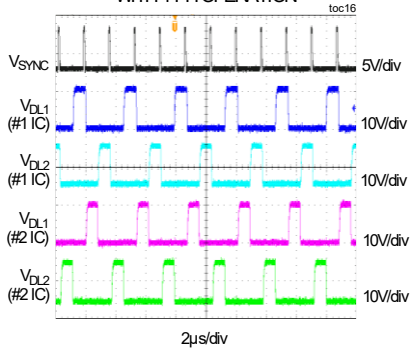
AUTO-RETRY AFTER OVERCURRENT FAULT



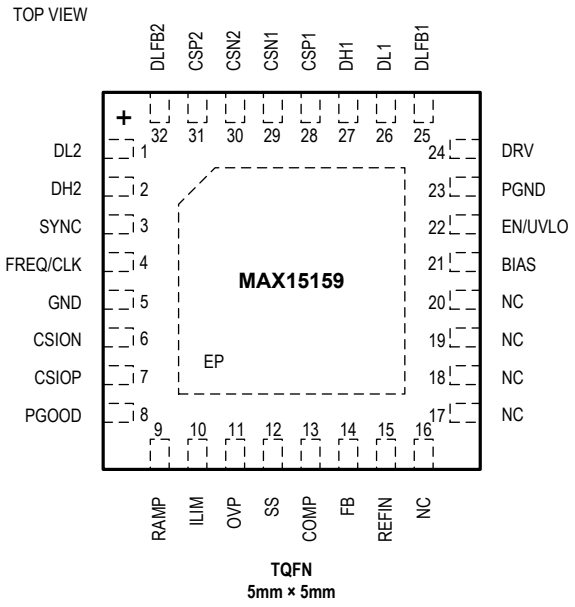
DL_ PHASE SHIFT WITH 3-PH OPERATION



DL_ PHASE SHIFT WITH 4-PH OPERATION



Pin Configurations

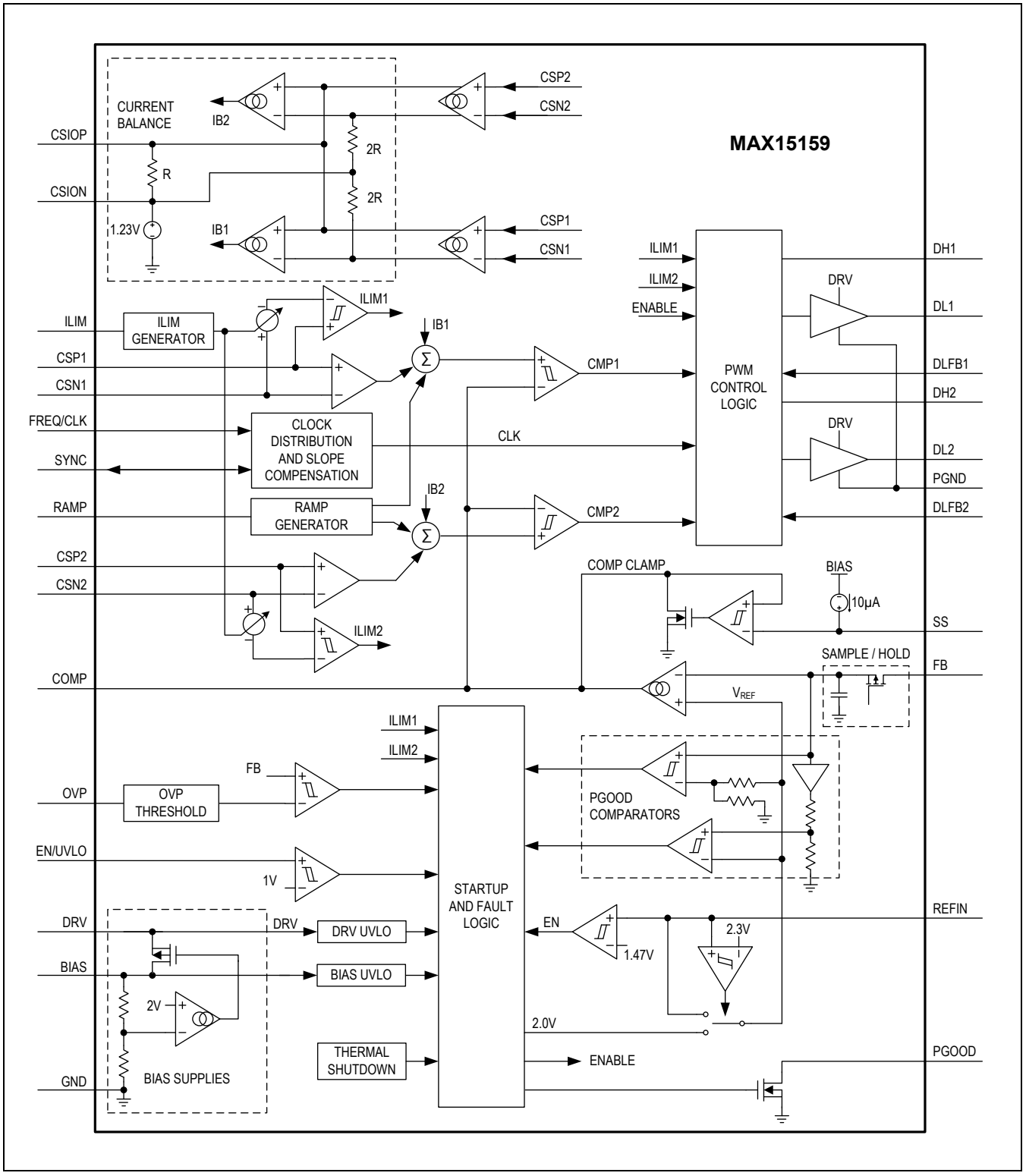


Pin Descriptions

PIN	NAME	FUNCTION
1	DL2	Gate Driver Output for Low-Side MOSFET for the Second Phase. DL2 switches between DRV and PGND.
2	DH2	Logic Output for High-Side MOSFET Gate Driver for the Second Phase. Connect DH2 to the high-side input pin of second-phase external MOSFET driver. DH2 switches between BIAS and GND.
3	SYNC	Multiphase Synchronization Pin. For single-IC operation, leave this pin unconnected. Tie this pin together when two ICs are stacked-up in controller/target operation mode.
4	FREQ/CLK	Frequency Selection/Clock Synchronization Input. The MAX15159 supports switching frequencies from 120kHz to 1MHz. Set the switching frequency by either selecting the appropriate external resistor to use the internal oscillator frequency, or by synchronizing the regulator to an external system clock (see *Table 2*). Leave the FREQ/CLK pin unconnected to select the preset 300kHz switching frequency, or place a resistor between FREQ/CLK and GND to set the following: $f_{SW} = (R_{FREQ}/100k\Omega) \times 600kHz$.
5	GND	Analog Ground.
6	CSION	Negative Input of Controller/Target Current-Sense Signal. The MAX15159 uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15159 ICs are stacked up in controller/target operation mode.
7	CSIOP	Positive Input of Controller/Target Current-Sense Signal. The MAX15159 uses a differential current-sense signal to ensure proper startup and current-balance behavior in applications where two MAX15159 ICs are stacked up in controller/target operation mode.
8	PGOOD	Open-Drain Power-Good Output. The MAX15159 pulls PGOOD low when the output voltage exceeds the OVP threshold during soft-start and shutdown (EN/UVLO pulled low). The PGOOD output goes high-impedance when the controller completes soft-start and remains in regulation. Leave PGOOD of the target IC unconnected in controller/target operation mode.
9	RAMP	Slope Compensation Input. A resistor connected from RAMP to GND programs the amount of slope compensation. See the *Adjustable Slope Compensation (RAMP)* section.
10	ILIM	CSP_ - CSN_ Cycle-by-Cycle/Hiccup Current-Limit Threshold Selector. Connect a resistor from ILIM to GND to select the protection value.
11	OVP	Program Pin. Connect a resistor from OVP to GND to configure FB overvoltage protection, and multiphase selection (see *Table 1*).
12	SS	Soft-Start Control. The capacitance (C_{SS}) between SS to GND sets the startup period. An internal pull-down MOSFET holds SS low until the controller begins the startup sequence.

13	COMP	Compensation Amplifier Output. COMP is the output of the internal transconductance error amplifier. Connect a Type II compensation network, as shown in the *Typical Application Circuits*. (Also see the *Compensation Design Guidelines* section).
14	FB	Feedback Input. Connect FB to the center of a resistor-divider across the tertiary winding in a Flyback converter for no-opto feedback. When two MAX15159 ICs are stacked-up in controller/target operation mode, connect FB of the target IC to BIAS.
15	REFIN	External Reference Input. REFIN sets the FB regulation voltage when supplied with a voltage between 1.5V and 2.2V. Connect the REFIN pin to BIAS to select the internal 2.0V reference voltage. Less than 1.45V (typ) falling threshold on REFIN pin disables the IC and stops PWM operation.
16, 17, 18, 19, 20	NC	Not Connected.
21	BIAS	5V Linear Regulator Output and Controller Bias Supply. Bypass to GND with a 2.2µF or greater ceramic capacitor.
22	EN/UVLO	Enable Control/Adjustable Undervoltage Lockout Input for Startup/Shutdown Power Sequencing. Connect EN/UVLO to the center of a resistor-divider between the input and GND to adjust the undervoltage lockout voltage level, as shown in the *Typical Application Circuits*.
23	PGND	Power Ground. PGND is the return path of the DL_ gate driver switching current. Connect it directly to system ground plane.
24	DRV	Supply Voltage Input. Provide a 8.5V to 14V supply for internal bias generation.
25	DLFB1	External MOSFET Status Feedback Pin for the First Phase. Connect DLFB1 to the center of a resistor-divider between the gate of the first-phase low-side MOSFET and GND. See the *MOSFET Gate Control* section.
26	DL1	Gate Driver Output for Low-Side MOSFET for the First Phase. DL1 switches between DRV and PGND.
27	DH1	Logic Output for High-Side MOSFET Gate Driver for the First Phase. Connect DH1 to the high-side input pin of the first-phase external MOSFET driver. DH1 switches between BIAS and GND.
28	CSP1	Positive Low-Side Differential Current-Sense Input for the First Phase. The MAX15159 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSP1 to the MOSFET side of the current-sense resistor.
29	CSN1	Negative Low-Side Differential Current-Sense Input for the First Phase. The MAX15159 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSN1 to the ground side of the current-sense resistor.
30	CSN2	Negative Low-Side Differential Current-Sense Input for the Second Phase. The MAX15159 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSN2 to the ground side of the current-sense resistor.
31	CSP2	Positive Low-Side Differential Current-Sense Input for the Second Phase. The MAX15159 uses the differential current-sense signal in the current-mode control loop and multiphase current sharing. Connect CSP2 to the MOSFET side of the current-sense resistor.
32	DLFB2	External MOSFET Status Feedback Pin for the Second Phase. Connect DLFB2 to the center of a resistor-divider between the gate of the second-phase low-side MOSFET and GND. See the *MOSFET Gate Control* section.
-	EP	Exposed Pad. Connect to GND.

Functional Diagrams



Detailed Description

The MAX15159, a high-voltage, multiphase boost/flyback controller with enhanced low-side MOSFET gate driver capability, is designed to support single-phase or dual-phase boost/flyback configurations. Two devices can be stacked up for triple-phase or quad-phase operation. The output voltage can be dynamically set through the 1.5V to 2.2V reference input (REFIN) for modular design support.

The switching frequency is controlled either through an external resistor setting the internal oscillator or by synchronizing the regulator to an external clock. The device is designed to support 120kHz to 1MHz switching frequencies. When two devices are stacked up as controller-target for triple-phase or quad-phase operation, the SYNC pins of two devices are connected to ensure clock synchronization and phase interleaving. The controller has a dedicated enable/input undervoltage lockout (EN/UVLO) pin to configure for flexible power sequencing.

The MAX15159 has a dedicated RAMP pin to adjust internal slope compensation. The device features adjustable overcurrent protection through the dedicated ILIM pin. The device incorporates current-sense amplifiers to accurately measure the current of each phase across external sense resistors to implement accurate phase current sharing. The controller is also protected against output overvoltage, input undervoltage, and thermal shutdown.

No-Opto Feedback

Thanks to the internal sample/hold circuitry at FB pin, the MAX15159 supports no-opto feedback when operating in an isolated Flyback, which could save an optocoupler and secondary feedback circuits. The FB pin is connected to the center of a resistor-divider across the tertiary winding. In the case of multiphase operation, this tertiary winding must be a winding of the transformer in Phase1 of controller IC, as shown in *Figure 1*.

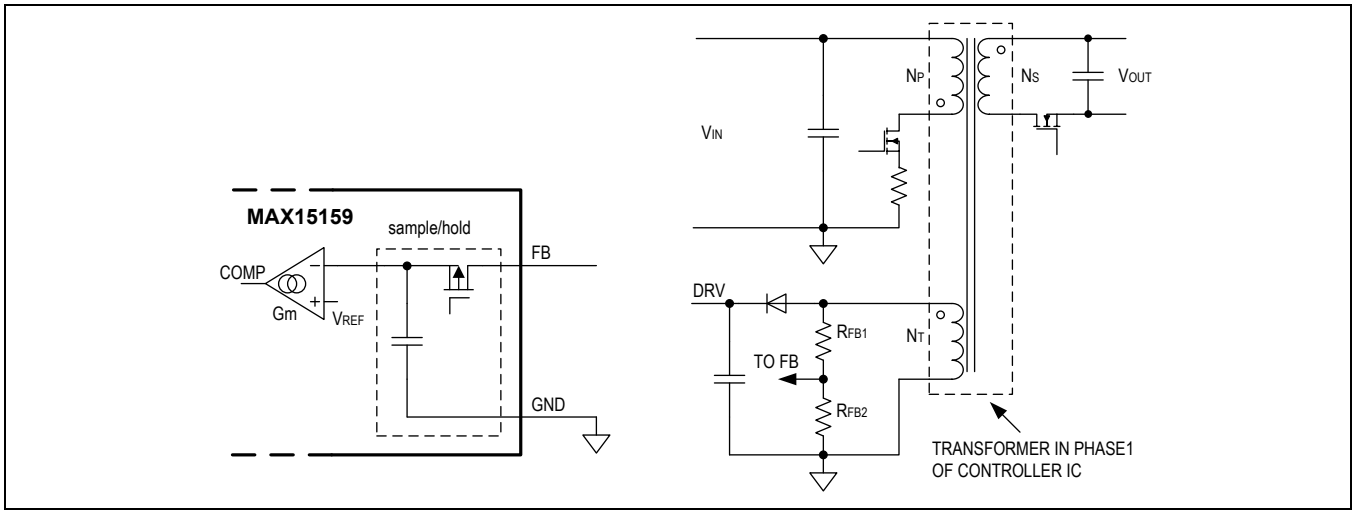


Figure 1. No-Opto Feedback in a Flyback Converter

The output voltage is given by the following equation:

$V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times V_{REF} \times N_S/N_T$

V_{REF} can be externally supplied with a voltage between 1.5V and 2.2V at the REFIN pin. By connecting the REFIN pin to BIAS, the default internal 2.0V reference voltage is selected.

During on-time, a negative voltage on FB pin is given by the following equation:

$V_{FB-ON} = - [R_{FB2}/(R_{FB1} + R_{FB2})] \times V_{IN} \times N_T/N_P$

Care must be taken to ensure that this negative voltage at FB pin is within its Absolute Maximum Rating.

where:

V_{IN} = input voltage

N_S/N_T = transformer secondary-to-tertiary turns ratio

N_T/N_P = transformer tertiary-to-primary turns ratio

Especially with light output load condition in a secondary diode rectifier flyback converter, the secondary winding current discharge duration could be minimal, causing significant errors in the sampled V_{OUT} voltage if internal sample/hold ends after the complete decay of the secondary winding energy. Then an additional RCD circuit is suggested, helping hold the sampled voltage across the tertiary winding, see *Figure 2*. Its output voltage is given by the following equation:

$$V_{OUT} = [(1 + R_{FB1}/R_{FB2}) \times V_{REF} + V_{D\_FB}] \times N_S/N_T - V_{D\_REC}$$

where:

V_{D_FB} = forward voltage of diode D_{FB} (*Figure 2)*

V_{D_REC} = forward voltage of output rectifier diode D_{REC} (*Figure 2)*

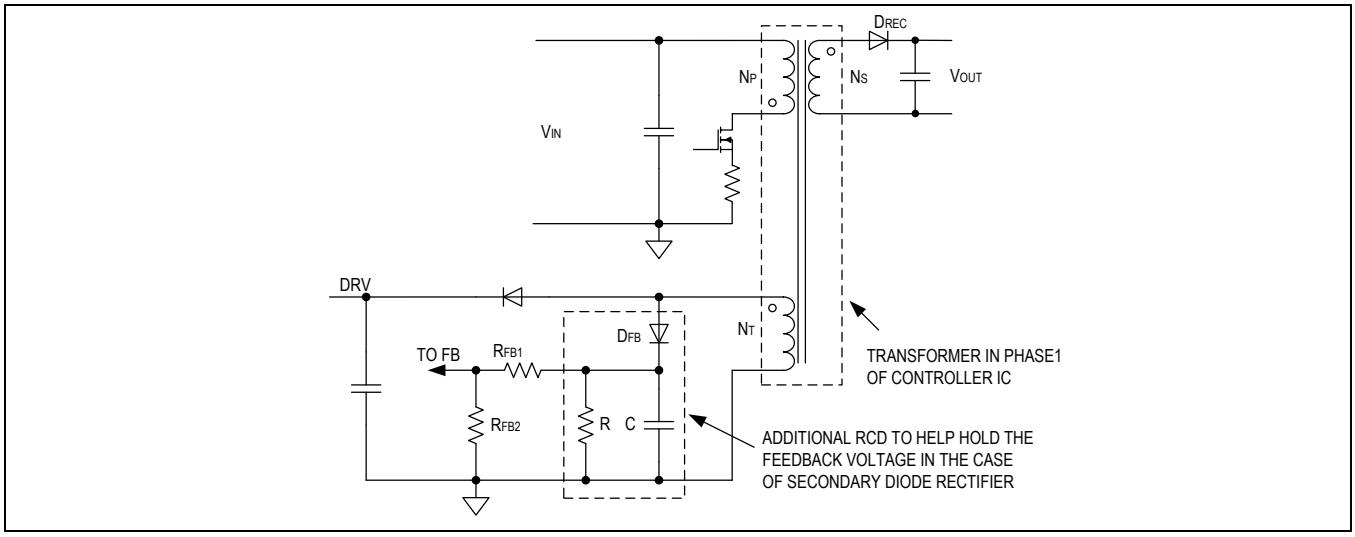


Figure 2. No-Opto Feedback with Additional RCD across Tertiary Winding

Boost/Inverting Buck-Boost Application

The MAX15159 can support both boost and inverting buck-boost applications.

When configured in inverting buck-boost operation, the GND pin of the device must be connected to the negative input voltage terminal (V_{IN-}), so that the ground of the IC is different than the ground of the output capacitor and load. Output voltage cannot be controlled using a simple resistor-divider, and an external FB level shifter consists of two matched PNP transistors, as shown in *Figure 3(a)*.

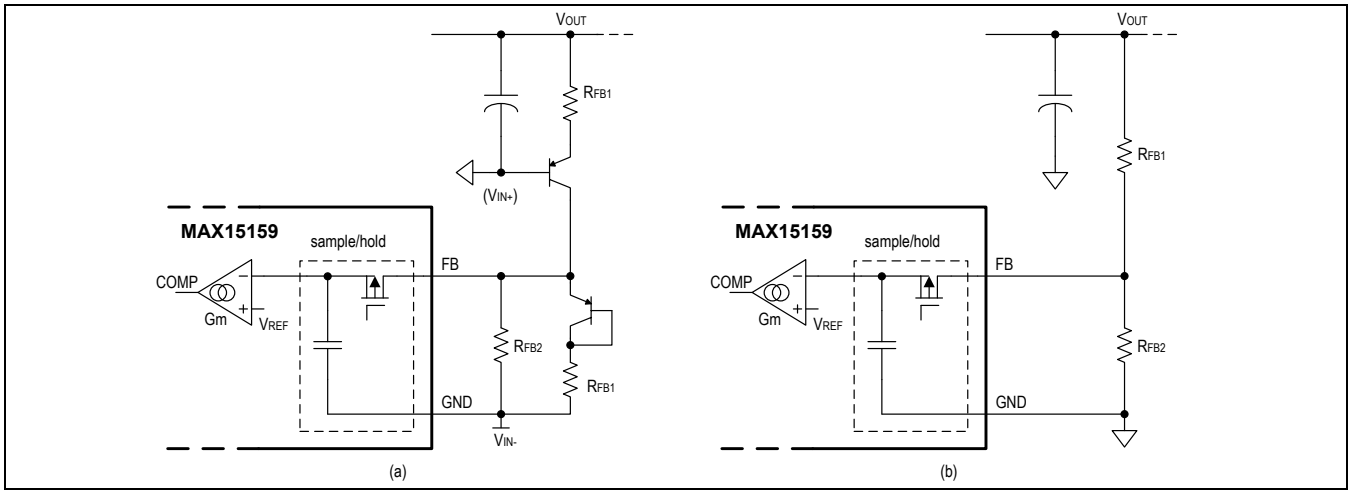


Figure 3. FB Connection in (a) Inverting Buck-Boost Application with External FB Level Shifter (b) Boost Application

The output voltage for boost and inverting buck-boost is given by the following equation:

$V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times V_{REF}$

where:

V_{REF} = reference voltage for FB regulation, set by REFIN pin

Peak-Current-Mode Control Loop

The controller relies on a fixed-frequency, peak-current-mode architecture to regulate the output. A detailed block diagram of the control loop is shown in *Figure 4*. A sense resistor is required between the source of the low-side MOSFET and GND for current sensing. The sense resistor should be selected so that the maximum differential voltage across CSP_ and CSN_ does not exceed the cycle-by-cycle peak current-limit threshold (see the *Overcurrent Protection* section). The differential voltage across CSP_ and CSN_ is amplified 4.4 times by an internal current-sense amplifier, and summed to the internal PWM slope compensation ramp, used to generate the controller PWM output. A high-frequency RC noise filter is suggested across the sense resistor.

The error between the output voltage feedback (V_{FB}) and reference voltage (V_{REFIN} or internal 2V) is fed to the input of an error amplifier. The output of error amplifier (COMP) is required to connect to a Type II compensation network for control loop stability (see the *Compensation Design Guidelines* section). Particularly, the COMP voltage is also controlled by the SS voltage. During startup, the MAX15159 charges the SS capacitor (C_{SS} in *Figure 4*) with a constant 10µA current source, SS voltage rises up linearly, which allows COMP voltage to ramp up linearly with a controlled rate and allows duty cycle and peak current to increase gradually. Then, the output voltage ramps up monotonically until it reaches its regulation setpoint. Connecting a resistor (R_{SS} in *Figure 4*) between SS and GND can set the maximum voltage on SS, consequently, clamps the COMP voltage to set the maximum duty cycle and maximum peak current.

A slope compensation ramp generator is also used. The slope of the compensation ramp can be adjusted by connecting a resistor between RAMP and GND (see the *Adjustable Slope Compensation (RAMP)* section).

The controller drives on the low-side MOSFET (DL_ driven high) on each rising clock edge. The controller pulls DL_ low and drives DH_ high when the PWM comparator detects that the sum of the current-sense amplifier output ($V_{CS\_}$), the slope compensation ramp, and the phase current imbalance signal exceeds the COMP voltage.

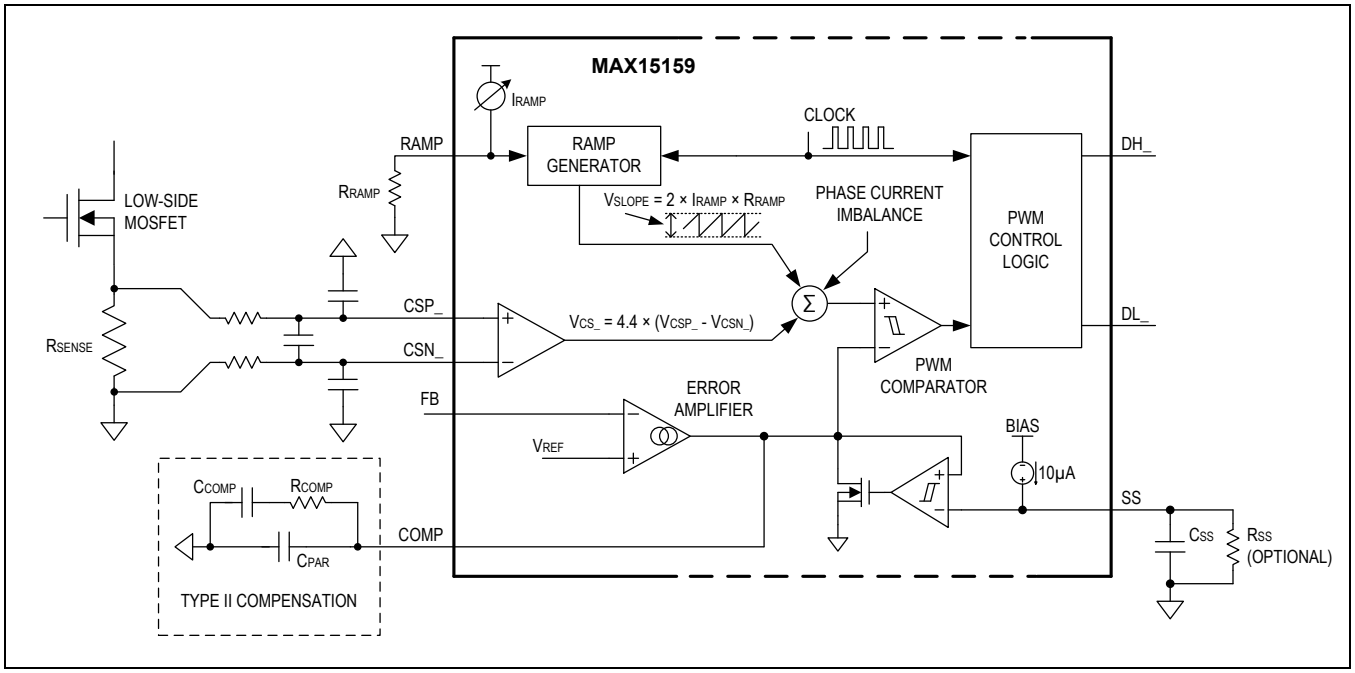


Figure 4. Peak-Current-Mode Control Loop

Compensation Design Guidelines

The MAX15159 utilizes a fixed-frequency, peak-current-mode control scheme to provide easy compensation and fast-transient response. It is by design for boost/inverting buck-boost/flyback converters to have a right half plane (RHP) zero in their small signal control-to-output transfer function.

For boost converters, the location of RHP zero is calculated by the following equation:

$$f_{RHP} = \frac{V_{OUT} \times (1-D)^2}{2 \times \pi \times I_{OUT(MAX)} \times L}$$

where:

$I_{OUT(MAX)}$ = maximum load current per phase

D = duty cycle = $1 - V_{IN}/V_{OUT}$

L = value of the inductor

For inverting buck-boost/flyback converters, the location of RHP zero is calculated by the following equation:

$$f_{RHP} = \frac{V_{OUT} \times (1-D)^2 \times (N_P/N_S)^2}{2 \times \pi \times I_{OUT(MAX)} \times L \times D}$$

where:

D = duty cycle = $(N_P/N_S \times V_{OUT})/[|V_{IN}| + (N_P/N_S \times V_{OUT})]$

N_P/N_S = transformer primary-to-secondary turns ratio for flyback converter, select N_P/N_S = 1 for inverting buck-boost converter

For stable operation, it is required that the bandwidth of control loop (BW) be sufficiently lower than f_{RHP} and the switching frequency (f_{SW}):

BW ≤ minimum($f_{RHP}/7$, $f_{SW}/10$)

A Type II compensation network is required to be connected between COMP and GND (R_{COMP}, C_{COMP}, and C_{PAR} in *Figure 4*) to provide sufficient phase margin and gain margin to the control loop.

R_{COMP} for boost converter can be selected by the following equation:

$$R_{COMP} = \frac{2 \times \pi \times BW \times C_{OUT} \times A_{CS} \times R_{SENSE} \times V_{OUT}}{N \times G_{MEA} \times V_{REF} \times (1 - D)}$$

where:

R_{SENSE} = value of the sense resistor

C_{OUT} = value of the output capacitor

N = number of phases

G_{MEA} = error amplifier transconductance (1.15mS, typ)

A_{CS} = current-sense amplifier gain (4.4V/V, typ)

R_{COMP} for inverting buck-boost/flyback converter can be selected by the following equation:

$$R_{COMP} = \frac{2 \times \pi \times BW \times C_{OUT} \times A_{CS} \times R_{SENSE} \times V_{OUT}^2}{N \times G_{MEA} \times V_{REF} \times D \times V_{IN}}$$

C_{COMP} and C_{PAR} can be selected by the following equation:

$$C_{COMP} = \frac{5}{\pi \times R_{COMP} \times BW}$$

$$C_{PAR} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{SW}}$$

Adjustable Slope Compensation (RAMP)

When the MAX15159 operates at a duty cycle greater than 50%, additional slope compensation is required to ensure stability and prevent subharmonic oscillations that occur naturally in peak-current-mode controlled converters operating in continuous-conduction mode (CCM). The MAX15159 provides RAMP input to select the internal slope compensation ramp within a range of 260mV to 1500mV. It is recommended that discontinuous-conduction mode (DCM) designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

As shown in *Figure 4*, by connecting a resistor (R_{RAMP}) between RAMP and GND, the amplitude of the slope compensation ramp is calculated as follows:

$$V_{SLOPE} = 2 \times V_{RAMP} = 2 \times I_{RAMP} \times R_{RAMP}$$

where:

I_{RAMP} = current sourced from RAMP to GND (10µA, typ)

To guarantee stable and jitter-free operation, it is suggested to select the RAMP resistor such that:

$$R_{RAMP} \geq \frac{5 \times (V_{OUT(MAX)} - V_{IN(MIN)}) \times R_{SENSE}}{I_{RAMP} \times f_{SW} \times L}$$

where:

$V_{OUT(MAX)}$ = maximum output voltage

$V_{IN(MIN)}$ = minimum input voltage

R_{SENSE} = value of the sense resistor

f_{SW} = switching frequency

L = value of the inductor

DRV Supply and Bias Regulator (BIAS)

The controller requires an external 8.5V to 14V DRV supply. The DRV supply powers the internal linear regulator that generates a regulated 5V bias supply to power the internal analog and digital control circuitry as shown in the *Functional Diagrams*. Bypass the BIAS pin with a 2.2µF or greater ceramic capacitor to maintain noise immunity and stability. The BIAS regulator provides up to 35mA of load current.

The controller has a UVLO threshold on DRV. The undervoltage-protection circuits inhibit switching until DRV rises above 8.25V (typ).

If DRV drops below its undervoltage threshold, the controller determines that there is insufficient supply voltage to make valid control decisions. To protect the regulator and the output, the controller immediately pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5.5Ω discharge MOSFET, placing the regulator into a high-impedance output state so the output capacitance passively discharges through the load current.

The BIAS linear regulator powers up as long as DRV exceeds its UVLO threshold.

EN/UVLO and Soft-Start/Shutdown

The EN/UVLO pin allows the input voltage operating range to be externally adjusted for power sequence control. Connect EN/UVLO to the center of a resistor-divider between the input and GND to adjust the UVLO voltage level, as shown in the *Typical Application Circuits*. In the case where the DRV voltage threshold of the external MOSFET driver is higher than the UVLO threshold of the DRV pin, the EN/UVLO pin should also be pulled to GND before the external MOSFET driver is enabled.

At power-up, once the voltage of EN/UVLO is higher than 1V (typ), and the internal reference stabilizes, the controller starts the initialization period where the OVP pin configuration is checked. During this initialization period, the controller pulls SS low through a 5.5Ω discharge MOSFET. As long as initialization is complete and 1.5V < V_{REFIN} < 2.2V or REFIN shorted to BIAS, the controller starts the soft-start sequence by charging the SS capacitor with a constant 10µA current source. COMP voltage increases with a slew rate controlled by the SS voltage. PWM starts when COMP and SS reach 1.5V (typ), ramping the FB up to the preset regulation setpoint.

At power-down, once the voltage of EN/UVLO is below 0.9V (typ) or V_{REFIN} is below 1.4V (typ), the controller immediately pulls PGOOD, CSION, DH_, and DL_ low, and discharges the SS capacitor and COMP rapidly to GND (see *Figure 5*).

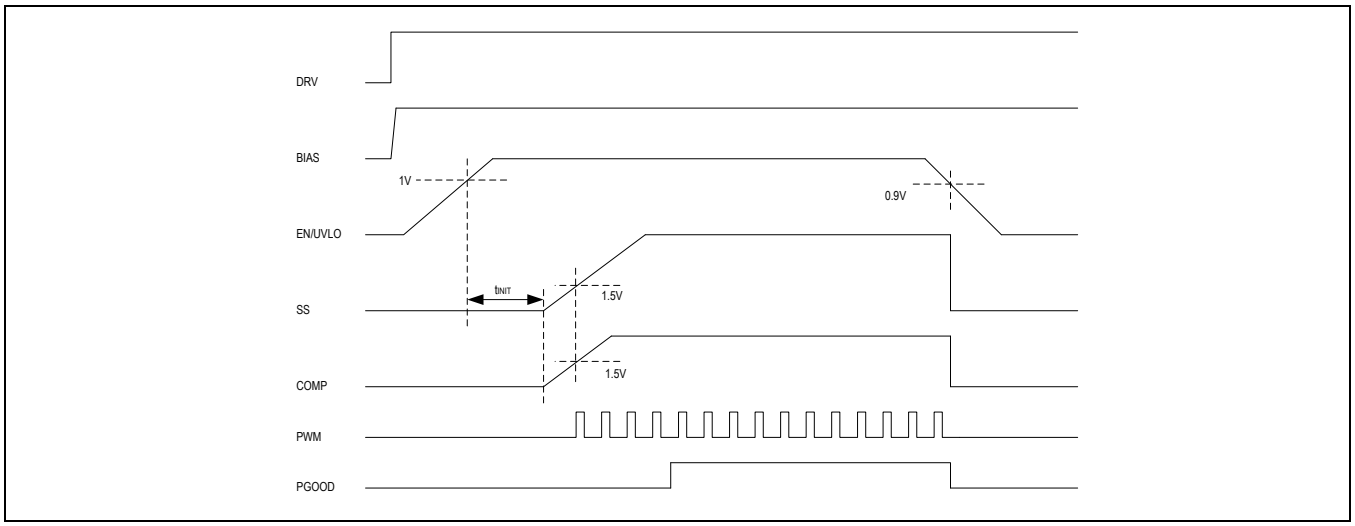


Figure 5. Soft-Start and Shutdown Sequence with EN/UVLO

Overcurrent Protection

A current-sense resistor is connected between the source of the low-side MOSFET and GND. The MAX15159 detects the current-sense signal (CSP_ to CSN_) and compares it with the cycle-by-cycle peak current-limit threshold during low-side on-time. When the current exceeds the cycle-by-cycle peak current-limit threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET until the end of that switching cycle. Each phase has an independent up-down counter to accumulate the number of consecutive peak current-limit events. If the counter exceeds 32, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

There is a secondary fast positive overcurrent protection (FPOCP) threshold, which is 33% higher than the cycle-by-cycle peak current-limit threshold. If the inductor peak current exceeds the FPOCP threshold, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

The cycle-by-cycle peak current-limit threshold is set by the resistor at the ILIM pin. A 10µA source current flows into this resistor and generates a voltage level. This voltage level is internal scaled by a factor of 0.1 to set the cycle-by-cycle peak current-limit threshold. The minimum and maximum settable current-limit levels (V_{OCP}) are 20mV and 100mV. The cycle-by-cycle peak current-limit level is given by the following equation:

$$V_{OCP} = 0.1 \times 10\mu A \times R_{ILIM}$$

The maximum peak inductor current is set by both V_{OCP} and the current-sense resistor (R_{SENSE}):

$$I_{PEAK(MAX)} = V_{OCP}/R_{SENSE}$$

The device also has a negative overcurrent protection (NOCP) threshold, which is -80% of the cycle-by-cycle peak current-limit threshold. When the low-side MOSFET is turned on and the inductor current is below the NOCP threshold, the device commands to keep the low-side MOSFET on to allow the inductor current to be charged by the input voltage until the end of that switching cycle. Each phase has an independent up-down counter to accumulate the number of consecutive NOCP events. If the counter exceeds 32, the device disables the drivers (all driver outputs are pulled low) and discharges the SS capacitor. After 32,768 clock cycles, the device automatically attempts to restart using the soft-start sequence.

Overvoltage Protection

The MAX15159 has an OVP comparator to monitor the FB voltage. The device can be configured to disable OVP or select OVP threshold of 110% by connecting a resistor from the OVP pin to GND.

Once OVP is enabled, the drivers start switching and the V_{REF} is in the range of 1.5V to 2.2V. The FB overvoltage comparator trips if the feedback voltage exceeds the V_{REF} voltage by 110% for more than 128 PWM clock cycles, and then the MAX15159 forces PGOOD, CSION, SS, and COMP pins low and disables the drivers. The controller immediately

restarts once the fault condition has been removed. When OVP is disabled, the PGOOD remains high when the FB voltage is 10% higher than the V_{REF} voltage.

The resistor from the OVP pin to GND is also used to select single-, dual-/quad-, or triple-phase operation. See *Table 1* for details.

Table 1. FB OVP Settings and Phase Configuration

R_{OVP} (1% RESISTOR)	FB OVP THRESHOLD	PHASE CONFIGURATION
GND	110%	Dual-phase or quad-phase operation
51.1kΩ	Disabled	
95.3kΩ	110%	Single-phase operation
140kΩ	Disabled	
182kΩ	110%	Triple-phase operation
226kΩ	Disabled	

Switching Frequency (FREQ/CLK)

The controller supports 120kHz to 1MHz switching frequencies. Leave FREQ/CLK unconnected to select the preset 300kHz switching frequency. To adjust the switching frequency, either place an external resistor from FREQ/CLK to GND or drive FREQ/CLK with an external system clock (see *Table 2*). The resistively programmable switching frequency is determined by the following equation:

$$f_{SW} = \frac{R_{FREQ}}{100k\Omega} \times 600kHz$$

Table 2. Phase and Controller/Target Configuration

NUMBER OF PHASES	NUMBER OF MAX15159 DEVICES	FB OF TARGET IC CONNECTED TO BIAS	CLK FREQUENCY
1	1	N/A	$4 \times f_{SW}$
2	1	N/A	$4 \times f_{SW}$
3	2	Yes	$3 \times f_{SW}$
4	2	Yes	$4 \times f_{SW}$

Phase and Controller/Target Configurations

The MAX15159 can be configured in single-phase, dual-phase, triple-phase, or quad-phase operation modes. When supporting triple-phase or quad-phase operation, two MAX15159 ICs are used as controller and target. The controller identifies the number of phases by the resistor at the OVP pin (selecting the same R_{OVP} required for the controller IC and target IC). This identification is used to determine how the controller responds to the multiphase clock signal generated by the primary phase.

For proper synchronization between two devices, connect the SYNC, COMP, CSIOP, and CSION of the controller and target devices together. Connect the FB and REFIN pins of the target device to its BIAS pin (see *Figure 10*).

In a triple-phase converter, the two phases of the MAX15159 controller interleave by 240°, while the MAX15159 target Phase 1 operates with a 120° phase shift compared to the controller. The second phase of the target remains unused (*Figure 6*).

In a quad-phase converter, the two phases of the MAX15159 controller or target interleave by 180°, while the controller and target operate with 90° phase shift (*Figure 7*).

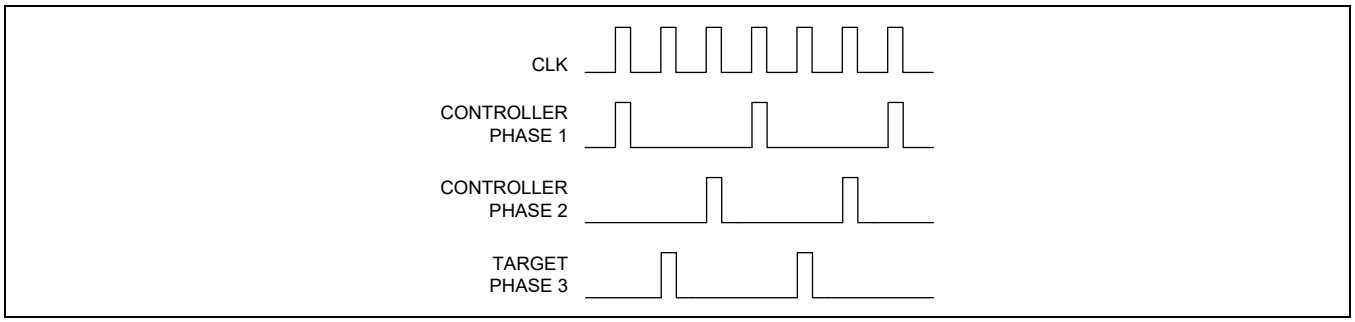


Figure 6. Triple-Phase Synchronization (Controller/Target)

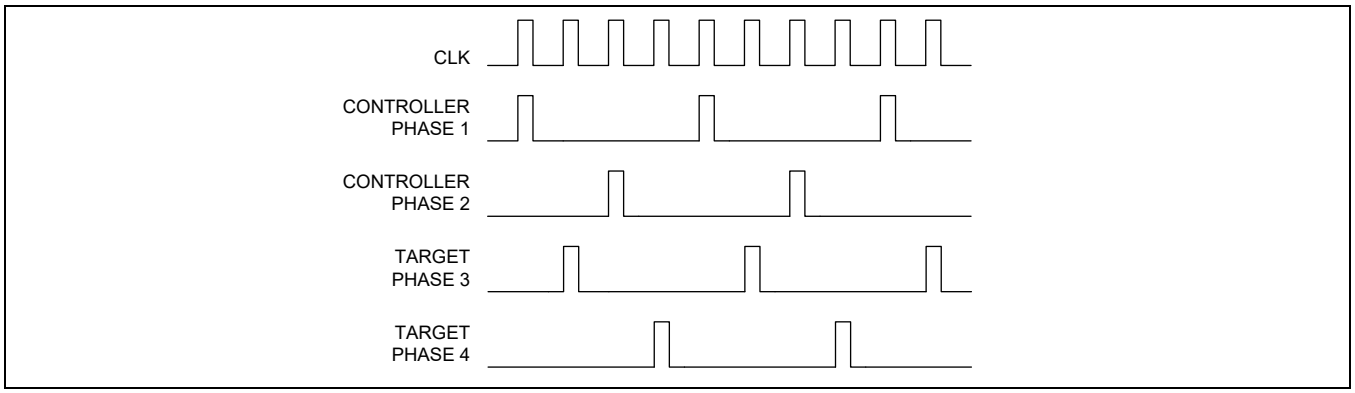


Figure 7. Quad-Phase Synchronization (Controller/Target)

Multiphase Current Balance

The MAX15159 monitors the low-side MOSFET current of each phase for active phase current balancing in multiphase operations. The current imbalance is applied to the cycle-by-cycle current sensing circuitry as feedback, helping regulate so that the load current is evenly shared between the two phases (see the *Functional Diagrams*).

In triple-phase or quad-phase operation, the device uses the differential CSIO_ connections to communicate the average per-chip current between controller and target. The current-mode controller and target devices regulate their current so that all phases share the load current equally.

MOSFET Gate Control

The DL_ outputs of the MAX15159 can directly drive MOSFETs for flyback, non-synchronous boost/inverting buck-boost applications.

For synchronous boost/inverting buck-boost applications, the MAX15159 must be used with external MOSFET drivers to drive power MOSFETs. The device has dedicated DLFB_ pins to detect the gate voltage of the low-side MOSFETs to ensure no shoot-through between the high- and low-side MOSFETs due to the mismatch delays caused by the external MOSFET driver. The DLFB_ pins have a rising threshold of 0.8V (typ) and falling threshold of 0.5V (typ). A resistor-divider can be used from the gate of the low-side MOSFET to the DLFB_ pins to match the MOSFET gate threshold voltage and the DLFB_ threshold (see the *Typical Application Circuits*) to allow robust operation with a wide range of MOSFETs while minimizing dead-time power losses.

Thermal Shutdown

The controller features a thermal fault-protection circuit. When the junction temperature rises above +165°C, the internal thermal sensor triggers the fault protection, disables the drivers, and discharges the SS capacitor. The controller remains disabled until the junction temperature cools by 15°C. Once the device has cooled down, the controller automatically restarts using the soft-start sequence.

Transformer/Inductor Selection

The transformer plays an important role for a flyback converter. Its magnetizing inductance determines the flyback converter works in DCM or CCM. Larger magnetizing inductance results in lower ripple current, leading to reduced core

loss. However, larger magnetizing inductance results in either a larger physical size or a lower saturation current rating. The magnetizing inductance (L_M, open-circuit inductance of primary winding) can be estimated by the following equation:

$$L_M = \frac{\eta \times (D \times V_{IN})^2}{2 \times f_{SW} \times V_{OUT} \times I_{OUT\_BOUNDARY}}$$

where:

η = target efficiency

$I_{OUT\_BOUNDARY}$ = desired output current when the flyback converter works in the boundary mode between DCM and CCM. For DCM operating over input/output range, select $V_{IN} = V_{IN(MIN)}$, $I_{OUT\_BOUNDARY} = I_{OUT(MAX)}$.

Transformer primary-to-secondary turns ratio (N_P/N_S) can be estimated by the following equation:

$$N_P/N_S = \frac{D_{MAX} \times V_{IN(MIN)}}{(1 - D_{MAX}) \times V_{OUT}}$$

where:

D_{MAX} = desired maximum duty cycle in a flyback converter, usually select $D_{MAX} = 0.45$

For boost/inverting buck-boost converter, a larger inductor value results in reduced inductor ripple current leading to a reduced inductor core loss. However, a larger inductor value results in either a larger physical size or a higher series resistance (DCR) and a lower saturation current rating. Typically, the inductor value is chosen to have current ripple (ΔI_L) around 50% of the average inductor current, which can be calculated as follows:

$$I_{L(AVE)} = \frac{I_{OUT(MAX)}}{(1 - D) \times N}$$

where:

N = number of phases

The inductor can be chosen with the following formula:

$$L = \frac{D \times V_{IN}}{f_{SW} \times \Delta I_L}$$

Output Capacitor Selection

The output capacitors are selected to improve stability, output voltage ripple, and load transient performance. To meet output voltage ripple (V_{RIPPLE}) requirement, the output capacitor can be selected by the following equation:

$$C_{OUT(RIPPLE)} = \frac{D \times I_{OUT(MAX)}}{N \times f_{SW} \times V_{RIPPLE}}$$

For some applications, it is desired to limit output voltage overshoot and undershoot during load transient. To meet the load-transient requirement, the output capacitor can be selected by the following equation:

$$C_{OUT(TRANSIENT)} = \frac{\Delta I_{OUT}}{3 \times BW \times \Delta V_{OUT}}$$

where:

ΔI_{OUT} = load current step

BW = control loop bandwidth (see *Compensation Design Guidelines*)

ΔV_{OUT} = desired output voltage overshoot or undershoot

The final output capacitance should be selected as follows:

$C_{OUT} \geq$ maximum ($C_{OUT(RIPPLE)}$, $C_{OUT(TRANSIENT)}$)

Input Capacitor Selection

The input capacitors are selected to help reduce input voltage ripple (V_{IN_RIPPLE}).

For boost converters, the input current is continuous. Neglecting ESR and ESL of the input capacitor, the input capacitor can be selected by the following equation:

$$C_{IN} = \frac{\Delta I_L}{8 \times N \times f_{SW} \times V_{IN\_RIPPLE}}$$

For inverting buck-boost/flyback converters, the input current is discontinuous. The input capacitor can be selected by the following equation:

$$C_{IN} = \frac{D \times I_{OUT(MAX)} \times N_S/N_P}{N \times f_{SW} \times V_{IN\_RIPPLE}}$$

where:

N_S/N_P = transformer secondary-to-primary turns ratio for flyback converter, select N_S/N_P = 1 for inverting buck-boost converter.

PCB Layout Guidelines

The PCB layout can dramatically affect the performance of the power converter. A poorly designed board can degrade efficiency, thermal performance, noise control, and even control-loop stability. At higher switching frequencies, layout issues are especially critical.

As a general guideline, the input capacitors, inductor or transformer, MOSFETs, sense resistor, and output capacitors should be placed close together to minimize the high-frequency current path. The MOSFET driver should be placed close to the MOSFETs and the switching node (SW) to keep the gate drive, BST, and SW traces short. The MAX15159 should keep some distance from the high dv/dt SW, BST, and gate drive traces. The peripheral RC components should be placed as close to the controller as possible. Priority should be given to the pins that are sensitive to noise (COMP, SS, REFIN, FB, etc.). It is suggested to place both differential-mode and common-mode filters between the CSP_ pin, CSN_ pin, and sense resistor (see the *Typical Application Circuits*).

For high-power applications, it is suggested to use planes for the power traces V_{IN}, V_{OUT}, and GND. It is important to have enough vias connecting the power planes in different layers. The signal and power grounds must be separated. All of the power components, including the input and output capacitors, MOSFETs, sense resistor, and MOSFET driver should be connected to the power ground. The MAX15159 and its peripheral RC components must be connected to the signal ground. It is suggested to have an island of signal ground in the closest internal layer underneath the controller. Multiple vias can be used to connect the signal ground island to the exposed pad of the controller and the ground nodes of the noise-sensitive signal (COMP, SS, REFIN, FB, etc.). The signal ground should be tied to the power ground through a short trace or 0Ω resistor close to the power ground node of the sense resistor and input capacitors.

The current sense lines from sense resistor to CSP_ and CSN_ should be routed differentially. When the controller is configured to multiphase operation, the current sense lines of different phases should be kept apart to avoid signal coupling. Keep all sense lines and other noise-sensitive signals (CSIO_, COMP, SS, REFIN, FB, etc.) away from the noisy traces (SW, BST, gate drives, FREQ/CLK, SYNC, etc.).

Typical Application Circuits

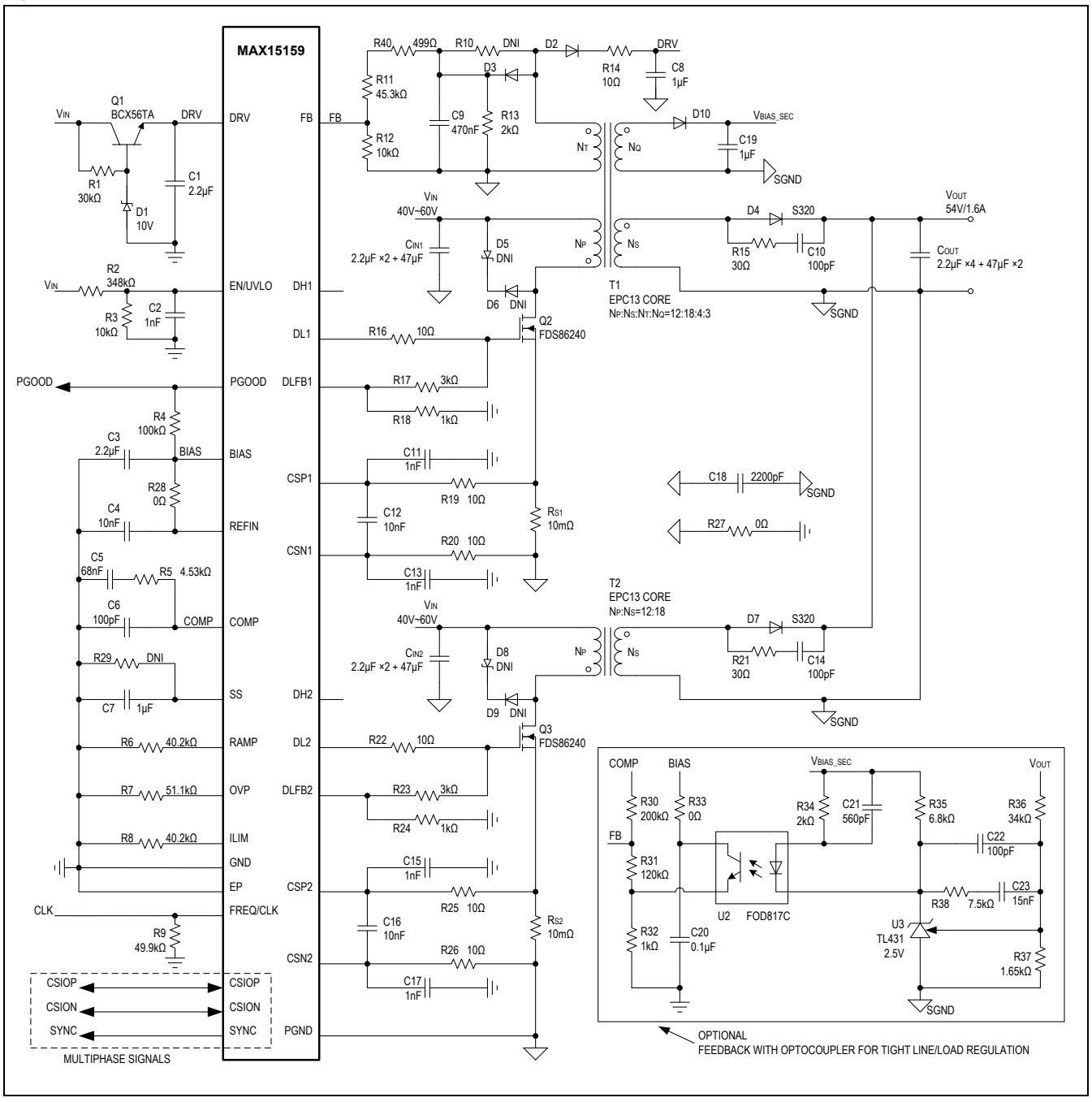


Figure 8. Dual-Phase Flyback Converter

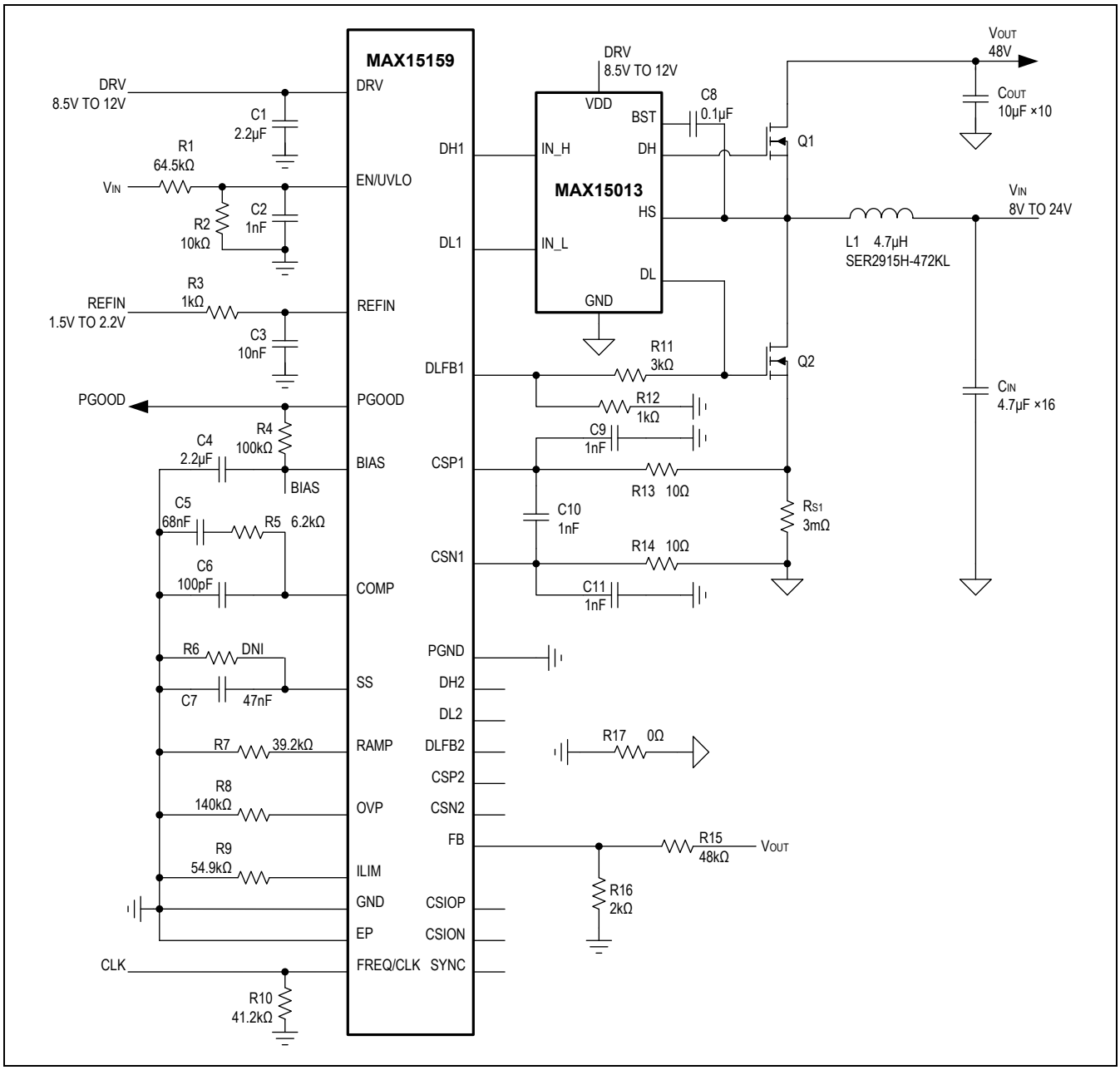


Figure 9. Single-Phase Synchronous Boost Converter

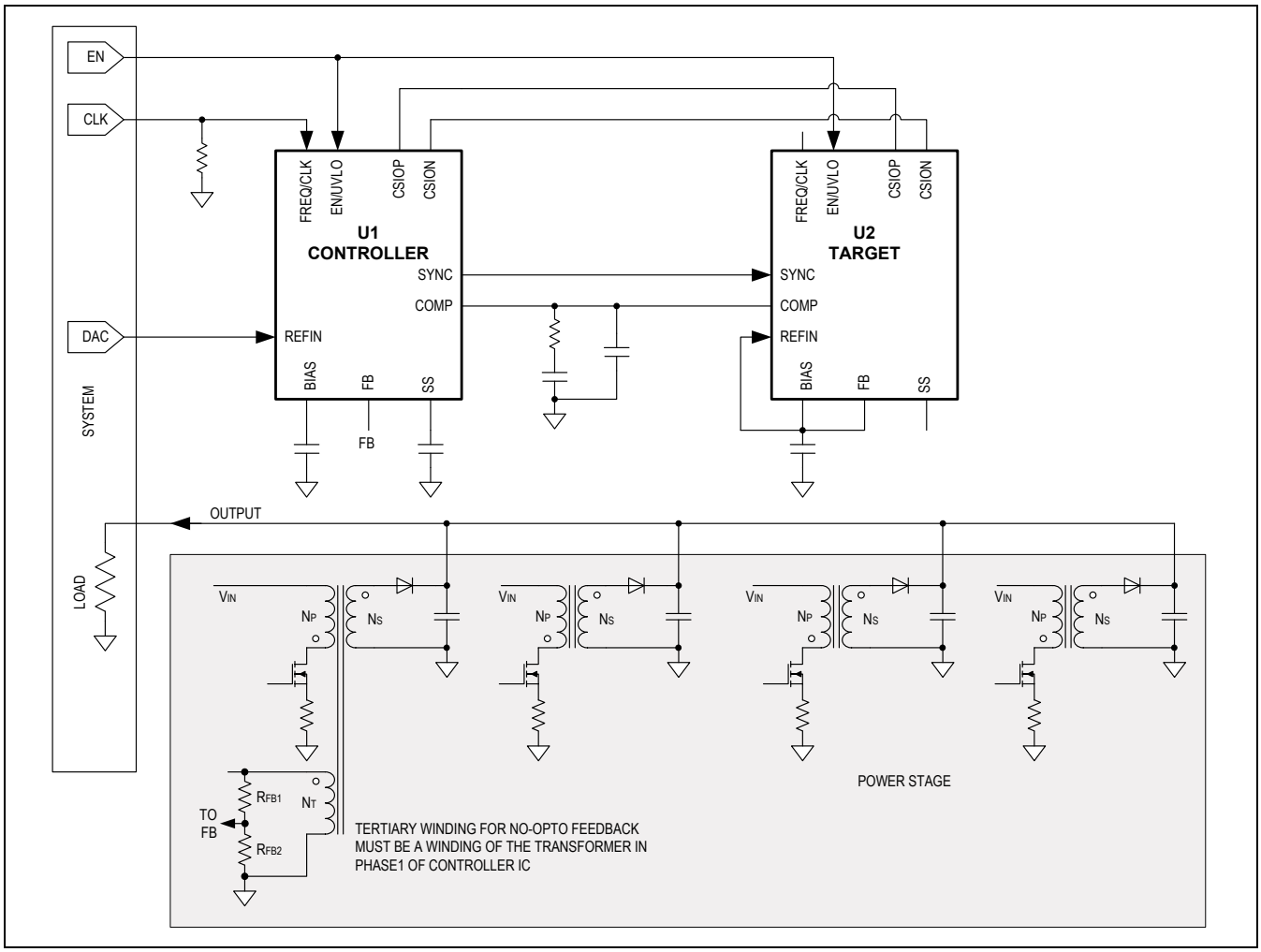


Figure 10. Quad-Phase Interconnects (Flyback Converter)

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX15159ATJ+	-40ºC to +125ºC	32 TQFN-EP*
MAX15159ATJ+T	-40ºC to +125ºC	32 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/23	Release for Market Intro	—