150 A Current Monitor for Intel Psys Applications

FEATURES

- Integrated current sense element
- 150 A current range
- 26,600:1 input-to-output current ratio (5 mA at 133 A)
- ±1.3% TUE maximum (I_{SENSE} = 45 A to 150 A)
- 3.2 MHz small-signal bandwidth (I_{SENSE} = 150 A)
- 150 µΩ current path resistance
- Powered from 2.7 V to 65 V
- Intel Psys compatible
- Available in 108-terminal, 10 mm × 20 mm × 2.75 mm, LGA package

APPLICATIONS

- Computers and network servers
- Intel central processing unit (CPU) motherboards
- Network storage
- Communication equipment
- Electric vehicles
- Photovoltaics

TYPICAL APPLICATION CIRCUIT

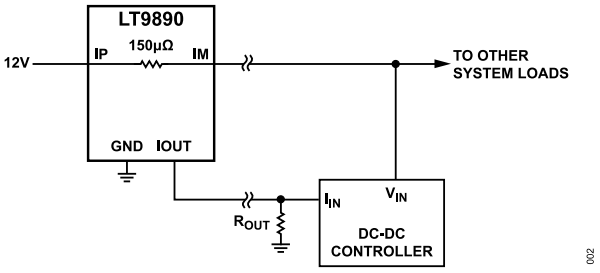

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

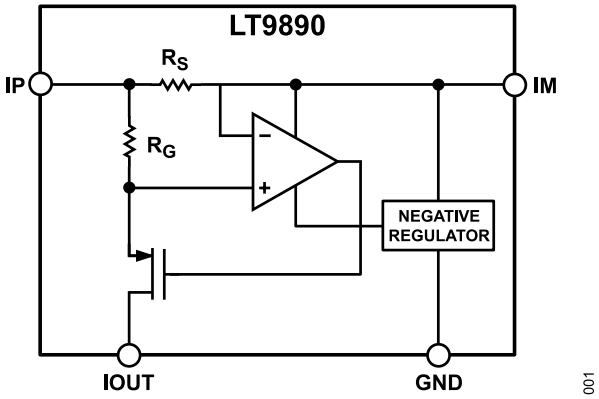

Figure 2. Functional Block Diagram (R_S Is the Sense Resistor, and R_G Is the Gain Resistor.)

GENERAL DESCRIPTION

The LT9890 is a high-precision current monitor with an internal current-sense element supporting up to 150 A of load current. Factory calibration of the current-sense element and a zero temperature coefficient architecture results in less than 1.3% total unadjusted error (TUE). A 26,600:1 input-to-output current ratio with a response bandwidth greater than 3 MHz provides a fast and accurate ground-referenced output signal while being insensitive to ground voltage variations. Minimal power loss is achieved through a low, 150 µΩ current-path resistance and an aspect ratio conducive to wide printed circuit board (PCB) traces. Input voltages from 2.7 V to 65 V are supported. The LT9890 is compatible with the Intel Psys (platform power) applications.

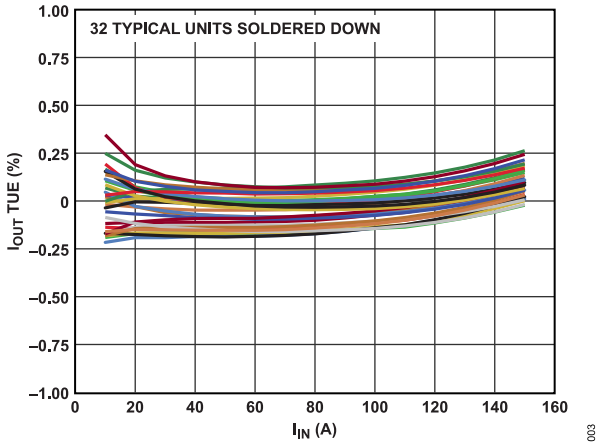

Figure 3. Output Current (I_{OUT}) TUE vs. I_{IN}

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REVISION HISTORY

2/2024—Rev. 0 to Rev. A

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Updated Outline Dimensions..... 11
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7/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

The operating voltage range (V_{IP}) = 12 V, the current from IP to IM (I_{SENSE}) = 100 A, and the output resistor (R_{OUT}) = 200 Ω, unless otherwise noted. All currents into the device pins are positive, and all currents out of the device pins are negative. All voltages are referenced to GND, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY CHARACTERISTICS					
V_{IP}	Voltage on the IP pin with respect to ground	2.7		65	V
Supply Current (I_{IP})	T_J = 25°C, IM floating			2.5	mA
V_{IP} Undervoltage Lockout (V_{UVLO})	V_{IP} ramping up			2.6	V
V_{UVLO} Hysteresis	T_J = 25°C		190		mV
Start-Up Time ($t_{START-UP}$)	T_J = 25°C, time from undervoltage lockout to output current within 1%		200		µs
CURRENT SENSE CHARACTERISTICS (IP AND IM)					
I_{SENSE}		7.5		150	A
Current Path Resistance (R_{PATH})	Resistance from IP to IM[1]		150	325	µΩ
OUTPUT CHARACTERISTICS (IOUT)					
Input-to-Output Current Ratio	T_J = 25°C		26,600		
I_{OUT} TUE	I_{SENSE} = 7.5 A			±4.0	%
	I_{SENSE} = 15 A			±2	%
	I_{SENSE} = 30 A			±1.6	%
	I_{SENSE} = 45 A to 150 A			±1.3	%
Common-Mode Rejection Ratio (CMRR)[2]	T_J = 25°C, DC, V_{IP} = 2.7 V and V_{IP} = 65 V, R_{OUT} = 200 Ω		92		dB
Small-Signal Bandwidth	T_J = 25°C, I_{SENSE} = 7.5 A		0.7		MHz
	T_J = 25°C, I_{SENSE} = 150 A		3.2		MHz
Large-Signal Response Time (t_{RESP})	T_J = 25°C, I_{SENSE} = 7.5 A to 150 A, I_{OUT} settled to within 0.1%		2		µs
Output Integrated Noise Relative to Output Current	T_J = 25°C, I_{SENSE} = 150 A		0.075		%

[1] Use the recommended PCB layout. See the Figure 17 for further details. The current path resistance has a 3900 ppm temperature coefficient.

[2] The CMRR is equal to (R_{OUT} ΔV/IP ΔV)/(Averaged R_{OUT} Voltage/Input Current, I_{IN}, x Shunt Resistance, R_{SHUNT}). R_{OUT} is 200 Ω on the tester.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
IP and IM Voltage Range	−0.3 V to +70 V
IP and IM Current	150 A
IP and IM Transient[1]	250 A
IOUT Voltage Range[2]	−0.3 V to +5 V
IP-to-IOUT Voltage Range[3]	−0.3 V to +70 V
Temperature	
Operating T_J Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum T_J	150°C

1 RMS current must not exceed 150 A in any 1 second period.

2 If IP is greater than 50 V, do not pull IOUT less than −0.3 V.

3 If IP is greater than 50 V and IOUT is pulled to less than −0.3 V, connect a Schottky diode between IOUT and ground. Tie the Schottky cathode to IOUT and the anode to ground.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JCT} and θ_{JCB} are the junction-to-case thermal resistances, top and bottom, respectively.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
CC-108-3	18	9.6	3.4	°C/W

1 Values determined per JEDEC 51-9 and JEDEC 51-12.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

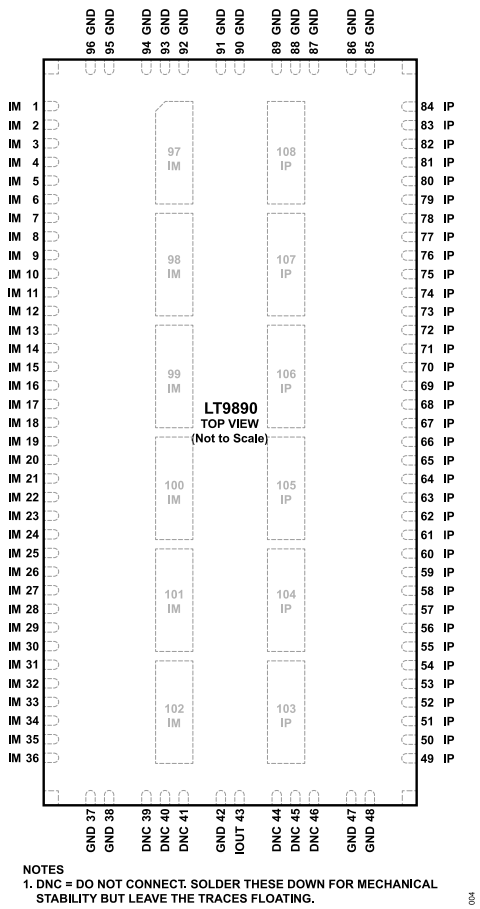


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
Pin 1 to Pin 36 and Pin 97 to Pin 102	IM	Negative Current Input. Tie all 42 IM pins together.
Pin 37 to Pin 38, Pin 42, Pin 47 to Pin 48, and Pin 85 to Pin 96	GND	Ground.
Pin 39 to Pin 41 and Pin 44 to Pin 46	DNC	Do Not Connect. Solder the DNC pins down for mechanical stability but leave the traces floating.
Pin 43	IOUT	Output Current. Proportional to the current flowing from IP to IM.
Pin 49 to Pin 84 and Pin 103 to Pin 108	IP	Positive Current Input. Tie all 42 IP pins together.

TYPICAL PERFORMANCE CHARACTERISTICS

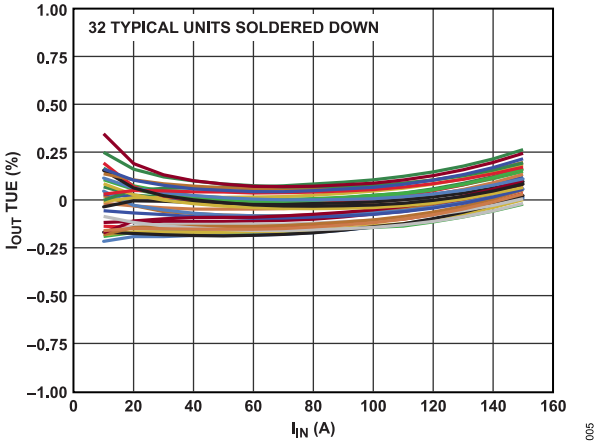


Figure 5. I_{OUT} TUE vs. I_{IN}

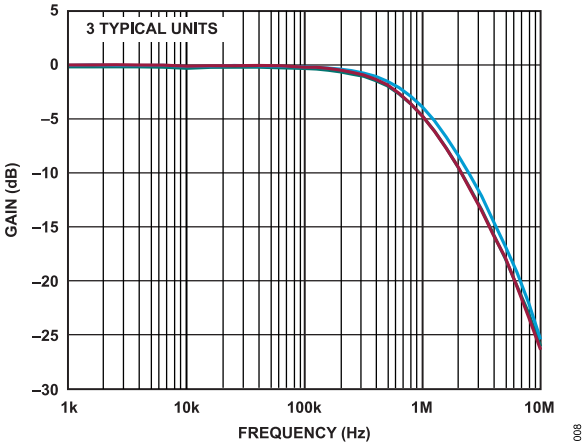


Figure 8. Small-Signal Gain vs. Frequency at 7.5 A

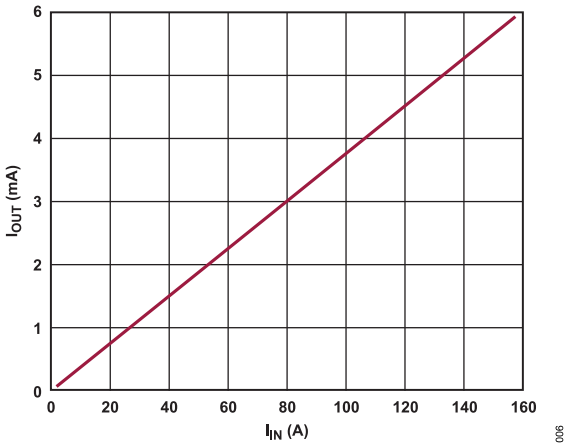


Figure 6. I_{OUT} vs. I_{IN}

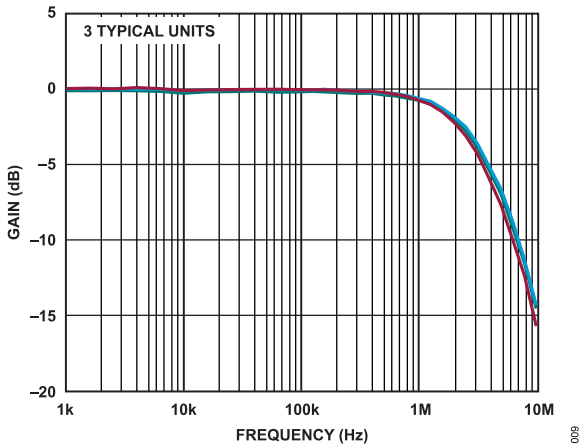


Figure 9. Small-Signal Gain vs. Frequency at 150 A

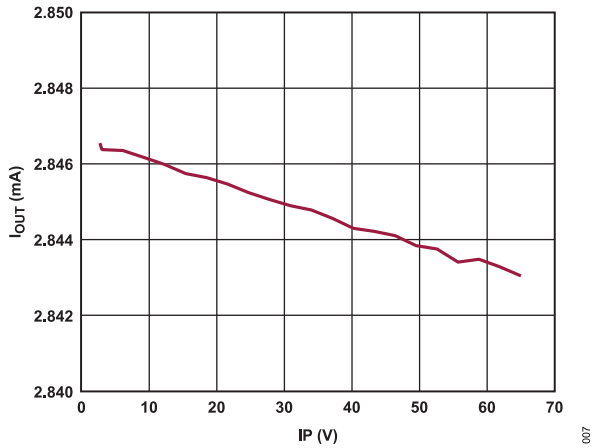


Figure 7. I_{OUT} vs. Input Voltage on IP

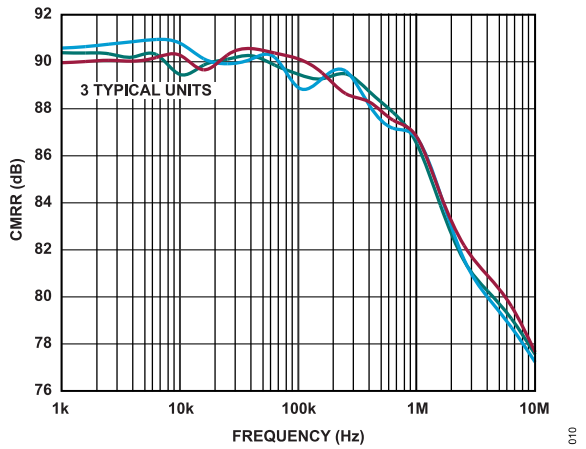


Figure 10. CMRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

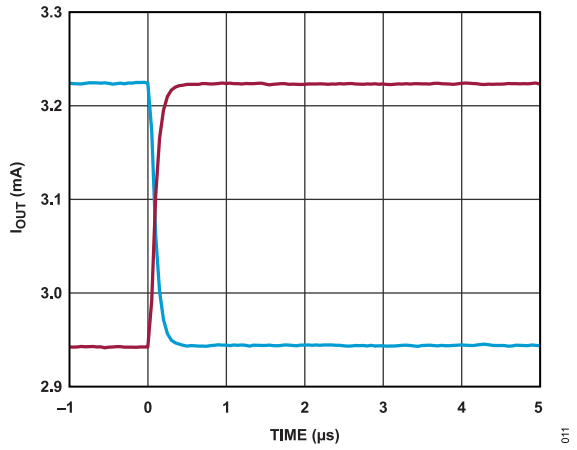


Figure 11. 7.5 A Step Response

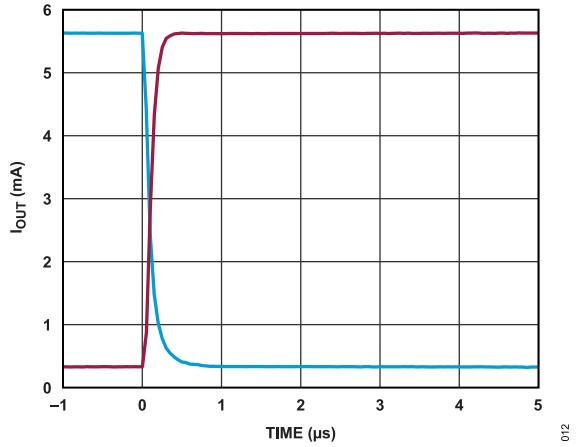


Figure 12. 7.5 A to 150 A Step Response

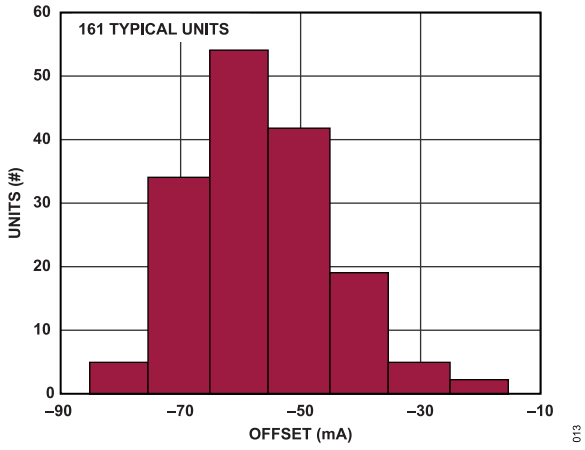


Figure 13. Histogram of Input Referred Offset

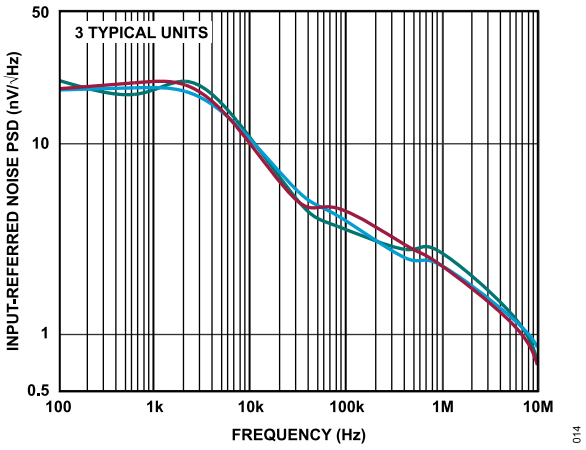


Figure 14. Input-Referred Noise Power Spectral Density (PSD) vs. Frequency at 150 A

THEORY OF OPERATION

Figure 15 shows a typical LT9890 application. An input current up to 150 A flows from the IP pin to the IM pin through an internal copper R_S. The open-loop gain of the amplifier drives the negative terminal voltage to the positive terminal voltage, making the current through the R_G proportional to the input current. This current becomes ground-referenced after flowing through the output p-channel metal-oxide semiconductor (PMOS) device. An internal algorithm with factory trim corrects for the copper-sense element nonidealities. The internal negative regulator forces the same supply voltage across the amplifier through the entire 2.7 V to 65 V voltage range, creating excellent common-mode rejection. All internal circuitry runs off the input rail. The small-supply current relative to the large-signal current has an insignificant effect on the TUE.

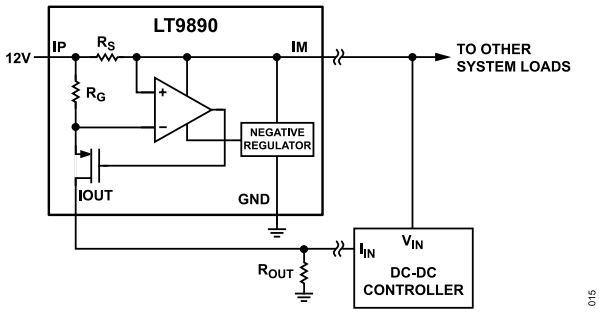


Figure 15. Typical Application

APPLICATIONS INFORMATION

The LT9890 is a high-side current-sense amplifier with an integrated current-sense element. The current-sense element is copper (a proprietary method that corrects for the nonideal resistance traits of the copper). The sense voltage across the sense element is amplified and level shifted to a ground-referred I_{OUT}. The output signal is analog and can be used as is or processed with an output filter.

SELECTION OF R_{OUT}

R_{OUT} determines how I_{OUT} is converted to the IOUT voltage (V_{IOUT}). V_{IOUT} is the output current, I_{IOUT}, × R_{OUT}. In choosing R_{OUT}, the maximum output voltage, $V_{OUT\ (MAX)}$, must first be considered. If the circuit that is driven by the output does not limit V_{OUT}, R_{OUT} must be chosen such that the $V_{OUT\ (MAX)}$ does not exceed the LT9890 I_{OUT} maximum V_{OUT} rating. If the following circuit is a buffer or analog-to-digital converter (ADC) with a limited input range, R_{OUT} must be chosen so that $I_{OUT\ (MAX)}$ × R_{OUT} is less than the allowed maximum input range of this circuit.

In addition, the output impedance is determined by R_{OUT}. If the circuit driven has a high enough input impedance (R_I), most R_{OUT} values are acceptable. However, if the driven circuit has relatively low R_I or draws spikes of current, such as an ADC does, a lower R_{OUT} value is required to preserve the accuracy of the output. For example, if the R_I of the driven circuit is 100 x R_{OUT}, the accuracy of V_{IOUT} is reduced by 1% because of the following:

$$V_{IOUT} = I_{IOUT} \times \frac{R_{OUT} \times R1}{R_{OUT} + R1} \approx 0.99 \times I_{IOUT} \times R_{OUT} \quad (1)$$

OUTPUT FILTERING

The high-frequency performance of the LT9890 is useful for some applications, but other applications require less bandwidth. In these instances, an output capacitor (C_{OUT}) can be placed in parallel with R_{OUT} to reduce noise and to help keep the output steady while driving a switching circuit, such as a multiplexer or ADC. This C_{OUT} in parallel with the R_{OUT} creates a pole in the output response at the following:

$$f_{-3\ dB} = \frac{1}{2 \times \pi \times R_{OUT} \times C_{OUT}} \quad (2)$$

PCB LAYOUT

The high currents through the LT9890 require careful PCB routing. The wide package size was chosen to allow 18 mm wide copper into and out of the device. Use at least 70 µm thick board copper. All current flows through the large IP (Pin 103 to Pin 108) and IM pins (Pin 97 to Pin 102) beneath the package. The many IP pins on the top (Pin 49 to Pin 84) and IM pins on the bottom (Pin 1 to Pin 36) of the PCB carry no current. These pins exist for mechanical stability. Solder these pins to IP and IM as labeled.

A wide copper sense element exists within the package. Current density variations through that shunt can cause errors.

Figure 16 shows three possible routing methods of copper through the LT9890. The left-most method is best because it places the LT9890 directly in the path from the connector to the downstream circuitry. The other two methods create additional TUE. To minimize trace resistance, use multiple wide planes to the LT9890. Reduce the width of these wide planes to 18 mm approximately 4 mm before the large IP and IM pins to force the current to run straight into the LT9890 and avoid crowding. Figure 17 depicts this recommended power layout for one side of the LT9890. Note that the other side mirrors it. The row of vias near the power pads connects the multiple planes right before current enters the LT9890. The vias also operate as thermal vias to dissipate the heat of the LT9890 to all power planes. PCB path resistance often exceeds the 150 µΩ path resistance of the LT9890, which raises the T_J beyond typical calculations. Use short distances, multiple power planes, and thermal vias to reduce self heating. For heat dissipation, the planes on the top and the bottom of the PCB are most important. For minimum PCB resistance, the top planes are most important.

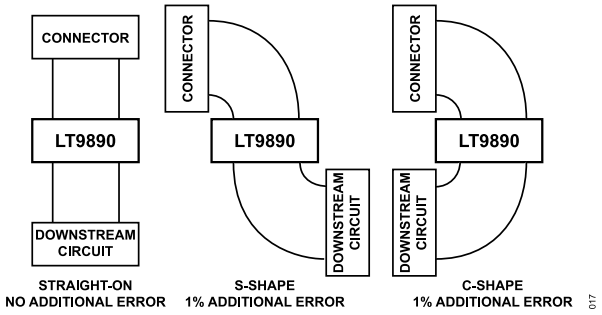


Figure 16. Three Routing Methods of Copper

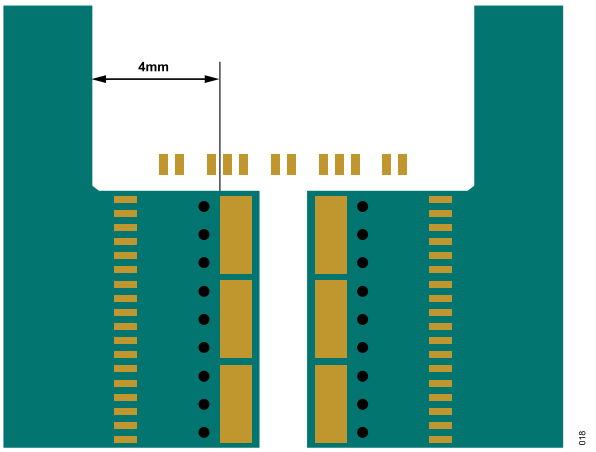


Figure 17. Recommended Power Layout

FACTORY CALIBRATION

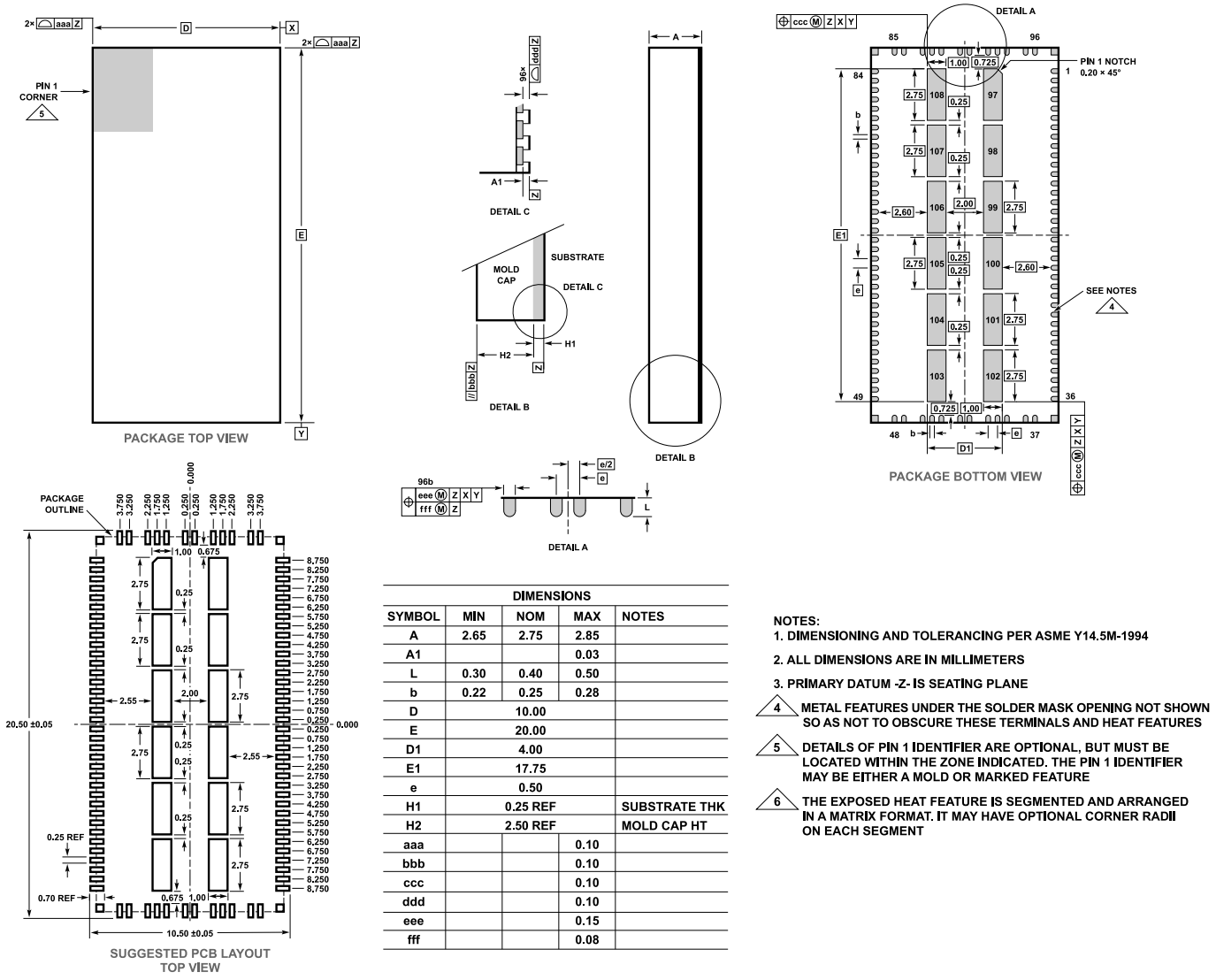
The LT9890 is factory calibrated to correct for the copper sense nonideal resistivity of the element.

RELATED PARTS

Table 5. Related Parts

Part Number	Description	Test Conditions/Comments
LTC2947	30 A power/energy monitor with integrated sense resistor	0 V to 15 V input range, 300 µΩ sense resistor
LTC6102	Precision zero drift current sense amplifier	4 V to 60 V input range, ±10 µV offset

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.65	2.75	2.85	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		10.00		
E		20.00		
D1		4.00		
E1		17.75		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		2.50 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT

Figure 18. 108-Terminal Land Grid Array [LGA]
(10 mm × 20 mm × 2.75 mm)
(Reference DWG# CC-108-3)

Updated: November 17, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
LT9890AV#PBF	-40°C to +125°C	108-Terminal Land Grid Array [LGA] (10 mm x 20 mm x 2.75 mm)	CC-108-3

[1] The LT9890AV#PBF is a RoHS compliant part.

EVALUATION BOARDS

Model[1]	Description
EVAL-LT9890-A1Z	Evaluation Boards

[1] Z = RoHS Compliant Part.