Flip-Chip, Silicon SPDT Switch, 1 GHz to 90 GHz

FEATURES

- Usable frequency range: 1 GHz to 90 GHz
- Low insertion loss
  - 1.2 dB typical to 40 GHz
  - 1.7 dB typical to 67 GHz
  - 3.0 dB typical to 90 GHz
- High Isolation
  - 40 dB typical up to 40 GHz
  - 40 dB typical up to 67 GHz
  - 30 dB typical up to 81 GHz
- High input linearity
  - P0.1dB: 24 dBm typical
  - IP3: 45 dBm typical
- High RF input power handling
  - Through path: 24 dBm
  - Hot switching: 21 dBm
- No low frequency spurs
- CMOS/LVTTL compatible
- Fast RF switching time: 15 ns
- RF settling time (50% V_{CTRL} to 0.1 dB of final RF output): 35 ns
- Single-supply operation capability (VDD = 3.3 V , VSS = 0 V)
- 30-ball, 1.56 mm × 2.04 mm, bumped, bare die sales

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

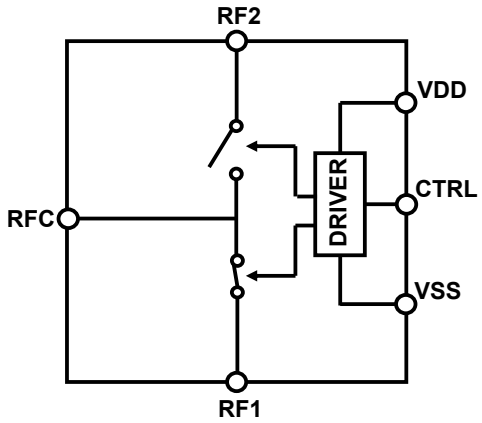

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5420 is a reflective, single-pole double-throw (SPDT) switch manufactured in the silicon process. This switch operates from 1 GHz to 90 GHz with better than 3.0 dB of insertion loss and 30 dB of isolation. The ADRF5420 has an RF input power handling capability of 24 dBm for the through path and 21 dBm for hot switching.

The ADRF5420 draws a low current of 130 µA on the positive supply of +3.3 V and 490 µA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5420 can also operate with a single positive supply voltage (VDD) applied while the negative supply voltage (VSS) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See Table 2 for more details.

The ADRF5420 RF ports are designed to match a characteristic impedance of 50 Ω. The ADRF5420 is a 30-ball, 1.56 mm x 2.04 mm, bumped bare die sales and can operate between −40°C to +105°C.

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, control voltage (V_{CTRL}) = 0 V or VDD, and case temperature (T_{CASE}) = 25°C for 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		90	GHz
INSERTION LOSS						
Between RFC and RF1/RF2 (On)						
		100 MHz to 18 GHz		0.9		dB
		18 GHz to 40 GHz		1.2		dB
		40 GHz to 55 GHz		1.5		dB
		55 GHz to 67 GHz		1.7		dB
		67 GHz to 90 GHz		3.0		dB
RETURN LOSS						
RFC and RF1/RF2 (On)						
		100 MHz to 18 GHz		18		dB
		18 GHz to 40 GHz		16		dB
		40 GHz to 55 GHz		15		dB
		55 GHz to 70 GHz		15		dB
		67 GHz to 90 GHz		10		dB
ISOLATION						
Between RFC and RF1/RF2		100 MHz to 18 GHz		47		dB
		18 GHz to 40 GHz		40		dB
		40 GHz to 55 GHz		40		dB
		55 GHz to 67 GHz		40		dB
		67 GHz to 90 GHz		30		dB
Between RF1 and RF2		100 MHz to 18 GHz		49		dB
		18 GHz to 40 GHz		42		dB
		40 GHz to 55 GHz		43		dB
		55 GHz to 67 GHz		40		dB
		67 GHz to 90 GHz		30		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		5		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		15		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF output		35		ns
INPUT LINEARITY[1]		1 GHz to 67 GHz				
0.1 dB Power Compression	P0.1dB			24		dBm
Third-Order Intercept	IP3	Two tone input power = 14 dBm each tone, Δf = 1 MHz		45		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			130		µA
Negative Supply Current	I_{SS}			490		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2]	P_{IN}	f = 3 GHz to 70 GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through connected RF1 and RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			21	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 13 to Figure 16.

[2] For power derating over frequency, see Figure 2 and Figure 3.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

VDD = 3.3 V, VSS = 0 V, V1 = 0 V or VDD, V2 = 0 V or VDD, and T_{CASE} = 25°C for 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		90	GHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		20		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		38		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		42		ns
INPUT LINEARITY		f = 1 GHz to 67 GHz				
0.1 dB Power Compression	P0.1dB			14		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, Δf = 1 MHz		41		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1]	P_{IN}	f = 3 GHz to 70 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1/RF2			14	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1/RF2			11	dBm

[1] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 1 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input[1]	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[2] (V_{DD} = +3.3 V, V_{SS} = −3.3 V, f = 3 GHz to 70 GHz, T_{CASE} = 85°C[3])	
Through Path	25 dBm
Hot Switching	22 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 3 GHz to 70 GHz, T_{CASE} = 85°C[3])	
Through Path	15 dBm
Hot Switching (RFC)	12 dBm
RF Input Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	15 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for dual supply and 1 dB for single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CD-30-3, Through Path	537	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

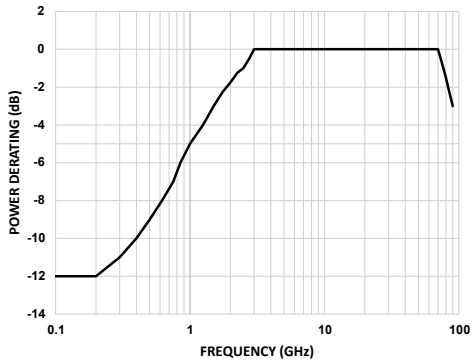

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

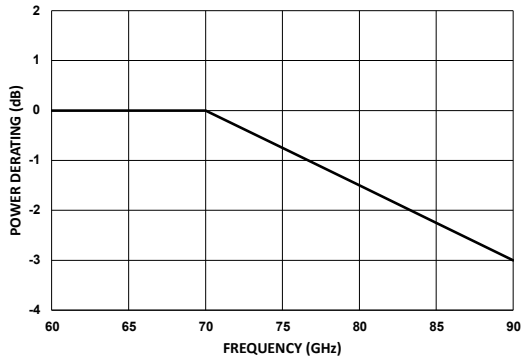

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5420

Table 5. ADRF5420, 30-Ball Bumped Bare Die Sales

ESD Model	Withstand Threshold (V)
HBM	±500 for RF Pins ±2000 for Supply and Digital Control Pins

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

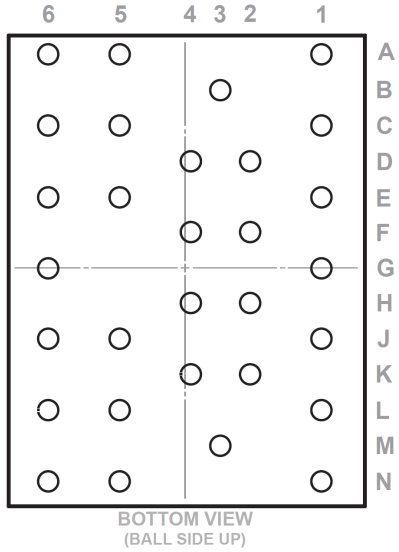

Figure 4. Pin Configuration (Bottom View—Ball Side Up)

Table 6. Pin Function Descriptions

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
A1	GND	−0.575	+0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
A5	GND	+0.275	+0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
A6	GND	+0.575	+0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B3	RF2	−0.15	+0.75	RF Port 2. The RF2 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
C1	GND	−0.575	+0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C5	GND	+0.275	+0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C6	GND	+0.575	+0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
D2	GND	−0.275	+0.45	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
D4	GND	−0.025	+0.45	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
E1	GND	−0.575	+0.3	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
E5	GND	+0.275	+0.3	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
E6	VSS	+0.575	+0.3	Negative Supply Voltage. See Figure 7 for the interface schematic.
F2	GND	−0.275	+0.15	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
F4	GND	−0.025	+0.15	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G1	RFC	−0.575	0	RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
G6	CTRL	+0.575	0	Control Input Voltage. See for the Figure 6 interface schematic.
H2	GND	−0.275	−0.15	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
H4	GND	−0.025	−0.15	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J1	GND	−0.575	−0.3	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J5	GND	+0.275	−0.3	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J6	VDD	+0.575	−0.3	Positive Supply Voltage. See Figure 7 for the interface schematic.
K2	GND	−0.275	−0.45	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
K4	GND	−0.025	−0.45	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L1	GND	−0.575	−0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L5	GND	+0.275	−0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L6	GND	+0.575	−0.6	Ground. The GND pin must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
M3	RF1	−0.15	−0.75	RF Port 1. The RF1 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
N1	GND	−0.575	−0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N5	GND	+0.275	−0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N6	GND	+0.575	−0.9	Ground. The GND pin must be connected to the RF and DC ground of the PCB.

INTERFACE SCHEMATICS

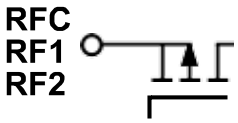

Figure 5. RFx Pins Interface Schematic

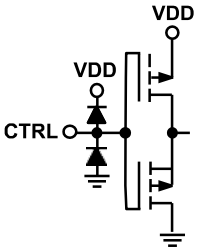

Figure 6. CTRL Interface Schematic

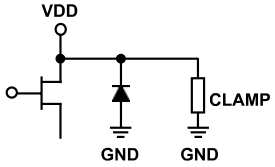

Figure 7. VDD Pin Interface Schematic

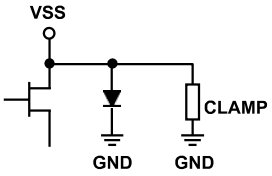

Figure 8. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL} = 0 V or VDD, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. Insertion loss, return loss and isolation are measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RFx pins.

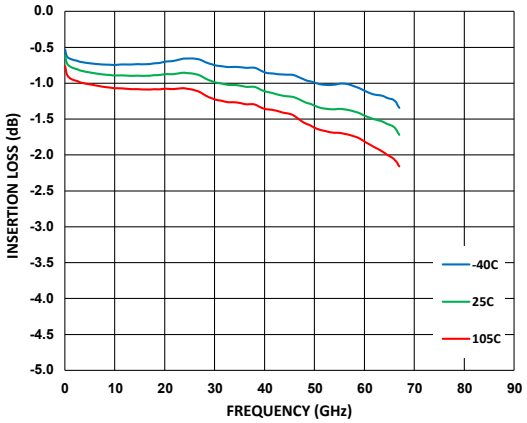

Figure 9. Insertion Loss vs. Frequency over Temperature (Setup limitation 67 GHz)

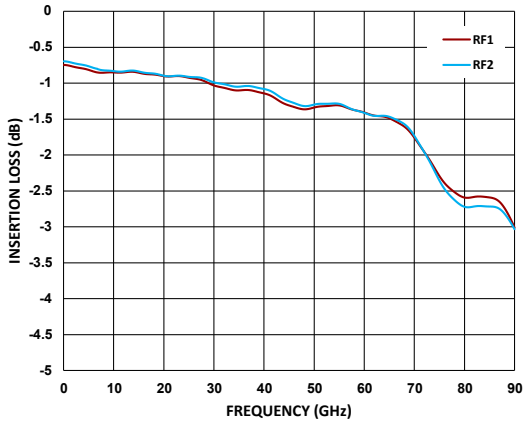

Figure 11. Insertion Loss vs. Frequency

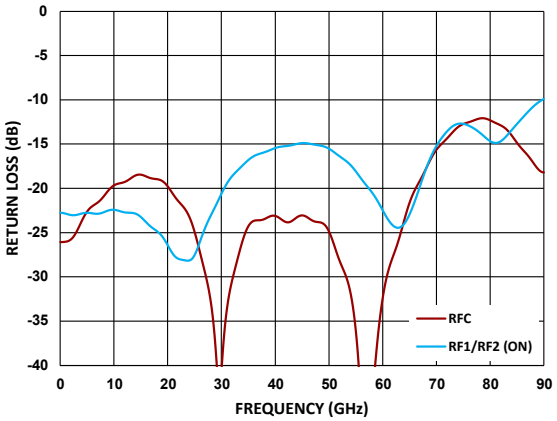

Figure 10. Return Loss vs. Frequency

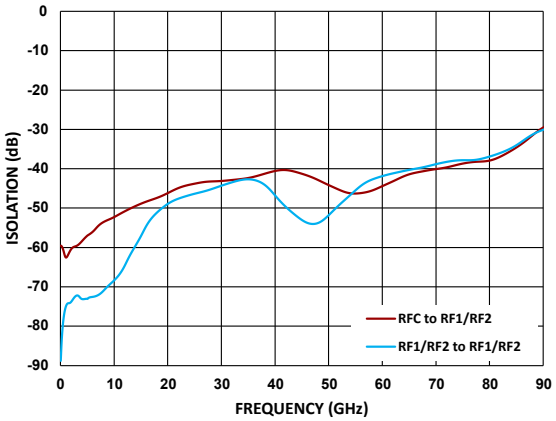

Figure 12. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, V_{CTRL} = 0 V or VDD, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. All of the large signal performance parameters were measured on the evaluation board.

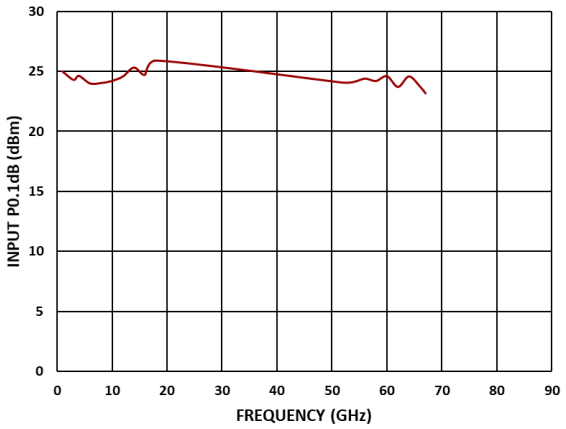

Figure 13. Input P0.1dB vs. Frequency

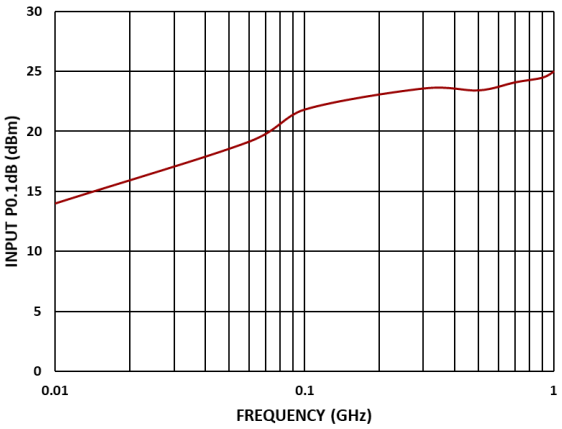

Figure 15. Input P0.1dB vs. Frequency (Low Frequency Detail)

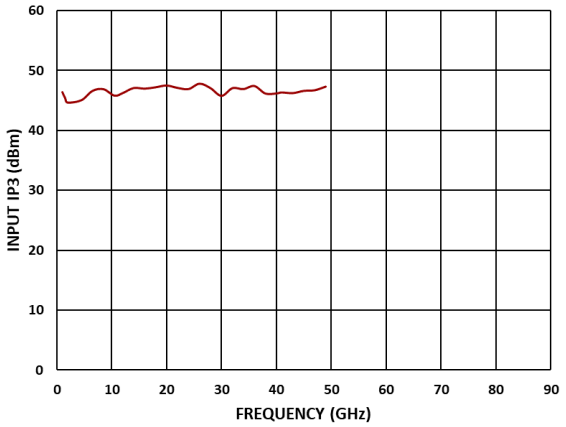

Figure 14. Input IP3 vs. Frequency

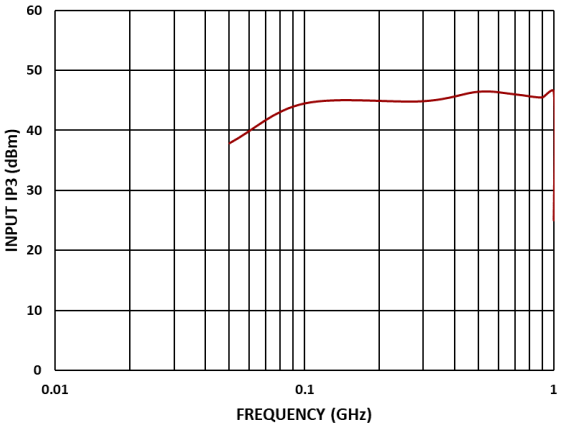

Figure 16. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5420 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

All of the RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5420 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. This driver features a single digital control input pin, CTRL. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state and in the isolation state (see Table 7).

The unselected RF port of the ADRF5420 is reflective. The isolation path provides high isolation between the unselected port and the insertion loss path.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply digital control input. Powering the digital control input before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pin is not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 7. Control Voltage Truth Table

	RF Path	
Digital Control Input (V_{CTRL})	**RF1 to RFC**	**RF2 to RFC**
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

APPLICATIONS INFORMATION

The ADRF5420 has two power supply pins (VDD and VSS) and one control pin (CTRL). Figure 17 shows the external components and connections for the supply pin. The VDD, VSS, and CTRL pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to the Pin Configuration and Function Descriptions section for further details.

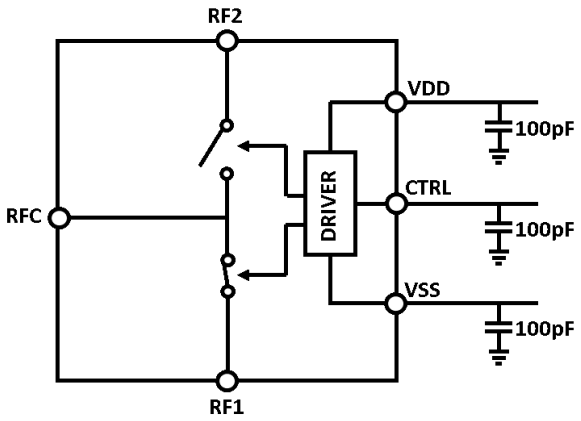

Figure 17. Recommended Schematic

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB.Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 6 mil thick Megtron6 2×1080 R-5775G dielectric material. The RF trace with 300 µm width and 300 µm clearance is recommended for 42 µm finished copper thickness.

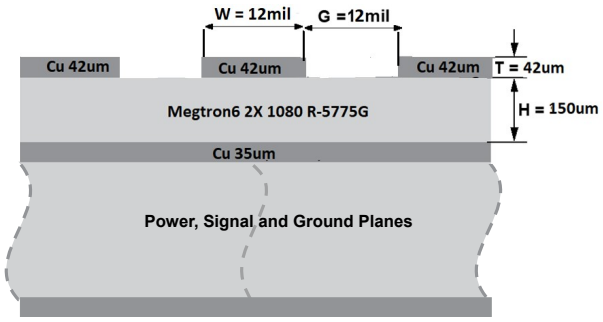

Figure 18. Probe Matrix Board Stackup

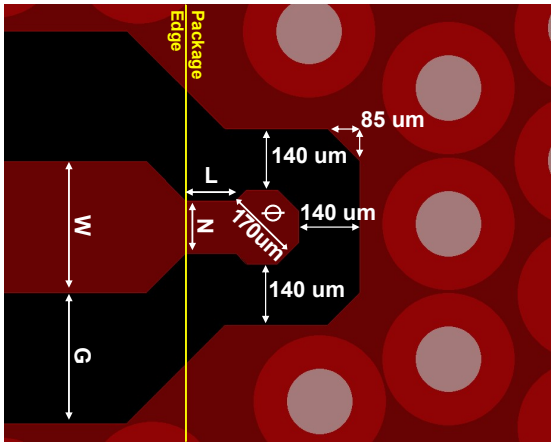

Figure 19. Recommended RF Pin Transition

Figure 19 shows the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. Signal pads have a 170 µm diameter for ease of assembly. The RF trace from the PCB pad is extended with a thinner neck for broadband tuning and tapered to RF trace with a 45° angle. The RFx pin transition for of the ADRF5420 is optimized for the different stackups in Table 8 for broadband performance. For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

Table 8. Recommended RFx Pin Transitions for Different Stackups

RF Stackup Height and Dielectric		RF Trace Dimensions		ADRF5420	Transition Dimensions	
H (µm)	Er	W (µm)	G (µm)	Mnemonics	N (µm)	L (µm)
85	3.02	180	250	RFC	100	190
				RF1, RF2	100	215
100	3.34	200	225	RFC	120	190
				RF1, RF2	120	165
115	3.40	225	250	RFC	120	140
				RF1, RF2	120	165
125	3.00	250	225	RFC	120	90
				RF1, RF2	120	165
150[1].	3.40	300	300	RFC	120	90
				RF1, RF2	120	165
175	3.16	360	245	RFC	120	90
				RF1, RF2	120	165
190	3.00	425	225	RFC	170	90
				RF1, RF2	170	165
200	3.55	425	275	RFC	170	90
				RF1, RF2	170	165

[1] Design reference and generic footprint

APPLICATIONS INFORMATION

DIE ASSEMBLY

The ADRF5420 complies with standard RoHS reflow assembly process and its temperature profiles. The ADRF5420 can be assembled with other surface-mounted technology (SMT) components in the same reflow cycle. However, the PCB must be designed according to the pick and place process.

The top copper layer of the PCB is designed for optimum RF performance where the solder mask and paste mask layers are designed for optimum assembly yield. The ground pads are drawn as solder mask defined. The signal pads are drawn as pad defined. The same solder mask and paste mask design can be used for both pads.

The ADRF5420 can also be assembled without applying a solder paste on the PCB. If no solder paste is applied, the device must be dipped into flux prior to placement on the PCB.

Reflow Assembly with Solder Paste

Solder mask openings of 175 µm in a square shape is recommended for signal and RF pads and 150 µm in a square shape is recommended for GND pads. Solder mask thickness must not exceed 50 µm. Paste mask is drawn circular with a 150 µm diameter. Using a stencil with 2 mil thickness and no aperture reduction yields the optimum paste mask print. In this assembly, the device does not need any flux dipping during the pick and place process.

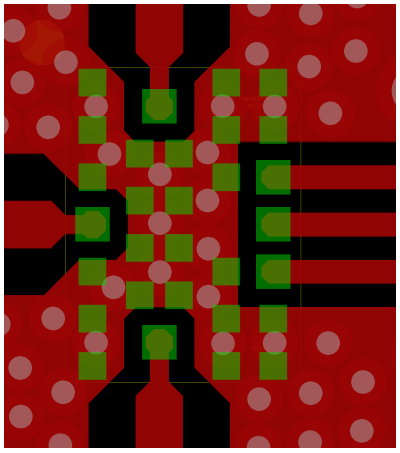

Figure 20. Recommended footprint for Solder Paste

Reflow Assembly with Flux Dipping

Solder mask openings that are circular and 130 µm in diameter are recommended. Solder mask thickness must not exceed 50 µm. Solder paste is not applied. The device is dipped into flux prior to placement on the board.

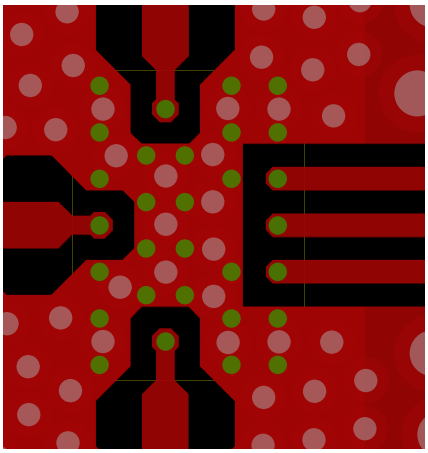

Figure 21. Recommended Footprint for Flux Dip Assembly

OUTLINE DIMENSIONS

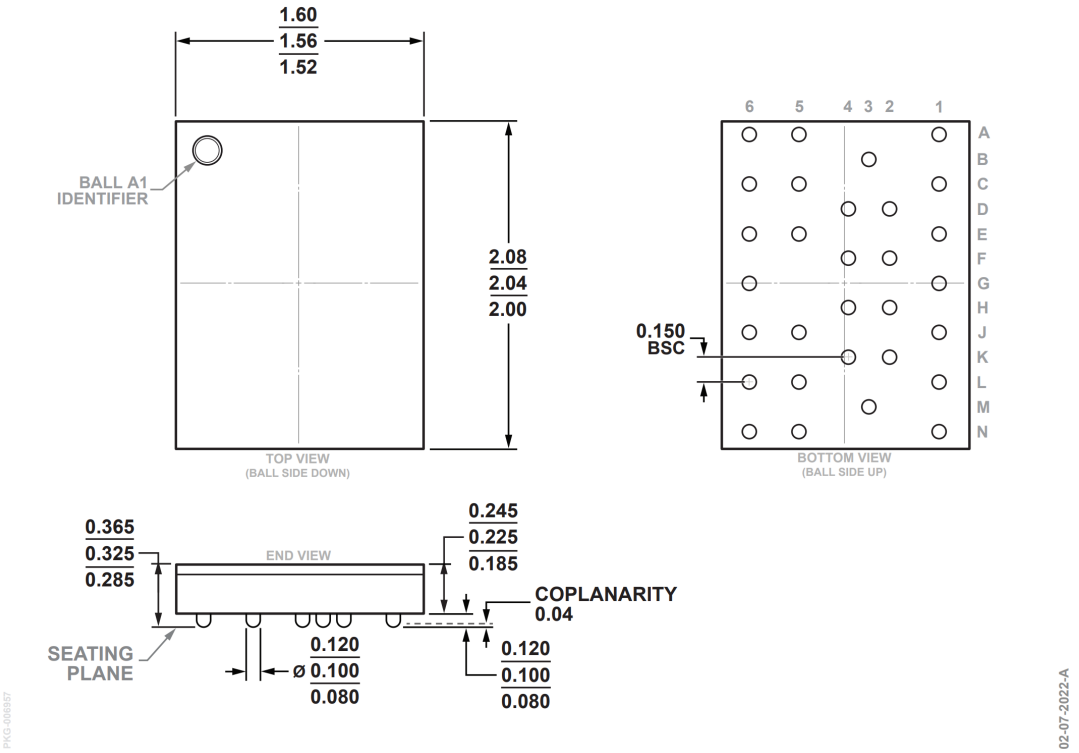

Figure 22. 30-Ball Bumped Bare Die Sales [BUMPED_CHIP]
(CD-30-3)
Dimensions shown in millimeters