Preliminary Data Sheet

ADRF5030

100 MHz to 20 GHz, Non-Reflective, Silicon SPDT Switch

FEATURES

- Ultra-wideband frequency range, 100 MHz to 20 GHz
- Non-reflective design
- Low insertion loss
  - 0.7 dB typical between 0.1 GHz to 6 GHz
  - 0.9 dB typical between 6 GHz to 12 GHz
  - 1.2 dB typical up to 20 GHz
- High isolation
  - 45 dB typical up to 20 GHz for RFC-RF1/2
  - 45 dB typical up to 20 GHz for RF1-RF2
- High input linearity
  - P0.1dB: >36 dBm typical
  - IP3: 60 dBm typical
- High RF power handling
  - Through path: 36 dBm peak / 33 dBm avg
  - Terminated Path: 36 dBm peak / 33 dBm avg
  - Hot switching path: 36 dBm peak /33 dBm avg
- CMOS/LVTTL compatible
- No low-frequency spur; No negative voltage generator
- Fast RF switching time: 60 ns
- RF settling time (50% V_{CTRL} to 0.1 dB of RF output): 90 ns
- Single-supply operation capability (V_{DD} = 3.3 V, V_{SS} = 0 V)
- 20-terminal, 3 mm x 3 mm LGA package
- Pin Compatible with ADRF5022 & ADRF5026

APPLICATIONS

- Test instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

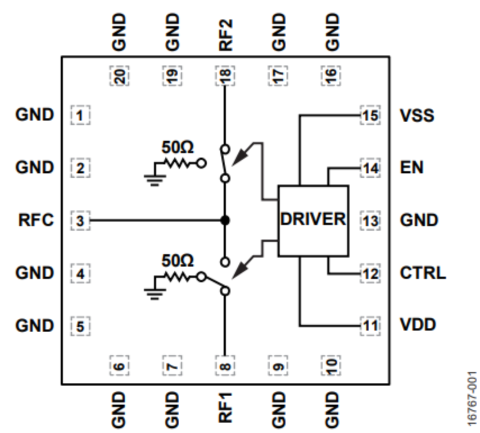


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5030 is a non-reflective, single-pole double-throw (SPDT) switch manufactured using the silicon on insulator (SOI) process. The ADRF5030 operates from 100 MHz to 20 GHz with insertion loss of lower than 1.2 dB and isolation of higher than 45 dB. The device has an RF input power handling capability of 33 dBm average / 36 dBm peak for both through paths, termination and hot switching operation. The ADRF5030 operates with dual-supply voltages of ±3.3 V. The ADRF5030 employs CMOS and low-voltage transistor to transistor logic (LVTTL)-compatible control.

The ADRF5030 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated. See Table 2 for more details.

The ADRF5030 is pin compatible with the ADRF5022 and ADRF5026.

The ADRF5030 is packaged in a 20-terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA). The ADRF5030 operates from −40°C to +105°C.

TABLE OF CONTENTS

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. RFx refers to RF1 or RF2.

Table 1. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1 GHz to 6 GHz		0.7		dB
		6 GHz to 12 GHz		0.9		dB
		12 GHz to 20 GHz		1.2		dB
RETURN LOSS						
RFC		0.1 GHz to 20 GHz		21		dB
RFx (On)		0.1 GHz to 20 GHz		19		dB
RFx (Off)		0.1 GHz to 20 GHz		17		dB
ISOLATION						
Between RFC and RFx		0.1 GHz to 20 GHz		45		dB
Between RFx and RFx		0.1 GHz to 20 GHz		45		dB
SWITCHING						
Rise and Fall Time	t_{RISE},t_{FALL}	10% to 90% of RF output		13		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		60		ns
Settling Time						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		90		ns
INPUT LINEARITY[1]		f = 0.1 GHz to 20 GHz				
Input Compression	P0.1dB			36		dBm
Third-Order Intercept	IP3	Two-tone input power = 14 dBm each tone, Δf = 1 MHz		60		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			150		μA
Negative Supply Current	I_{SS}			520		μA
DIGITAL CONTROL INPUTS		CTRL, EN pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		μA
High	I_{INH}			33		μA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Inputs Voltage	V_{CTL}		0		V_{DD}	V
RF Input Power[2, 3]	P_{IN}	f = 0.1 GHz to 20 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or RF1/RF2				
Average					33	dBm
Peak					36	dBm
Terminated Path		RF signal is applied to RF1/RF2 and terminated within internal resistor				
Average					33	dBm
Peak					36	dBm
Hot Switching		RF signal is applied to RFC or RF1/RF2				
Average					33	dBm
Peak					36	dBm
Case Temperature	T_{CASE}		−40		+105	°C

SPECIFICATIONS

[1] For input linearity performance over frequency, see Figure 12 to Figure 15.

[2] For power derating over frequency, see the Power Derating Curves section.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C for 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operational Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		TBD		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		TBD		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		TBD		ns
INPUT LINEARITY		f = 1 GHz to 60 GHz				
0.1 dB Power Compression	P0.1dB			22		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, Δf = 1 MHz		TBD		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1]	P_{IN}	f = 1 GHz to 20 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1/RF2			TBD	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1/RF2			TBD	dBm

[1] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input[1]	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[2] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 0.1 GHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	
Average	34 dBm
Peak	37 dBm
Terminated Path	
Average	33.5 dBm
Peak	36.5 dBm
Hot Switching (RFC)	
Average	34 dBm
Peak	37 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 0.1 GHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	TBD dBm
Terminated Path	TBD dBm
Hot Switching (RFC)	TBD dBm
RF Input Power, Unbiased (V_{DD}, V_{SS} = 0 V)	TBD dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for dual supply and 3 dB for single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction-to-case bottom (channel-to-package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-20-21, Through Path	93.3	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

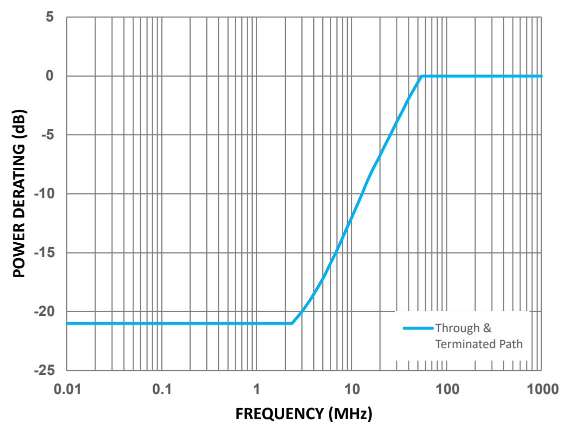


Figure 2. Power Derating vs. Frequency, Low-Frequency Detail, T_{CASE} = 85°

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5030

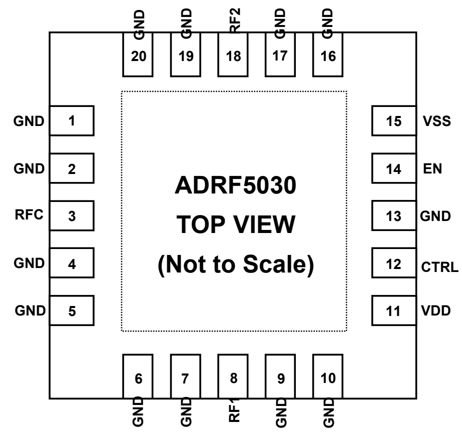
Table 5. ADRF5030, 20-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1.5 kV for RF pins	1B
	2 kV for supply and digital control pins	1B
CDM	500 V for all pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



► NOTES

► 1. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND OF THE PCB.

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 6, 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. These pins must be connected to the RF/DC ground of the PCB.
3	RFC	RF Common Port. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
8	RF1	RF Port 1. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
11	VDD	Positive Supply Voltage. See Figure 6 for the interface schematic.
12	CTRL	Control Input Voltage. See Figure 5 for the interface schematic.
14	EN	Enable Input Voltage. See for the truth table. See Figure 5 for the interface schematic.
15	VSS	Negative Supply Voltage. See Figure 7 for the interface schematic.
18	RF2	RF Port 2. This pin is DC-coupled to 0 V. No DC-blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

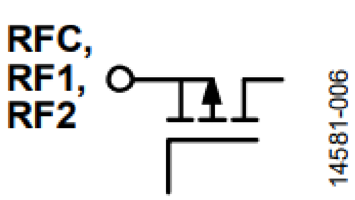


Figure 4. RFC, RF1, RF2 Pins Interface Schematic

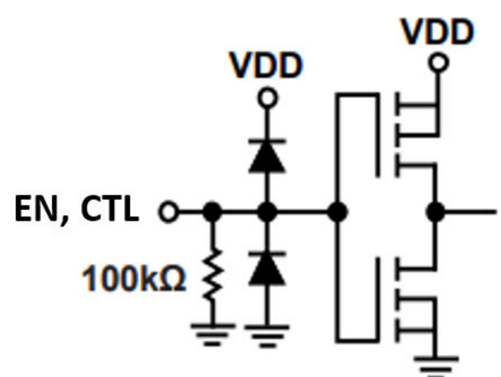


Figure 5. EN, CTL Pin Interface Schematic

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

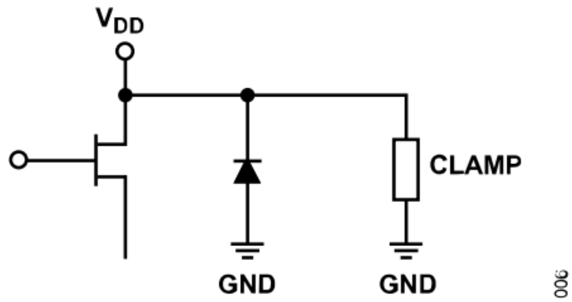


Figure 6. V_{DD} Interface Schematic

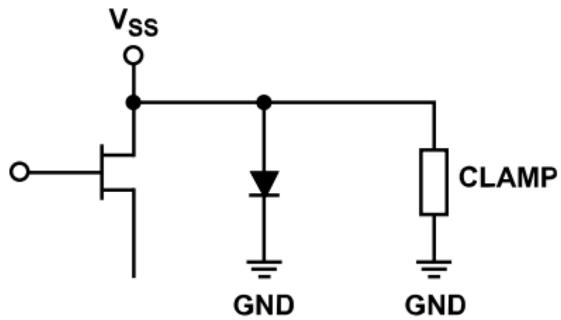


Figure 7. V_{SS} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = –3.3 V, V_{CTRL} = 0 V or V_{DD}, and T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. RFx refers to RF1 or RF2.

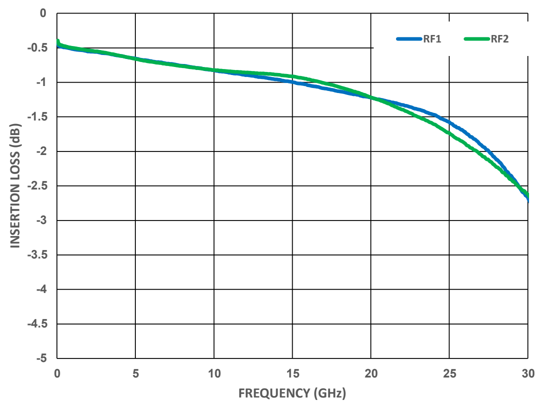


Figure 8. Insertion Loss vs. Frequency RF1 and RF2

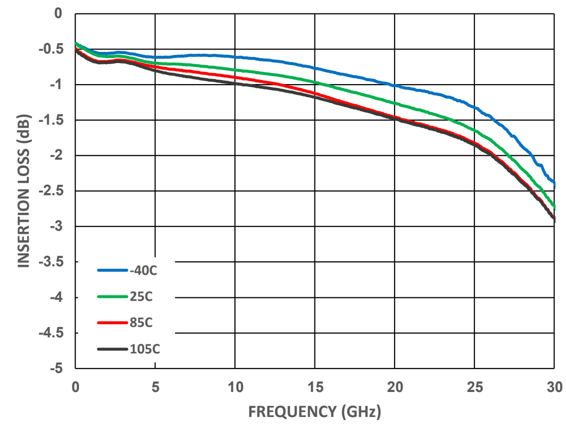


Figure 10. Insertion Loss vs. Frequency over Various Temperatures

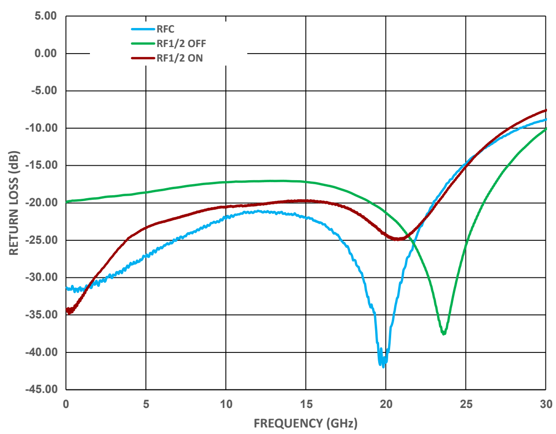


Figure 9. Return Loss vs. Frequency

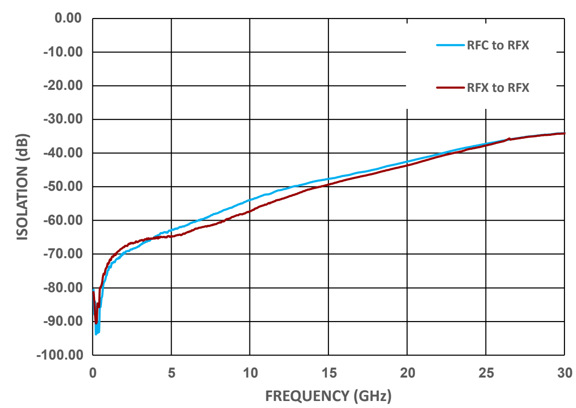


Figure 11. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3, V_{CTRL}= 0 V or V_{DD}, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted.

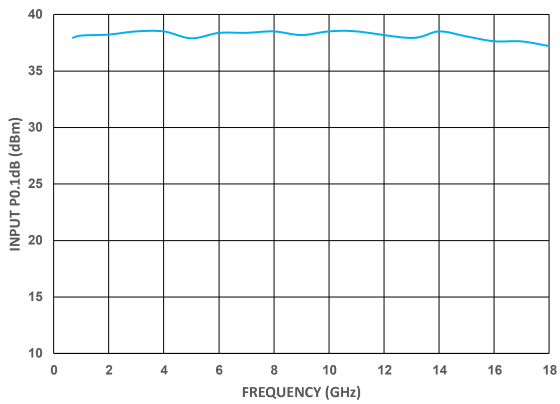


Figure 12. Input P0.1dB vs. Frequency

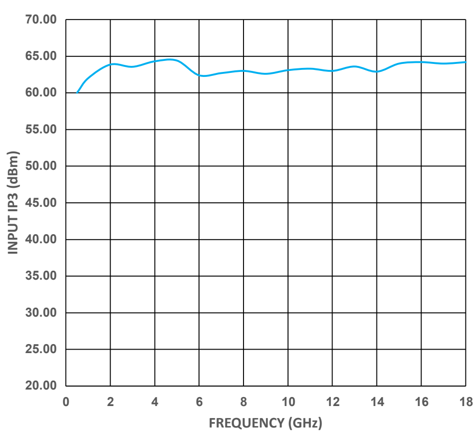


Figure 13. Input IP3 vs. Frequency

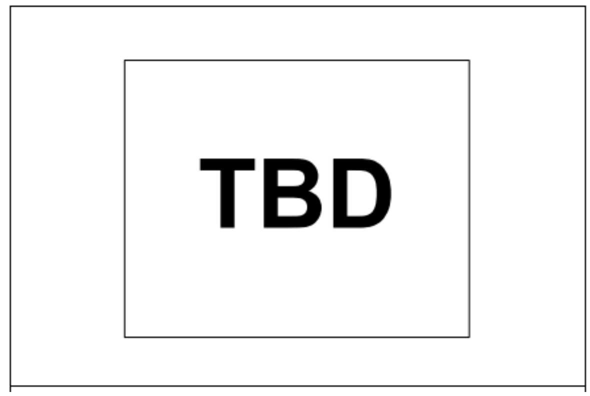


Figure 14. Input P0.1dB vs. Frequency (Low-Frequency Detail)

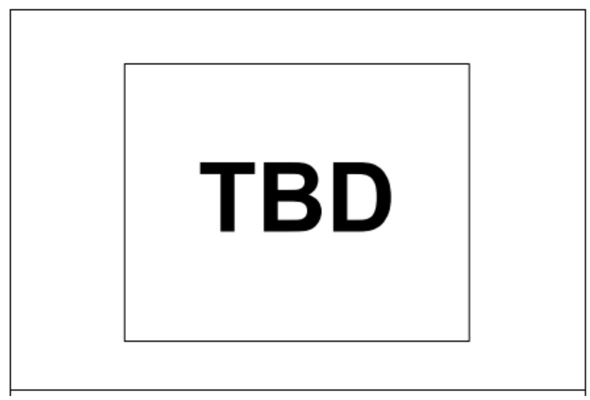


Figure 15. Input IP3 vs. Frequency (Low-Frequency Detail

THEORY OF OPERATION

The ADRF5030 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. There are 2 digital control input pins (EN, CTRL) that determines which RF port is in the insertion loss state and in the isolation state. See Table 7 for the control voltage truth table.

When the EN pin is logic high, all RF paths are in isolation state regardless of the logic state of other pin. The RF ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

RF INPUT AND OUTPUT

The RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC-blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω.

The ADRF5030 is bidirectional with equal power-handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw port. The unselected RF port of the ADRF5030 is non-reflective.

The power handling of the ADRF5030 derates with frequencies below 100 MHz. See Figure 2 for derating of the RF power towards lower frequencies.

POWER SUPPLY

The ADRF5030 requires that a positive supply voltage is applied to the VDD pin and a negative supply voltage to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply RF input signal.

The ideal power-down sequence is the reverse of the above.

Table 7. Control Voltage Truth Table

Digital Control Input		RFx Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low or High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

The ADRF5030 has two power-supply pins (VDD and VSS) and two control pins (EN, CTRL). Figure 16 shows the external components and connections for the supply pin. The VDD and VSS pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC-blocking capacitors on the RF pins when the RF lines are biased at a voltage other than 0 V. See Table 6 for details.

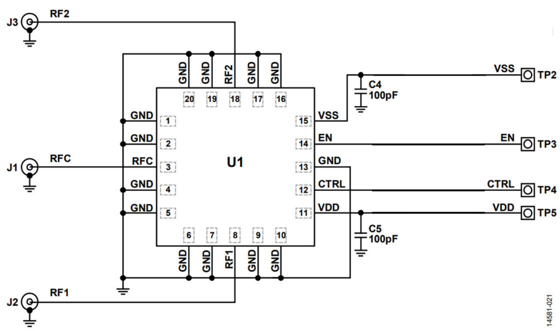


Figure 16. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 17 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003C dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

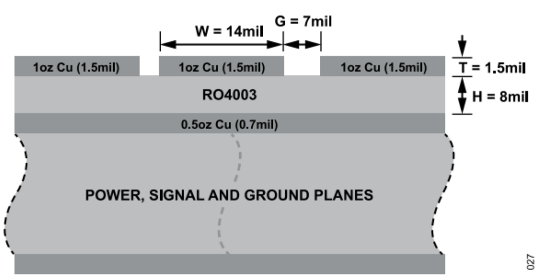


Figure 17. Example PCB Stack-up

Figure 18 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

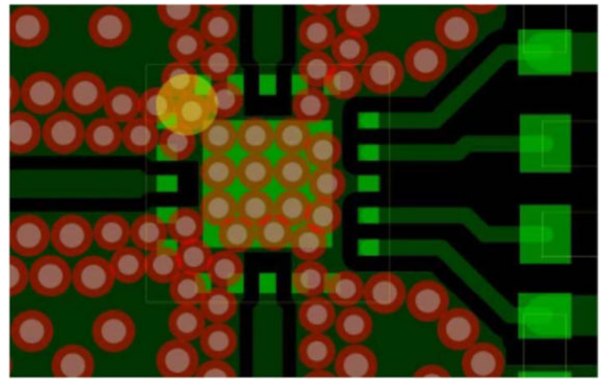


Figure 18. PCB Layout

Figure 19 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width to the package edge and tapered to RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

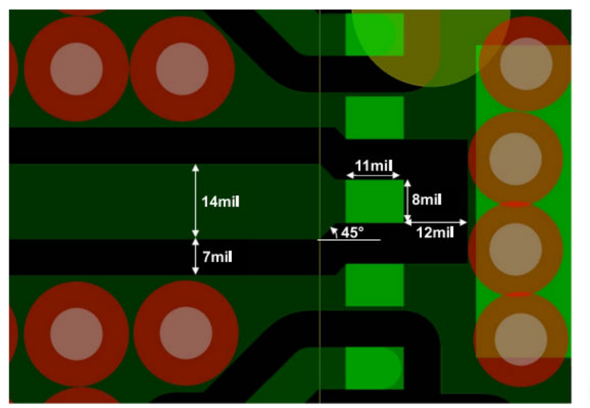


Figure 19. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and RF trace design, contact Analog Devices Technical Support for further recommendations.

OUTLINE DIMENSIONS

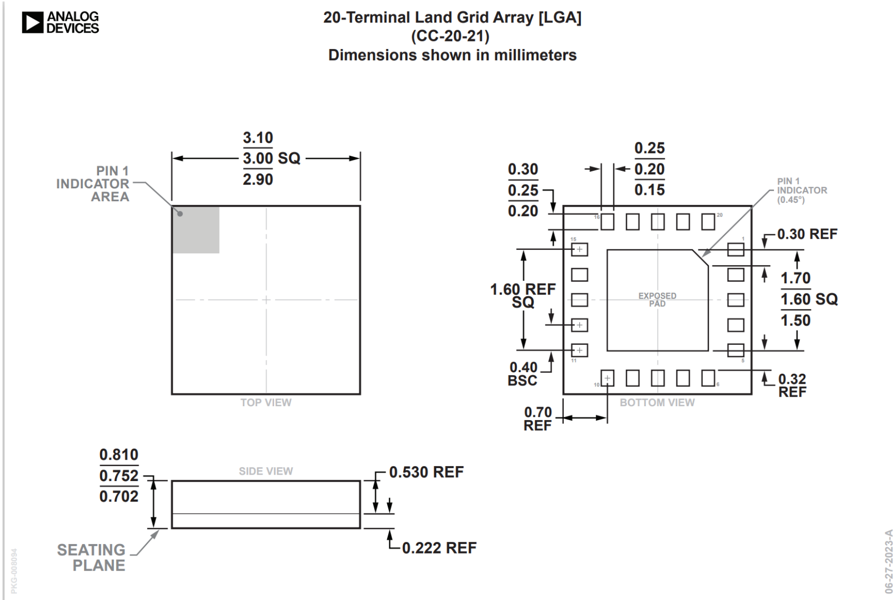


Figure 20. 20-Terminal Land Grid Array [LGA]
3 mm × 3 mm Body and 0.75 mm Package Height (CC-20-21)
Dimensions Shown in Millimeters