

# 24.0 GHz to 29.5 GHz Transmit and Receive Dual Polarization Beamformer

### **FEATURES**

- Integration of a 16 (2 x 8) channel beamformer paired with a 2 transmit and 2 receive UDC
- ▶ RF range: 24.0 GHz to 29.5 GHz
- ▶ Single-ended LO input frequency range:
  - 7 GHz to 9.25 GHz for ×4 mode supporting lower sideband operation
  - 8.5 GHz to 13 GHz for x2 mode supporting upper sideband operation
- Single-ended complex IF operation from 4 GHz to 7 GHz with configurable common or separate transmit and receive IF ports
- $\blacktriangleright$  Beamformer channels and IF ports support 50  $\Omega$  termination in off state
- ▶ Fast TDD switching using TRX x pins
- On-chip temperature sensor for receive and transmit
- Automatic temperature compensation for gain
- Memory for 512 shared transmit and receive beam positions
- ▶ NVM for phase, beamformer, and UDC gain calibration
- Dual power supplies required: 3.3 V and 1.8 V with on-chip LDO voltage regulator for 1.2 V and 1.0 V
- Upconversion mode
  - ► Sideband rejection and carrier feedthrough optimization
  - ► Envelope detector for LO feedthrough calibration
  - ▶ Single channel power detector
- ► Downconversion mode: image reject optimization
- Calibration probes for array calibration
- LO chain features: I/Q phase correction values
- 3-wire or 4-wire SPI that supports up to 133 MHz SPI clock speed
- ▶ 335-ball, 12 mm × 9 mm CSP\_BGA

### **APPLICATIONS**

mmW 5G application

### **GENERAL DESCRIPTION**

The ADMV1228 is a silicon on insulator (SOI), 24.0 GHz to 29.5 GHz, mmW 5G integrated dual-channel upconverter, dual-channel downconverter, and beamformer. The RFIC integrates two transmit and receive (2T2R) configurations that contain 16 independent

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transmit and receive channels that are separated in a 2 by 8 configuration that supports dual polarization or single polarization array configurations (with an external splitter).

Both upconverters and downconverters offer a single mode of frequency translation that requires a complex intermediate frequency (IF) signal. The IF input and output path is configurable to be directly connected into the upconverter or downconverter via the IFV\_IN, IFH\_IN, IFV\_OUT, or IFH\_OUT pins or a common IF input and output pin via the IFV\_CM or IFH\_CM pin.

The upconverter and downconverter (UDC) offer 47.5 dB and 41 dB of dynamic gain range with a resolution of 0.5 dB utilizing the three available digital variable gain amplifiers (DVGAs) that are in the IF and RF section of the UDC and in the RF section for each channel of the beamformer. The DVGAs provide a flat phase response across the full gain range.

In either mode, each transmit and receive beamformer channel includes a vector modulator (VM) to control the phase, and one DVGA to control the amplitude. The VM provides a full 360° phase adjustment range in either transmit or receive mode to provide 6 bits of resolution for 5.625° phase steps. The transmit channels contain individual transmit power detectors.

The ADMV1228 can be programmed using a 3-wire or 4-wire serial port interface (SPI). An integrated, on-chip low dropout (LDO) voltage regulator generates the 1.2 V and 1.0 V supplies for various circuits to reduce the number of supply domains required. The on-chip memory can store up to 512 beam positions that can be allocated for either transmit mode or receive mode for the horizontal channels and vertical channels. On-chip nonvolatile memory (NVM) is used to store the calibrated gain and phase offset coefficients and the reference values for each channel. These values are used to perform channel to channel or chip to chip calibration. A dedicated load pin (LOAD) enables synchronization of all devices in the same array. A horizontal and vertical polarization transmit mode and receive mode control pin (TRX\_H or TRX\_V) is provided for fast switching between transmit mode and receive mode.

The ADMV1228 comes in a compact, 335-ball, 12 mm × 9 mm chip scale package ball grid array (CSP\_BGA). The ADMV1228 operates over the  $-40^{\circ}$ C to +95°C T<sub>C</sub> range. This CSP\_BGA package allows heatsinking from the topside of the package for the most efficient thermal heatsinking and to allow flexible antenna placement on the opposite side of the printed circuit board (PCB).

Rev. Sp0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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## NOTES





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