Data Sheet

ADIS16501

Precision, MEMS IMU

FEATURES

- Triaxial digital gyroscope, ±500°/sec
  - 2.7°/hr in-run bias stability
  - 0.15°/√hr angular random walk, x-axis and y-axis, 1 σ
  - ±0.25° axis to axis misalignment error
- Triaxial digital accelerometer, ±14 *g* dynamic range
  - 12.7 µ*g* in-run bias stability (x-axis and y-axis)
- Triaxial delta angle and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
- SPI compatible data communications
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Data ready indicator for synchronous data acquisition
  - External sync modes: direct, scaled, and output
  - On demand self test of inertial sensors
- Single-supply operation (VDD): 3.0 V to 3.6 V
- 1500 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Navigation, stabilization, and instrumentation
- Unmanned and autonomous vehicles
- Smart agriculture and construction machinery
- Factory/industrial automation, robotics
- Virtual/augmented reality
- Internet of Moving Things

GENERAL DESCRIPTION

The ADIS16501 is a precision, miniature microelectromechanical system (MEMS) inertial measurement unit (IMU) that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16501 combines with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, linear acceleration (gyroscope bias), and point of percussion (accelerometer location).

The ADIS16501 provides a simplified, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The ADIS16501 is available in a 100-ball ball grid array (BGA) module (MODULE) that is approximately 15 mm × 15 mm × 5.72 mm.

FUNCTIONAL BLOCK DIAGRAM

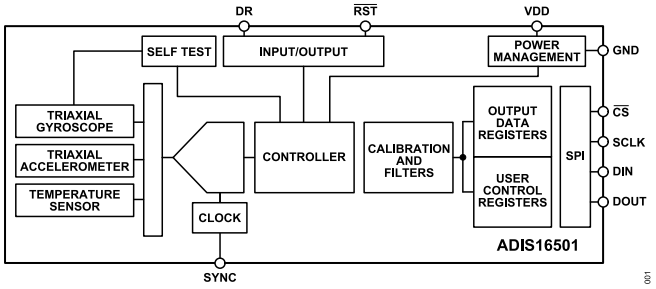

Figure 1. Functional Block Diagram

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

7/2024—Rev. A to Rev. B

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SPECIFICATIONS

Ambient temperature (T_A) = 25°C, VDD = 3.3 V, angular rate = 0°/sec, and dynamic range = ±500°/sec. 1 *g* is the acceleration due to gravity and defined as 9.798245 m/sec^2.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±500			°/sec
Sensitivity	16-bit data format		40		LSB/°/sec
	32-bit data format		2,621,440		LSB/°/sec
Error over Temperature	−40°C ≤ T_A ≤ +85°C, 1σ		±0.5		%
Misalignment Error	Axis to axis, −40°C ≤ T_A ≤ +85°C, 1 σ		±0.25		Degrees
Nonlinearity[1]	FS = 500°/sec		0.25		% FSR
Bias					
Repeatability[2]	−40°C ≤ T_A ≤ +85°C, 1 σ, x-axis and z-axis		0.14		°/sec
	−40°C ≤ T_A ≤ +85°C, 1 σ, y-axis		1.4		°/sec
In-Run Bias Stability	1 σ		2.7		°/hr
Angular Random Walk	X-axis and y-axis, 1 σ		0.15		°/√hr
	Z-axis, 1 σ		0.2		°/√hr
Error over Temperature	−40°C ≤ T_A ≤ +85°C, 1 σ, x-axis and z-axis		±0.3		°/sec
	−40°C ≤ T_A ≤ +85°C, 1 σ, y-axis		±0.7		°/sec
Linear Acceleration Effect	X-axis and y-axis, 1 σ		9.5		°/hr/*g*
	Z-axis, 1 σ		2.3		°/hr/*g*
Vibration Rectified Error (VRE)	Random vibration, 2 *g* rms, 50 Hz to 2 kHz				
	X-axis and y-axis, 1 σ		0.001		°/sec/*g*^{2}
	Z-axis, 1 σ		0.0004		°/sec/*g*^{2}
Output Noise	No filtering, 1 σ, 25°C				
	X-axis, y-axis		0.082		°/sec rms
	Z-axis		0.116		°/sec rms
Rate Noise Density	Frequency = 10 Hz to 40 Hz		0.181		
	X-axis and y-axis		0.0043		°/sec/√Hz rms
	Z-axis		0.0034		°/sec/√Hz rms
3 dB Bandwidth	X-axis and y-axis		480		Hz
	Z-axis		590		Hz
Sensor Resonant Frequency	X-axis, y-axis		66		kHz
	Z-axis		78		kHz
ACCELEROMETERS[3]	Each axis				
Dynamic Range		±14			*g*
Sensitivity	32-bit data format		52,428,800		LSB/*g*
Error over Temperature	−40°C ≤ T_A ≤ +85°C, 1 σ		±0.07		%
Repeatability[2]	−40°C ≤ T_A ≤ +85°C, 1 σ		±0.1		%
Misalignment Error	Axis to axis, −40°C ≤ T_A ≤ +85°C, 1 σ		±0.05		Degrees
Nonlinearity	Best fit straight line, ±2 *g*		0.25		% FSR
	Best fit straight line, ±14 *g*		0.5		% FSR
Bias					
Repeatability[2]	−40°C ≤ T_A ≤ +85°C, 1 σ		6.0		m*g*

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
In-Run Bias Stability	1 σ				
	X-axis and y-axis		12.7		μ*g*
	Z-axis		13.7		μ*g*
Velocity Random Walk	1 σ				
	X-axis and y-axis		0.039		m/sec/√hr
	Z-axis		0.033		m/sec/√hr
Error over Temperature	−40°C ≤ T_A ≤ +85°C, 1 σ		±1.6		m*g*
Output Noise	No filtering		2.5		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		89.6		μ*g*/√Hz rms
3 dB Bandwidth			750		Hz
Sensor Resonant Frequency	X-axis and Y-axis		5.3		kHz
	Z-axis		4.8		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 0°C (±5°C)		0.1		°C/LSB
LOGIC INPUTS[4]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			μs
$\overline{CS}$ Wake-Up Pulse Width		20			μs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	μA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	μA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	Source current (I_{SOURCE}) = 0.5 mA	2.4			V
Low, V_{OL}	Sink current (I_{SINK}) = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[5]	10,000			Cycles
Data Retention[6]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[7]	Time until data is available				
Power-On Start-Up Time			342		ms
Reset Recovery Time[8]	GLOB_CMD, Bit 7 = 1 (see Table 113)		282		ms
Factory Calibration Restore	GLOB_CMD, Bit 1 = 1 (see Table 113)		1		ms
Flash Memory Backup	GLOB_CMD, Bit 3 = 1 (see Table 113)		146		ms
Flash Memory Test Time	GLOB_CMD, Bit 4 = 1 (see Table 113)		48		ms
Self Test Time	GLOB_CMD, Bit 2 = 1 (see Table 113)		29		ms
CONVERSION RATE			2000		SPS
Initial Clock Accuracy			3		%
Sync Input Clock		1.9		2.1	kHz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[9]	Normal mode, VDD = 3.3 V		44	55	mA

SPECIFICATIONS

[1] This measurement is based on the deviation from a best fit linear model.

[2] Bias repeatability provides an estimate for long-term drift in the bias, as observed during 500 hours of high temperature operating life (HTOL) at 105°C.

[3] All specifications associated with the accelerometers relate to the full-scale range of ±14 *g*, unless otherwise noted.

[4] The digital input/output signals use a 3.3 V system.

[5] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

[6] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.

[7] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

[8] The $\overline{RST}$ line must be in a low state for at least 10 µs to ensure a proper reset initiation and recovery.

[9] Power supply current transients can reach 100 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_A = 25°C and VDD = 3.3 V, unless otherwise noted.

Table 2.

		Normal Mode			Burst Read Mode			
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{SCLK}	Serial clock	0.1		10	0.1		1.1	MHz
t_{STALL}	Stall period between data	16			N/A[1]			µs
$t_{READRATE}$	Read rate	24						µs
$t_{\overline{CS}}$	Chip select to SCLK edge	200			200			ns
t_{DAV}	DOUT valid after SCLK edge			25			25	ns
t_{DSU}	DIN setup time before SCLK rising edge	25			25			ns
t_{DHD}	DIN hold time after SCLK rising edge	50			50			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise/fall times		5	12.5		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise/fall times		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			0			ns
t_1	Input sync positive pulse width, direct sync mode, MSC_CTRL, Bits[3:2] = 01 (binary, see Table 107)	5			5			µs
t_{STDR}	Input sync to data ready valid transition, no SPI traffic, direct sync mode, MSC_CTRL, Bits[3:2] = 01 (binary, see Table 107)		305			305		µs
	Input sync to data ready valid transition, full SPI traffic[2], direct sync mode, MSC_CTRL, Bits[3:2] = 01 (binary, see Table 107)		405			405		µs
t_{NV}	Data invalid time		23			23		µs
t_2	Input sync period	500			500			µs

[1] N/A means not applicable.

[2] Full SPI traffic is defined as a transfer of 64 16-bit registers using an SCLK frequency of 2 MHz. Reading the sensor values from the previous data sample proportionally increases the t_{STDR} on the current cycle.

SPECIFICATIONS

Timing Diagrams

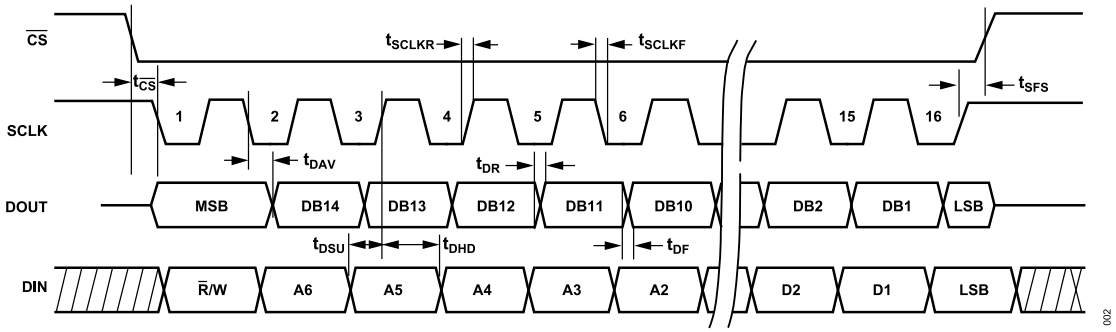

Figure 2. SPI Timing and Sequence Diagram

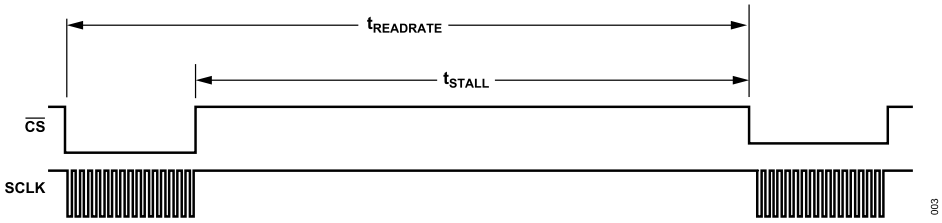

Figure 3. Stall Time and Data Rate Timing Diagram

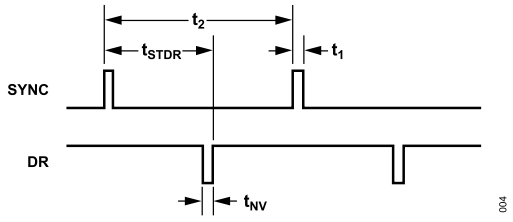

Figure 4. Input Clock Timing Diagram, Direct Sync Mode, Register MSC_CTRL, Bits[3:2] = 01 (Binary)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered, 0.5 ms	1500 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The ADIS16501 is a multichip module that includes many active components. The values in Table 4 identify the thermal response of the hottest component inside of the ADIS16501, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction temperature (T_J) inside of the ADIS16501 is 76.7°C.

$$T_J = \theta_{JA} \times VDD \times I_{DD} + 70°C$$

$$T_J = 107.1°C/W \times 3.3\ V \times 0.044\ A + 70°C$$

$$T_J = 85.6°C$$

Table 4. Package Characteristics

Package Type	θ_{JA}[1]	θ_{JC}[2]	Device Weight
ML-100-1[3]	107.1°C/W	74.7°C/W	<1.3 g

1 θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

2 θ_{JC} is the junction to case thermal resistance.

3 Thermal impedance values come from direct observation of the hottest temperature inside of the ADIS16501 when it is attached to an FR4-08 PCB that has two metal layers and has a thickness of 0.063 inches.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

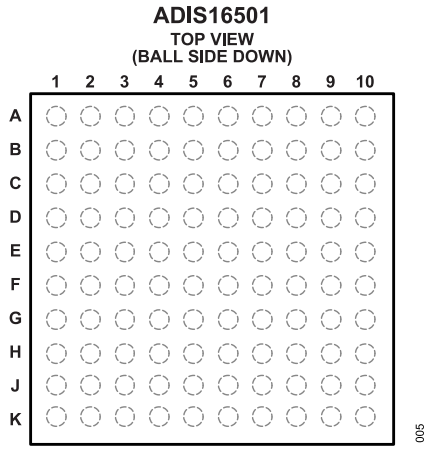

Figure 5. Pin Assignments, Bottom View

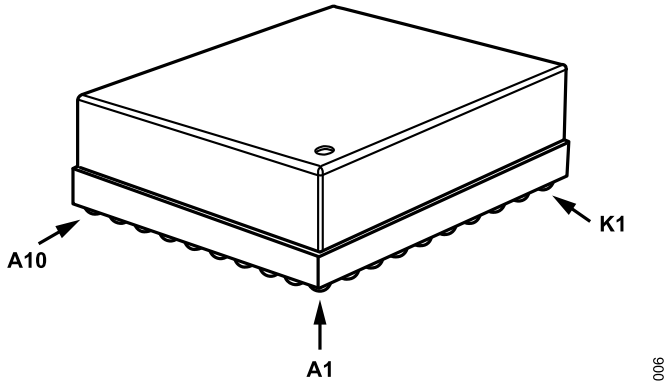

Figure 6. Pin Assignments, Package Level View

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Supply	Power Ground
A2	GND	Supply	Power Ground
A3	GND	Supply	Power Ground
A4	GND	Supply	Power Ground
A5	GND	Supply	Power Ground
A6	GND	Supply	Power Ground
A7	GND	Supply	Power Ground
A8	GND	Supply	Power Ground
A9	NC	Not applicable	No Connection
A10	NC	Not applicable	No Connection
B1	NC	Not applicable	No Connection
B2	NC	Not applicable	No Connection
B3	GND	Supply	Power Ground
B4	GND	Supply	Power Ground
B5	GND	Supply	Power Ground
B6	GND	Supply	Power Ground
B7	NC	Not applicable	No Connection
B8	NC	Not applicable	No Connection
B9	NC	Not applicable	No Connection
B10	NC	Not applicable	No Connection
C1	NC	Not applicable	No Connection
C2	GND	Supply	Power Ground
C3	DNC	Not applicable	Do Not Connect
C4	NC	Not applicable	No Connection
C5	NC	Not applicable	No Connection
C6	GND	Supply	Power Ground
C7	VDD	Supply	Power Supply
C8	NC	Not applicable	No Connection
C9	NC	Not applicable	No Connection
C10	NC	Not applicable	No Connection
D1	NC	Not applicable	No Connection

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
D2	NC	Not applicable	No Connection
D3	GND	Supply	Power Ground
D4	NC	Not applicable	No Connection
D5	NC	Not applicable	No Connection
D6	VDD	Supply	Power Supply
D7	NC	Not applicable	No Connection
D8	NC	Not applicable	No Connection
D9	NC	Not applicable	No Connection
D10	NC	Not applicable	No Connection
E1	NC	Not applicable	No Connection
E2	GND	Supply	Power Ground
E3	VDD	Supply	Power Supply
E4	NC	Not applicable	No Connection
E5	NC	Not applicable	No Connection
E6	GND	Supply	Power Ground
E7	GND	Supply	Power Ground
E8	NC	Not applicable	No Connection
E9	NC	Not applicable	No Connection
E10	NC	Not applicable	No Connection
F1	GND	Supply	Power Ground
F2	NC	Not applicable	No Connection
F3	A	Input	Reset
F4	NC	Not applicable	No Connection
F5	GND	Supply	Power Ground
F6	GND	Supply	Power Ground
F7	NC	Not applicable	No Connection
F8	GND	Supply	Power Ground
F9	NC	Not applicable	No Connection
F10	NC	Not applicable	No Connection
G1	VDD	Supply	Power Supply
G2	GND	Supply	Power Ground
G3	A	Input	SPI, Chip Select
G4	NC	Not applicable	No Connection
G5	NC	Not applicable	No Connection
G6	DIN	Input	SPI, Data Input
G7	GND	Supply	Power Supply
G8	NC	Not applicable	No Connection
G9	NC	Not applicable	No Connection
G10	NC	Not applicable	No Connection
H1	VDD	Supply	Power Supply
H2	NC	Not applicable	No Connection
H3	DOUT	Output	SPI, Data Output
H4	NC	Not applicable	No Connection
H5	NC	Not applicable	No Connection

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
H6	SCLK	Input	SPI, Serial Clock
H7	NC	Not applicable	No Connection
H8	GND	Supply	Power Ground
H9	NC	Not applicable	No Connection
H10	NC	Not applicable	No Connection
J1	NC	Not applicable	No Connection
J2	GND	Supply	Power Ground
J3	SYNC	Input	Sync (External Clock)
J4	VDD	Supply	Power Supply
J5	VDD	Supply	Power Supply
J6	DR	Output	Data Ready
J7	GND	Supply	Power Ground
J8	NC	Not applicable	No Connection
J9	NC	Not applicable	No Connection
J10	NC	Not applicable	No Connection
K1	GND	Supply	Power Ground
K2	NC	Not applicable	No Connection
K3	GND	Supply	Power Ground
K4	NC	Not applicable	No Connection
K5	NC	Not applicable	No Connection
K6	VDD	Supply	Power Supply
K7	NC	Not applicable	No Connection
K8	GND	Supply	Power Ground
K9	NC	Not applicable	No Connection
K10	NC	Not applicable	No Connection

TYPICAL PERFORMANCE CHARACTERISTICS

GYROSCOPES

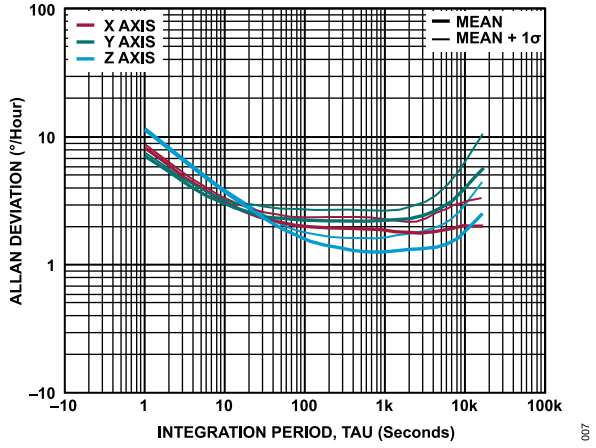

Figure 7. Gyroscope Allan Deviation, T_A = 25°C, Plot Taken After 10 Hours of Settling Time

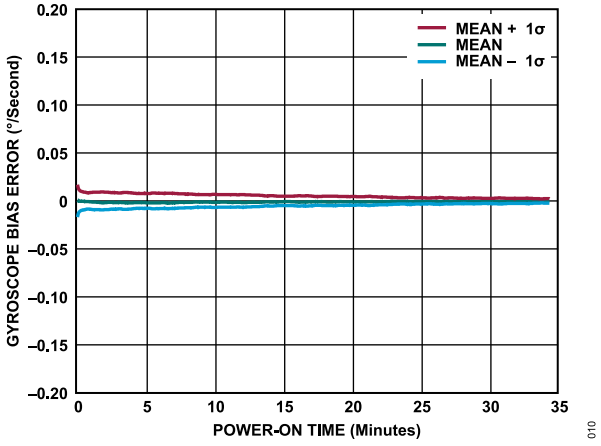

Figure 10. Gyroscope Bias Error vs. Power-On Time, T_A = 25°C, X-Axis Gyroscope

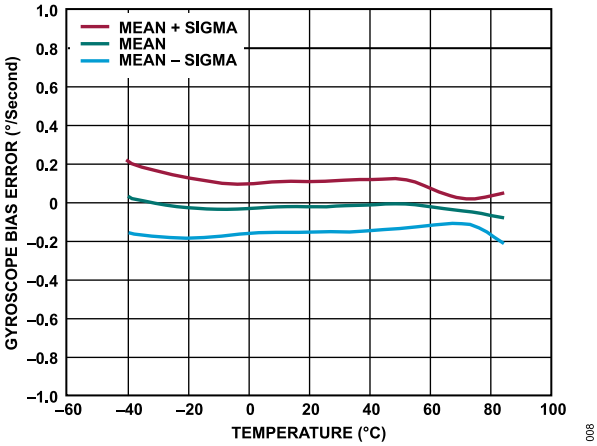

Figure 8. Gyroscope Bias Error vs. Temperature, All Axes

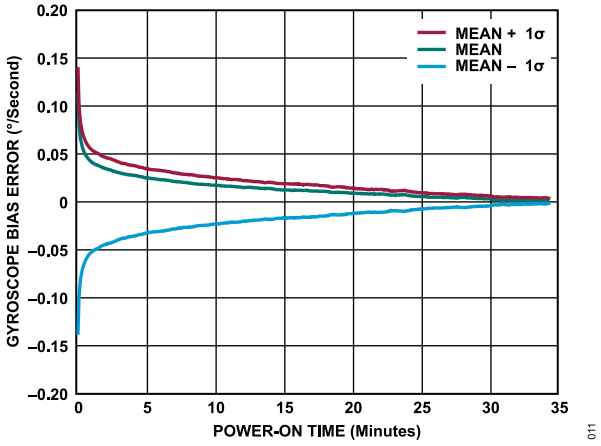

Figure 11. Gyroscope Bias Error vs. Power-On Time, T_A = 25°C, Y-Axis Gyroscope

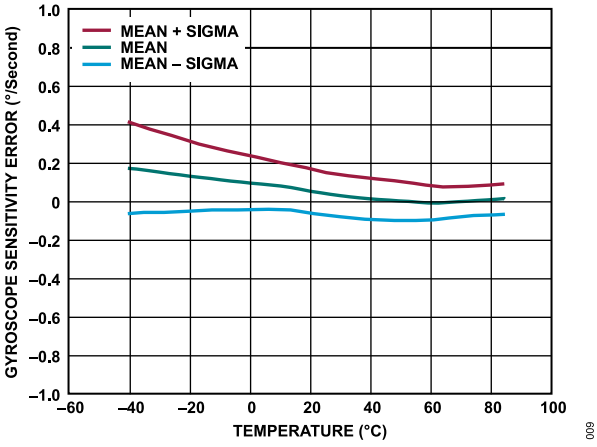

Figure 9. Gyroscope Sensitivity Error vs. Temperature, All Axes

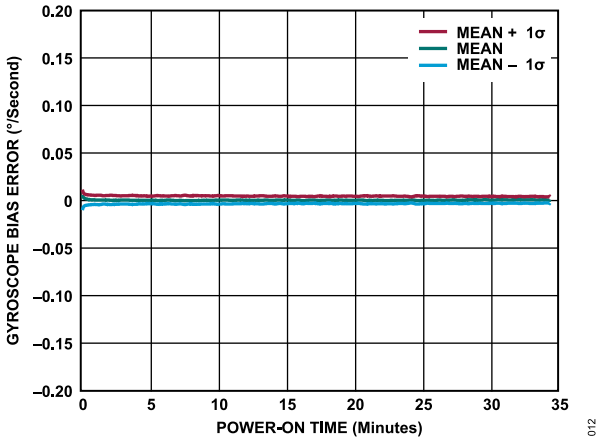

Figure 12. Gyroscope Bias Error vs. Power-On Time, T_A = 25°C, Z-Axis Gyroscope

TYPICAL PERFORMANCE CHARACTERISTICS

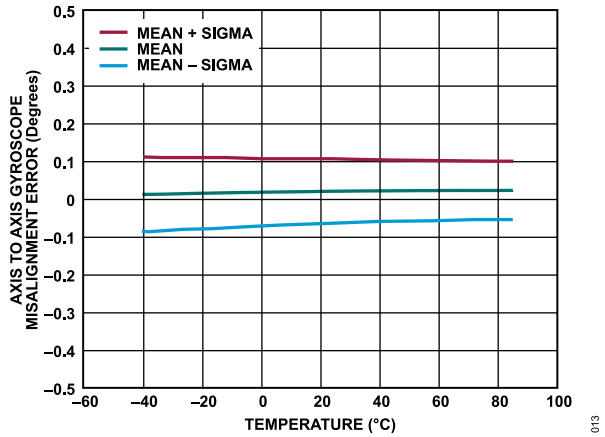

Figure 13. Axis to Axis Gyroscope Misalignment Error vs. Temperature, All Axes

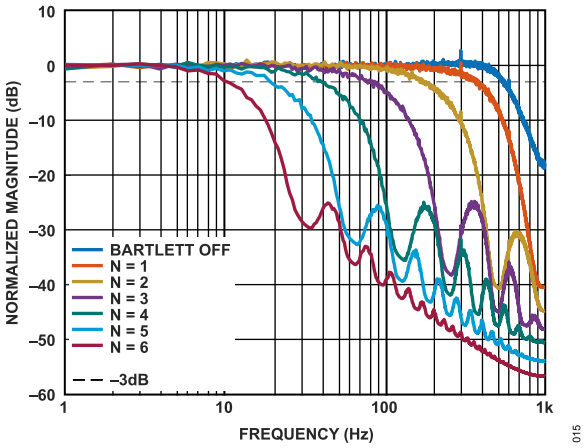

Figure 14. Normalized Gyroscope Noise Density, All Axes, T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

ACCELEROMETERS

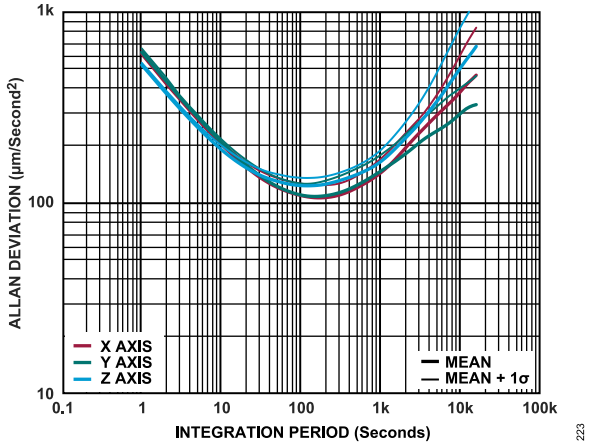

Figure 15. Accelerometer Allan Deviation, T_A = 25°C

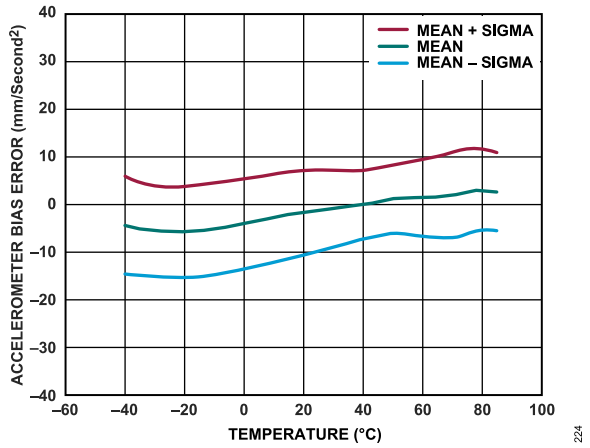

Figure 16. Accelerometer Bias Error vs. Temperature, All Axes

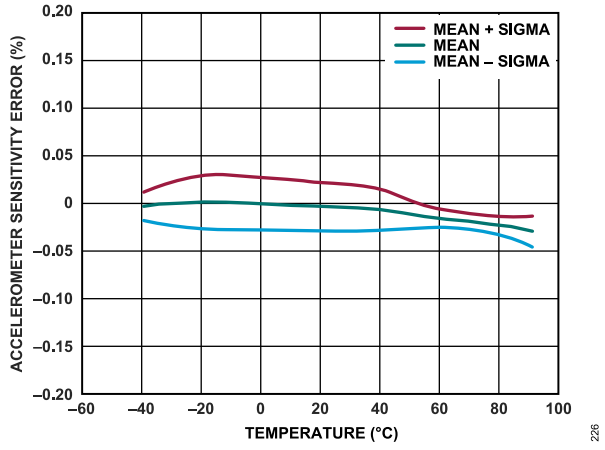

Figure 17. Accelerometer Sensitivity Error vs. Temperature, Cold to Hot, All Axes

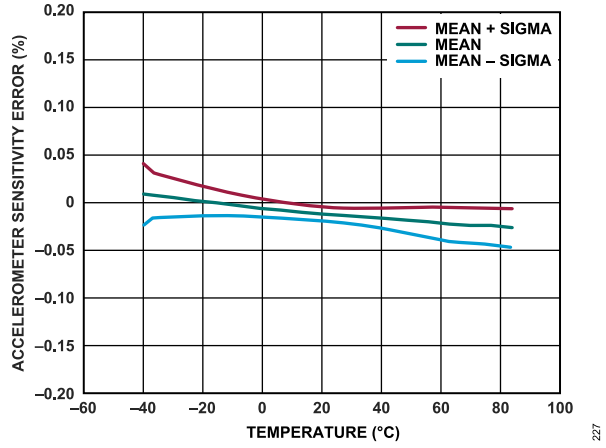

Figure 18. Accelerometer Sensitivity Error vs. Temperature, Hot to Cold, All Axes

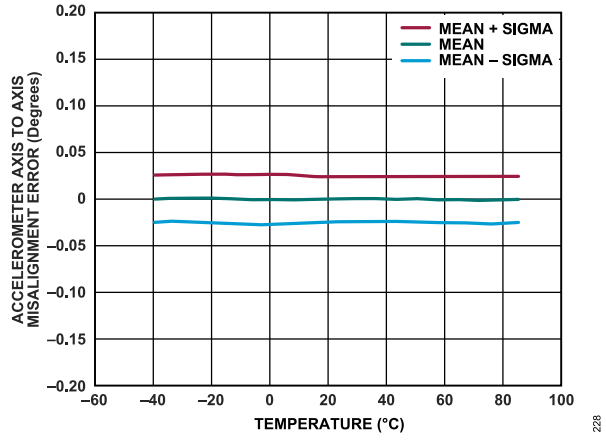

Figure 19. Accelerometer Axis to Axis Misalignment Error vs. Temperature

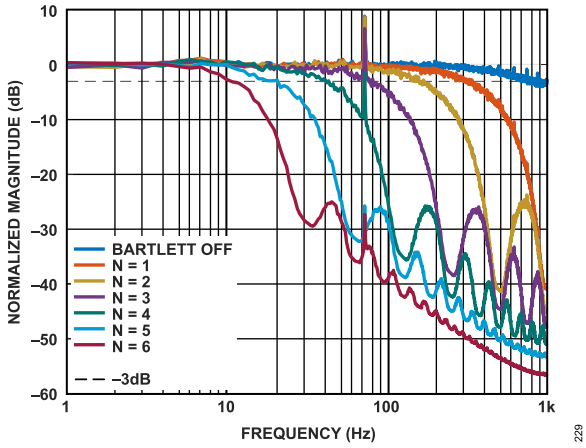

Figure 20. Accelerometer Normalized Noise Density

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Output Full-Scale Range

Output full-scale range is the guaranteed angular rate and acceleration measurement range at the output of the signal chain. The output full-scale range is specified as a minimum value and is guaranteed across all conditions. Angular rate and acceleration measurement are possible beyond this value. However, performance characteristics are not guaranteed.

Bias

Bias is any static (DC) error term on the output of the ADIS16501. It is measured as the deviation from 0°/sec or 0 *g* without externally applied angular rate or acceleration (including gravity). Bias is measured after the device is soldered to the application PCB.

To reduce the influence of external physical stimuli that may exist in the measurement system, average bias over a sufficiently long time window. Additionally, a data rate of >1 kHz is recommended.

Gyroscope = Ω_{MEAS} (Ω_{IN} = 0°/sec)

To calculate accelerometer bias, take measurements at orientations of +1 *g* and −1 *g* and calculate the average value of the two measurements.

$$XL = \frac{ACC_{MEAS}(g_{IN} = +1g) + ACC_{MEAS}(g_{IN} = -1g)}{2}$$

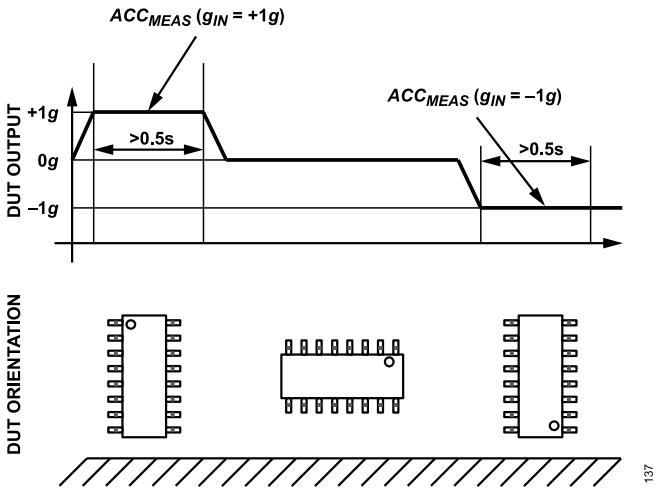

Figure 21. Acceleration Sensitivity Measurement Process

Bias Error over Temperature

Bias error over temperature is the change in bias directly attributed to changes in temperature. Bias error over temperature is measured relative to the bias at 25°C. Figure 22 shows the bias error over temperature expected for a device with a bias at 25°C equivalent to the initial (start of life) bias.

Bias drift over life can cause the offset measured at 25°C to diverge from the initial (start of life) bias measured during module manufacture. Figure 23 shows how the bias error over temperature limits is adjusted to accommodate the divergence of the bias at 25°C and the initial bias.

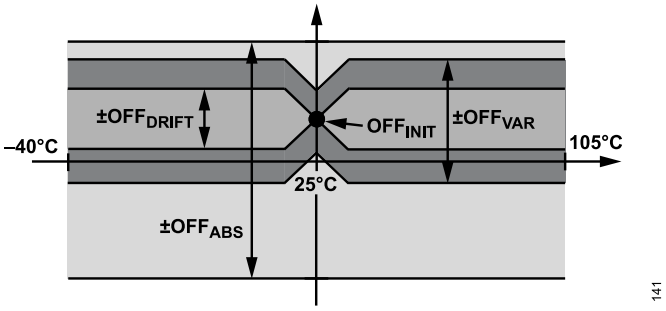

Figure 22. Bias Error over Temperature, $OFF_{INIT} = OFF_{AT\_25°C}$

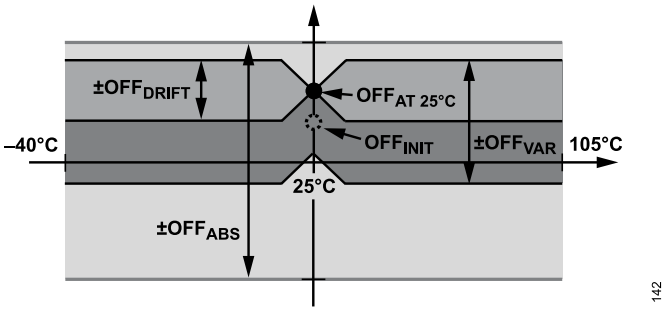

Figure 23. Bias Error over Temperature, $OFF_{INIT} \neq OFF_{AT\_25°C}$ (Change $OFF_{AT\_25°C}$ to $OFF_{AT\_25°C}$)

Bias Repeatability

Bias repeatability describes the long-term offset behavior over a variety of conditions. Bias repeatability represents a projection for long-term aging, which is derived from the drift behaviors that a sample of units exhibits throughout a 1000-hour, 110°C high temperature operating life (HTOL) stress.

In-Run Bias Stability

In-run bias (offset) stability is a measure of how quickly gyroscope (or accelerometer) outputs drift over time. In-run bias stability is derived from the minimum of the Allan variance curve as follows:

Accelerometer Allan Variance(τ) =

$$\sqrt{\frac{1}{2(n-1)}\sum_i \left(ACC_{MEAS}(\tau)_{i+1} - ACC_{MEAS}(\tau)_i\right)^2}$$

Gyroscope Allan Variance(τ) =

$$\sqrt{\frac{1}{2(n-1)}\sum_i \left(\Omega_{MEAS}(\tau)_{i+1} - \Omega_{MEAS}(\tau)_i\right)^2}$$

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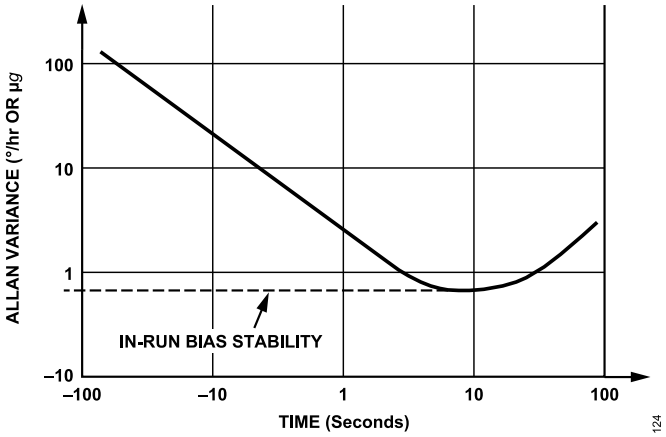

Figure 24. Allan Variance Plot Example

Inertial Data Format

Inertial data format is the digital representation of the angular rate or acceleration information output by the ADIS16501. Both the angular rate and acceleration information are transmitted as 16-bit (or 24-bit), twos complement values. Nominal sensitivity and nominal scale factor define the relationship for converting from the digital 16-bit (or 24-bit) value to either acceleration or angular rate.

Nominal Sensitivity

Nominal sensitivity is the slope of the line of best fit for the angular rate and acceleration transfer functions, as measured across the output full-scale range (FSR) of the ADIS16501. The sensitivity defines the change in output (LSB) per unit change of input (*g* or °/sec).

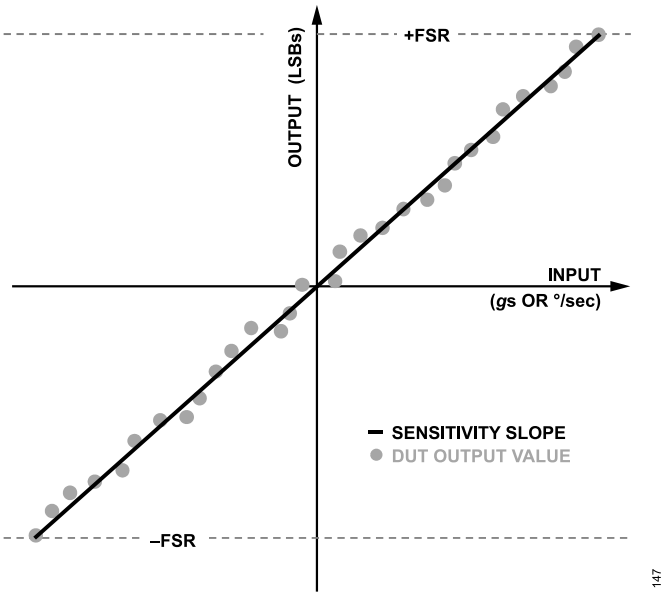

Figure 25. Nominal Sensitivity Slope

Nominal Scale Factor

The nominal scale factor is the inverse of the nominal sensitivity. It is the slope of the line of best fit for the angular rate and acceleration transfer functions, as measured across the output FSR of the ADIS16501. The nominal scale factor describes the change in input (*g* or °/sec) per change in the device output (LSB).

Sensitivity/Scale Factor Tolerance

The sensitivity/scale factor tolerance is the allowable variation between the applied angular rate or acceleration and the digital output (LSB). The acceleration sensitivity can be validated at inputs of ±1 *g*, and the angular rate sensitivity can be validated at any input greater than ±50°/sec.

Acceleration =

$$\frac{ACC_{MEAS}(g_{IN} = +1g) + ACC_{MEAS}(g_{IN} = -1g)}{2g}$$

Gyroscope =

$$\frac{\Omega_{MEAS}(\Omega_{IN} = +50°/sec) - \Omega_{MEAS}(\Omega_{IN} = -50°/sec)}{100°/sec}$$

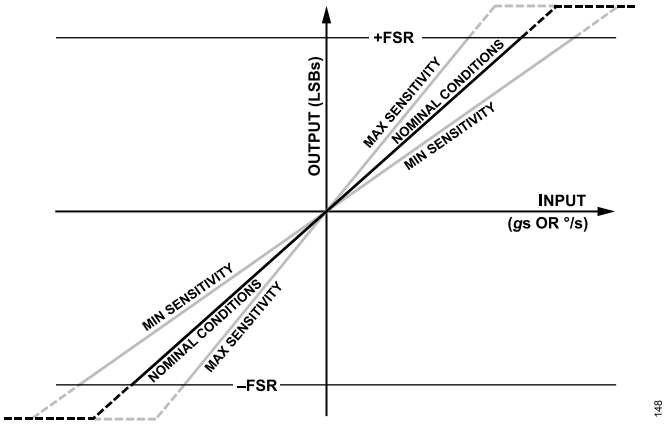

Figure 26. Sensitivity/Scale Factor Transfer Function

Cross Axis Sensitivity

Cross axis sensitivity is the measured output of the device in response to input stimuli orthogonal to the measurement axis. It is measured as a percentage of the applied orthogonal acceleration or rotation rate. All stimulus axes are defined relative to the package body as follows:

$$Gyroscope = \left[\frac{\Omega_{MEAS}(\Omega_Z)}{\Omega_X(\text{or}\,\Omega_Y)}\right] \times 100\,\%$$

$$Acceleration = \left[\frac{ACC_{MEAS}(g_X)}{g_Y(\text{or}\ g_Y)}\right] \times 100\,\%$$

where:
Ω_{MEAS} (Ω_Z) is the measured angular rate.
Ω_X (or Ω_Y) is the applied pitch or roll rate.
ACC_{MEAS} (g_X) is the measured x-axis acceleration.
g_Y (or g_Z) is the applied y- or z-axis acceleration.

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Nonlinearity

Nonlinearity is the maximum deviation of any sensor data point ($\Omega_{MEAS}(\Omega_n)$ or $ACC_{MEAS}(g_n)$) from the least squares linear fit of the sensor data at an equivalent applied angular rate or acceleration. Nonlinearity is mathematically expressed as

$$Gyroscope = \Omega_{MEAS}(\Omega_n) - \Omega_{CALC}(\Omega_n)$$

$$Acceleration = ACC_{MEAS}(g_n) - ACC_{CALC}(g_n)$$

where:
Ω_{MEAS} is the measured angular rate at Ω_n.
Ω_{CALC} is the linear fit calculation of the angular rate at Ω_n.
ACC_{MEAS} is the measured acceleration at g_n.
ACC_{CALC} is the linear fit calculation of acceleration at g_n.

For testing across a range of ±125°/sec (gyroscope) or ±2.5 *g* (accelerometer), apply the following input stimulus profile:

$$\Omega_n = -125°/sec + (n \times 2.5)$$

where n = 0, 1, …, 100.

$$g_n = -2.5\ g + (n \times 0.05)$$

where n = 0, 1, …, 100.

For testing across a range of ±500°/sec (gyroscope) or ±14 *g* (accelerometer), apply the following input stimulus profile:

$$\Omega_n = -500°/sec + (n \times 5)$$

where n = 0, 1, …, 200.

$$g_n = -14\ g + (n \times 0.2)$$

where n = 0, 1, …, 100.

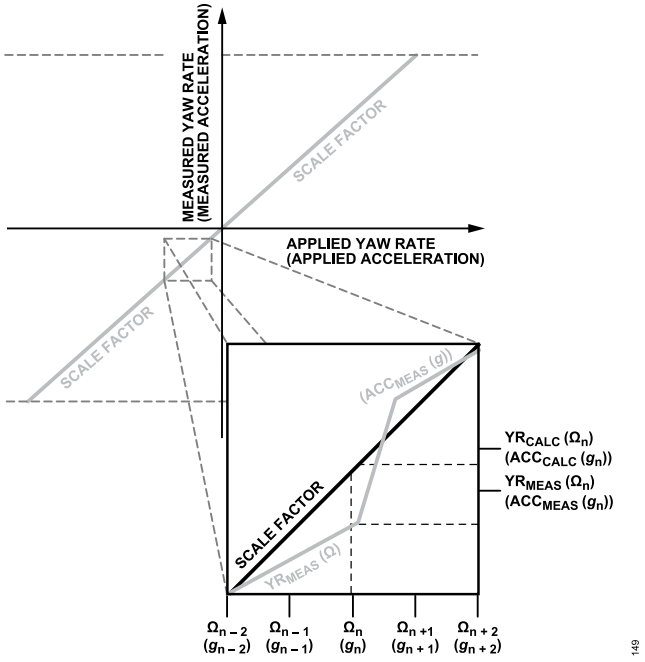

Figure 27. Nonlinearity Characteristic

Microlinearity

Microlinearity is the maximum deviation of the gradient between two neighboring sensor data points as compared to the scale factor calculated from the least squares linear fit of the sensor data. Microlinearity is mathematically expressed as

$$Gyroscope = \left[\frac{\Omega_{MEAS}(\Omega_n + 1) - \Omega_{MEAS}(\Omega_n)}{\Omega_{STEP} \times Sensitivity}\right] \times 100\ \%$$

$$Acceleration = \left[\frac{ACC_{MEAS}(g_n + 1) + ACC_{MEAS}(g_n)}{g_{STEP} \times Sensitivity} - 1\right] \times 100\ \%$$

where:
Ω_{MEAS} is the measured angular rate at a defined Ω_n.
ACC_{MEAS} is the measured acceleration at a defined g_n.

For testing across a range of ±125°/sec (gyroscope) or ±2.5 *g* (accelerometer), apply the following input stimulus profile:

$$\Omega_{STEP} = 5°/sec$$

$$g_{STEP} = 100\ mg$$

$$\Omega_n = -125°/sec + (n \times \Omega_{STEP})$$

where n = 0, 1, …, 50.

$$g_n = -2.5\ g + (n \times g_{STEP})$$

where n = 0, 1, …, 50.

For testing across a range of ±500°/sec (gyroscope) or ±14 *g* (accelerometer), apply the following input stimulus profile:

$$\Omega_{STEP} = 10°/sec$$

$$g_{STEP} = 250\ mg$$

$$\Omega_n = -500°/sec + (n \times \Omega_{STEP})$$

where n = 0, 1, …, 99.

$$g_n = -14\ g + (n \times g_{STEP})$$

where n = 0, 1, …, 95.

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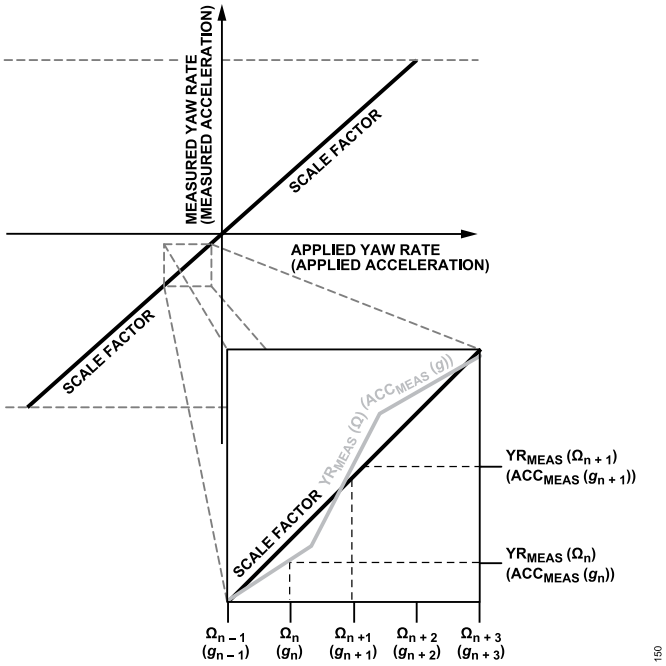

Figure 28. Microlinearity Characteristic

Cutoff (−3 dB) Frequency

For applied AC acceleration and angular rates, cutoff (−3 dB) frequency is the frequency at which the input stimulus is attenuated in amplitude by 29.3% (1 − √2 ÷ 2) at the output of the signal chain. The −3 dB corner is set according to the electrical signal chain filter selected by the user. All other signal chain elements have an appreciably high bandwidth and are not significant contributors to the cutoff frequency.

Cutoff (−3 dB) Frequency Tolerance

Cutoff (−3 dB) frequency tolerance is the allowable variation to the frequency at which a −3 dB (29.3%) signal attenuation is achieved. The device clock directly correlates to the cutoff frequency achieved by the ADIS16501. For each percent that the device clock frequency varies from its nominal value, so too does the cutoff frequency.

Low-Pass Filter Group Delay

The low-pass filter group delay is the time required for the signal chain output to transition from 10% to 90% of its final value. Low-pass filter group delay is measured in response to an applied step change in acceleration or angular rate. The low-pass filter group delay tolerance is equivalent to the cutoff (−3 dB) frequency tolerance.

RMS Noise

RMS noise is the standard deviation of the acceleration or angular rate output without an applied inertial stimulus. RMS noise can be specified at either room temperature (25°C ± 5°C), or over the entire operating temperature range (−40°C to +105°C). The calculation method to assess the RMS noise is the same, regardless of the temperature range. Make this measurement with a sufficiently high sample rate and sufficiently long duration to ensure that adequate accuracy and repeatability are achieved according to the requirements of the measurement system.

$$RMS\ \ noise = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - x)^2}$$

where:
n is the number of sample values.
x_i is the individual sample value.
x is the mean value of the population.

Resonant Frequency

Resonant frequency is also known as natural frequency (f_0). Input acceleration at the resonant frequency of a MEMS element causes the sensor to displace by an amount equivalent to the applied acceleration multiplied by the quality factor. For either underdamped or overdamped systems, acceleration applied at the resonant frequency is not inherently destructive to the MEMS element.

Quality Factor

The quality factor is a scalar factor that governs the increase or decrease in amplitude of an acceleration signal applied at the resonant frequency of a MEMS element.

Sensitivity to Linear Acceleration (Limited Condition, Gyroscope Only)

Sensitivity to linear acceleration is the change in the angular rate output of the ADIS16501 in response to an applied linear acceleration. It is measured in °/sec/*g*. Reduced sensitivity to linear acceleration improves the angular rate signal accuracy in harsh environments where shock and vibration are present. Analog Devices, Inc., validates the gyroscope sensitivity to linear acceleration through the application of both DC acceleration and Haversine shock testing (<90 *g* peak and ≤10 ms duration).

Power-On Reset (POR)

After either a hardware or software reset, the ADIS16501 performs a series of internal diagnostic routines to ensure the integrity of its various signal chains. Although the inertial channels are not fully settled until t_{SETTLE} elapses, SPI communications can be conducted after a minimum holdoff time of t_{POR}. This allows the system to request noninertial data, apply desired configurations, or run the available diagnostic routines.

THEORY OF OPERATION

INTRODUCTION

Figure 29 provides the basic signal chain for the accelerometers and gyroscopes of the ADIS16501. When using the factory default configuration, the ADIS16501 initializes itself at power-up and automatically starts a continuous process of sampling, processing, and loading calibrated sensor data into its output registers at a rate of 2000 SPS.

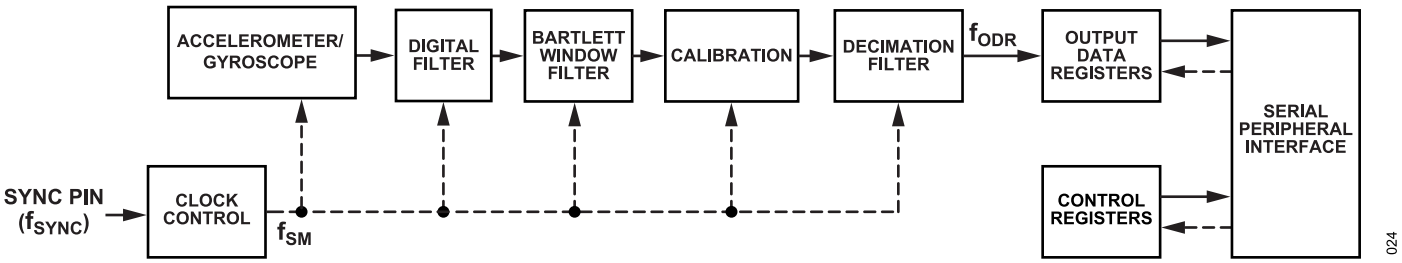

Figure 29. Sensor Signal Chain

THEORY OF OPERATION

CLOCK CONTROL

The ADIS16501 provides four modes of operation with respect to the source of the sampling and processing clock (see the frequency sampling clock (f_{SM}) in Figure 29): internal, direct input sync, scaled sync, and output sync. The MSC_CTRL register, Bits[3:2] (see Table 106 and Table 107) provide user selection of these modes.

Internal Clock Mode

Setting Register MSC_CTRL, Bits[3:2] = 00 selects the internal clock mode and is the default. In this mode, the ADIS16501 uses an internally generated clock that has a nominal frequency of 2000 Hz to drive sampling and data processing for each sensor and associated signal chain.

Direct Input Sync Mode

Setting Register MSC_CTRL, Bits[3:2] = 01 selects direct input sync mode and allows f_{SM} to come directly from an external clock to control the sensor sampling using the SYNC pin as an input. When operating in input sync mode, the ADIS16501 performs best when the external clock frequency (f_{SYNC}) is between 1900 Hz and 2100 Hz.

Scaled Sync Mode

Setting Register MSC_CTRL, Bits[3:2] = 10 selects scaled sync mode, which supports use of an external sync clock between 1 Hz and 128 Hz that can come from video systems or global positioning systems (GPSs). When operating in scaled sync mode, the frequency of the sample clock is equal to the product of the external clock scale factor, K_{ECSF} (from the UP_SCALE register, see Table 108 and Table 109), and the frequency of the clock signal on the SYNC pin. As in input sync mode, the ADIS16501 performs best when f_{SM} is between 1900 Hz and 2100 Hz.

Changes to the UP_SCALE register value reset the clock multiplication phase-locked loop (PLL) and restart the locking process. The locking process starts with an input reference clock edge resetting the feedback clock edge, and lock is declared when time differences between these two edges are ≤100 µs.

For example, when using a 1 Hz input signal, set UP_SCALE = 0x07D0 (K_{ECSF} = 2000 (decimal)) to establish a sample rate of 2000 SPS for the inertial sensors and their signal processing. Use the following sequence on the DIN pin to configure UP_SCALE for this scenario: 0xE2D0, then 0xE307.

Output Sync Mode

When Register MSC_CTRL, Bits[3:2] = 11, the ADIS16501 operates in output sync mode, which is the same as internal clock mode except that the SYNC pin pulses when the internal processor collects data from the inertial sensors. Figure 30 provides an example of this signal.

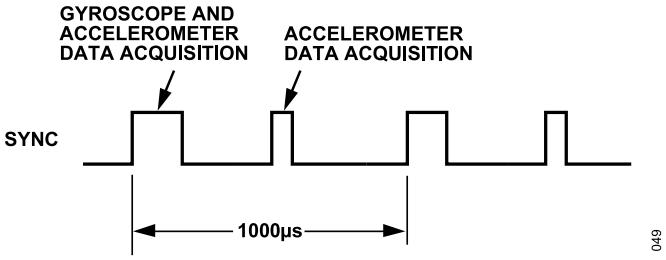

Figure 30. Sync Output Signal, Register MSC_CTRL, Bits[3:2] = 11

BARTLETT WINDOW FILTER

The Bartlett window filter is a finite impulse response (FIR) filter (see Figure 31) that contains two averaging filter stages in a cascade configuration. The FILT_CTRL register (see Table 103) provides the configuration controls for this filter.

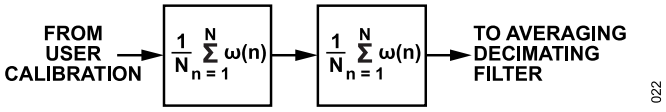

Figure 31. Bartlett Window FIR Filter Signal Path

CALIBRATION

The inertial sensor calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 32).

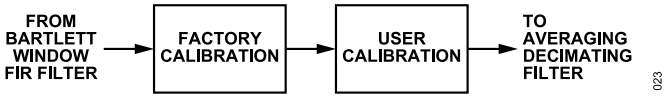

Figure 32. Inertial Sensor Calibration Processing

The factory calibration of the gyroscope applies the following correction formulas to the data of each gyroscope:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \left(\begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} \right) + \begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{21} & l_{22} & l_{23} \\ l_{31} & l_{32} & l_{33} \end{bmatrix} + \begin{bmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{bmatrix}$$

where:

ω_{XC}, ω_{YC}, and ω_{ZC} are the gyroscope outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
ω_X, ω_Y, and ω_Z are the gyroscope outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.
l_{11}, l_{12}, l_{13}, l_{21}, l_{22}, l_{23}, l_{31}, l_{32}, and l_{33} provide linear acceleration correction.
a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).

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All of the correction factors in this relationship come from direct observation of the response of each gyroscope at multiple temperatures over the calibration temperature range (−40°C ≤ T_A ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation or configuration.

The MSC_CTRL register, Bit 7 (see Table 107) provides the only user-configurable option for the factory calibration of the gyroscopes: an on/off control for the linear acceleration compensation. See Figure 56 for more details on the user calibration options available for the gyroscopes.

The factory calibration of the accelerometer applies the following correction formulas to the data of each accelerometer:

$$\begin{bmatrix} a_{XC} \\ a_{YC} \\ a_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \left[\begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} \right] + \begin{bmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{bmatrix} + \begin{bmatrix} \omega^2_{XC} \\ \omega^2_{YC} \\ \omega^2_{ZC} \end{bmatrix}$$

where:

a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
a_X, a_Y, and a_Z are the accelerometer outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.
p_{12}, p_{13}, p_{21}, p_{23}, p_{31} and p_{32} provide a point of percussion alignment correction (see Figure 59).
ω^2_{XC}, ω^2_{YC}, and ω^2_{ZC} are the square of the gyroscope outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each accelerometer at multiple temperatures, over the calibration temperature range (−40°C ≤ T_A ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation or configuration. The MSC_CTRL register, Bit 6 (see Table 107) provides the only user configuration option for the factory calibration of the accelerometers: an on/off control for the point of percussion, alignment function. See Figure 57 for more details on the user calibration options available for the accelerometers.

DECIMATION FILTER

The second digital filter averages multiple samples together to produce each register update. The number of samples in the average is equal to the reduction in the update rate (f_{ODR}) for the output data registers (see Figure 33). The DEC_RATE register (see Table 111) provides the configuration controls for this filter.

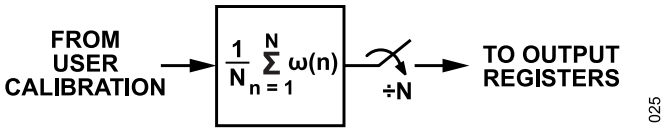

Figure 33. Decimating Filter Diagram

REGISTER STRUCTURE

All communication between the ADIS16501 and an external processor involves either reading the contents of an output register or writing configuration/command information to a control register. The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, and diagnostic options. Each user accessible register has two bytes (upper and lower), each of which has its own unique address. See Table 10 for a detailed list of all user registers, along with their addresses.

SPI

The SPI provides access to the user registers (see Table 10). Figure 34 shows the most common connections between the ADIS16501 and an SPI main device, which is often an embedded processor that has an SPI-compatible interface. In this example, the SPI main uses an interrupt service routine to collect data every time the data ready (DR) signal pulses.

Additional information on the SPI can be found in the Applications Information section.

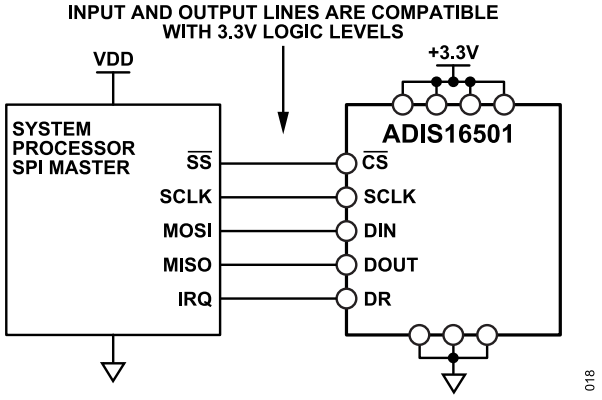

Figure 34. Electrical Connection Diagram

33 Ω termination resistors are recommended to improve SPI overshoot during communication. The $\overline{CS}$, SCLK, and MOSI resistors must be placed close to the system processor SPI main. The MISO and IRQ resistors must be placed close to the ADIS16501.

Table 6 provides an example list of pin names for the SPI port in an embedded processor.

Table 6. Generic SPI Main Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Subordinate select

THEORY OF OPERATION

Table 6. Generic SPI Main Pin Names and Functions (Continued)

Mnemonic	Function
SCLK	Serial clock
MOSI	Main output, subordinate input
MISO	Main input, subordinate output
IRQ	Interrupt request

Embedded processors typically configure their serial ports for communicating with SPI subordinate devices such as the ADIS16501 by using control registers on the processor itself. Table 7 lists the SPI protocol settings for the ADIS16501.

Table 7. Generic Main Processor SPI Settings

Processor Setting	Description
Main	ADIS16501 operates as subordinate
SCLK ≤ 10 MHz[1]	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 40 for coding
16-Bit Mode	Shift register and data length

[1] A burst mode read requires this value to be ≤1.1 MHz (see Table 2 for more information).

DATA READY (DR)

The factory default configuration provides users with a DR signal on the DR pin (see Table 5), which pulses when the output data registers are updating. Connect the DR pin to an input pin on the embedded processor and configure this pin to trigger data collection on the second edge of the pulse on the DR pin. The MSC_CTRL register, Bit 0 (see Table 107) controls the polarity of this signal. Figure 35 shows a DR signal with Register MSC_CTRL, Bit 0 = 1, meaning that data collection must start on the rising edges of the DR pulses.

Figure 35. Data Ready when Register MSC_CTRL, Bit 0 = 1 (Default)

During the start-up and reset recovery processes, the DR signal can exhibit some transient behavior before data production begins. Figure 36 shows an example of the DR behavior during startup, and Figure 37 and Figure 38 provide examples of the DR behavior during recovery from reset commands.

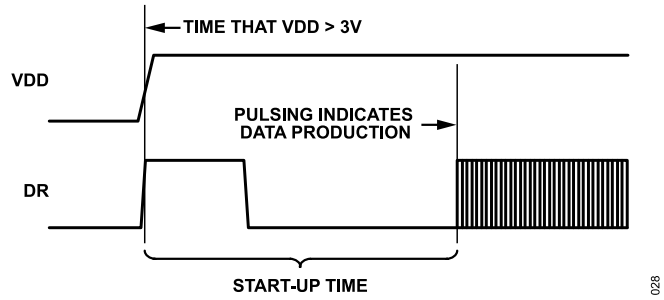

Figure 36. Data Ready Response During Startup

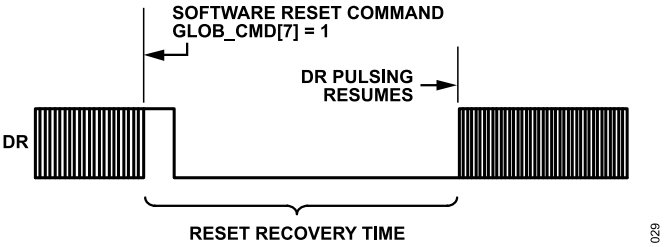

Figure 37. Data Ready Response During Reset Recovery (Register GLOB_CMD, Bit 7 = 1)

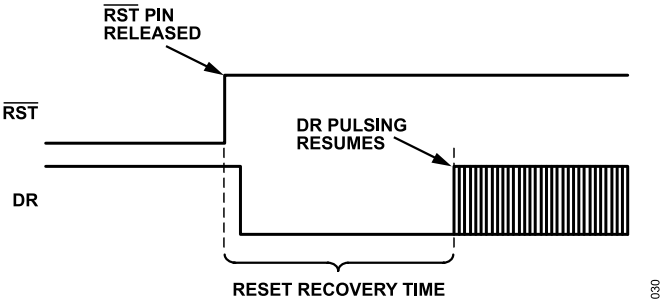

Figure 38. Data Ready Response During Reset ($\overline{RST}$ = 0) Recovery

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 40) for a read request on the SPI has three parts: the read bit ($\overline{R}$/W = 0), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 39 shows an example that includes two register reads in succession. This example starts with DIN = 0x0C00 to request the contents of the Z_GYRO_LOW register and follows with 0x0E00 to request the contents of the Z_GYRO_OUT register. The sequence in Figure 39 also shows full duplex mode of operation, which means that the ADIS16501 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

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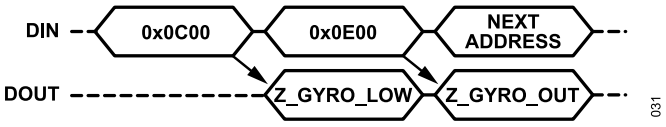
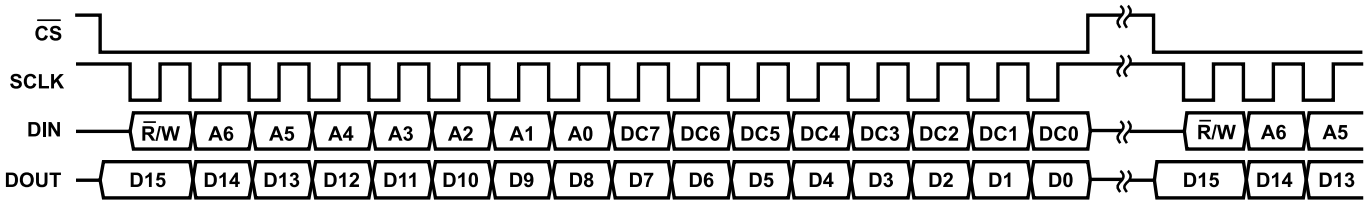


Figure 39. SPI Read Example

Figure 41 provides an example of the four SPI signals when reading the PROD_ID register (see Table 120) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI setup and communications because the signals are the same for each 16-bit sequence, except during the first cycle.



NOTES
1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH R/W = 0.
2. WHEN CS IS HIGH, DOUT IS IN A THREE-STATE, HIGH IMPEDANCE MODE, WHICH ALLOWS MULTIFUNCTIONAL USE OF THE LINE FOR OTHER DEVICES.

Figure 40. SPI Communication Bit Sequence

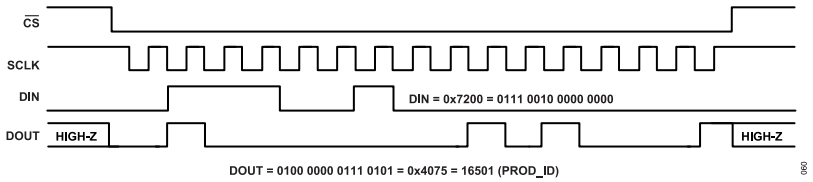


Figure 41. SPI Signal Pattern, Repeating Read of the PROD_ID Register

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BURST READ FUNCTION

The burst read function provides a way to read a batch of output data registers, using a continuous stream of bits, at a rate of up to 1 MHz (SCLK). This method does not require a stall time between each 16-bit segment (see Figure 3). As shown in Figure 42, start this mode by setting DIN = 0x6800, and then read each of the registers in the sequence out of DOUT while keeping $\overline{CS}$ low for the entire data transfer sequence. However, keeping the $\overline{CS}$ pin low after a burst transfer is complete can delay the next data ready pulse, and potentially interfere with the processing of the next IMU sample.

The three options for burst mode include: scaled sync mode on or off, BURST32 enabled and disabled, and BURST_SEL = 0 or BURSET_SEL = 1. This results in eight possible burst data formats.

Scaled Sync Mode Enabled vs. Disabled

The only differences in the burst data format between these two modes are the final two bytes in a burst. In scaled sync mode, the final two bytes are the values of the TIME_STAMP registers. When scaled sync mode is disabled, the final two bytes are the values in the DATA_CNTR registers. As always, Bits[15:8] appear before Bits[7:0] in both modes.

For the rest of the Burst Read Function section, it is assumed that scaled sync mode is disabled.

16-Bit Burst Mode with BURST_SEL = 0

In 16-bit burst mode with BURST_SEL = 0, a burst contains calibrated gyroscope and accelerometer data in 16-bit format. This mode is particularly appropriate for cases where there is no decimation or filtering. In this mode, with this particular setting, the sample rate is high (~2 kSPS) and the lower 16 bits are not used except in cases where the user is running these actions of averaging/filtering.

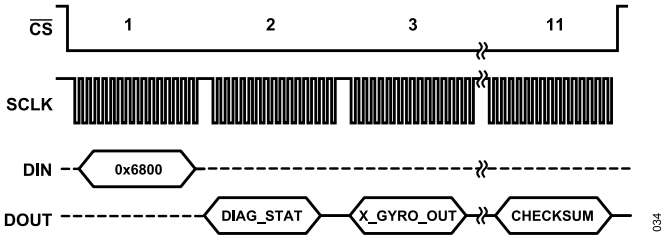

Figure 42. Burst Read Sequence with BURST_SEL = 0

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_GYRO_OUT, Y_GYRO_OUT, Z_GYRO_OUT, X_ACCL_OUT, Y_ACCL_OUT, Z_ACCL_OUT, TEMP_OUT, DATA_ CNTR, and the checksum value.

In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_GYRO_OUT, Bits[15:8] + X_GYRO_OUT, Bits[7:0] + Y_GYRO_OUT, Bits[15:8] + Y_GYRO_OUT, Bits[7:0] + Z_GYRO_OUT, Bits[15:8] + Z_GYRO_OUT, Bits[7:0] + X_ACCL_OUT, Bits[15:8] + X_ACCL_OUT, Bits[7:0] + Y_ACCL_OUT, Bits[15:8] + Y_ACCL_OUT, Bits[7:0] + Z_ACCL_OUT, Bits[15:8] + Z_ACCL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

16-Bit Burst Mode with BURST_SEL = 1

In 16-bit burst mode with BURST_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 16-bit format. This mode is particularly appropriate for cases where there is no decimation or filtering. In this mode, with this particular setting, the sample rate is high (~2 kSPS) and the lower 16 bits are not used.

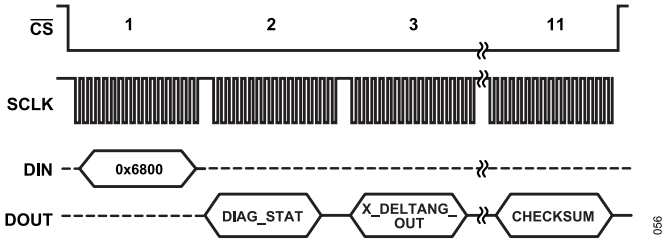

Figure 43. Burst Read Sequence with BURST_SEL = 1

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_DELTANG_OUT, Y_DELTANG_OUT, Z_DELTANG_OUT, X_DELTVEL_OUT, Y_DELTVEL_OUT, Z_DELTVEL_OUT, TEMP_OUT, DATA_ CNTR, and the checksum value.

In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_DELTANG_OUT, Bits[15:8] + X_DELTANG_OUT, Bits[7:0] + Y_DELTANG_OUT, Bits[15:8] + Y_DELTANG_OUT, Bits[7:0] + Z_DELTANG_OUT, Bits[15:8] + Z_DELTANG_OUT, Bits[7:0] + X_DELTVEL_OUT, Bits[15:8] + X_DELTVEL_OUT, Bits[7:0] + Y_DELTVEL_OUT, Bits[15:8] + Y_DELTVEL_OUT, Bits[7:0] + Z_DELTVEL_OUT, Bits[15:8] + Z_DELTVEL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

32-Bit Burst Mode with BURST_SEL = 0

In 32-bit burst mode with BURST_SEL = 0, a burst contains calibrated gyroscope and accelerometer data in 32-bit format. This

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mode is appropriate for cases where there is averaging (decimation) and/or low-pass filtering of the data.

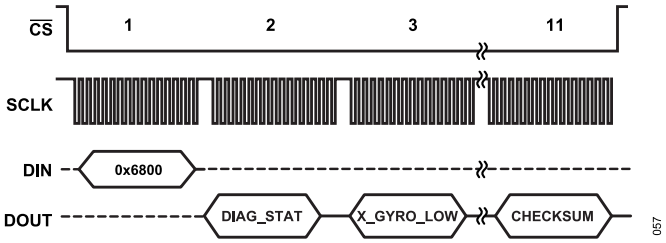

Figure 44. Burst Read Sequence with BURST_SEL = 0

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_GYRO_LOW, X_GYRO_OUT, Y_GYRO_LOW, Y_GYRO_OUT, Z_GYRO_LOW, Z_GYRO_OUT, X_ACCL_LOW, X_ACCL_OUT, Y_ACCL_LOW, Y_ACCL_OUT, Z_ACCL_LOW, Z_ACCL_OUT, TEMP_OUT, DATA_CNTR, and the checksum value. In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_GYRO_LOW, Bits[15:8] + X_GYRO_LOW, Bits[7:0] + X_GYRO_OUT, Bits[15:8] + X_GYRO_OUT, Bits[7:0] + Y_GYRO_LOW, Bits[15:8] + Y_GYRO_LOW, Bits[7:0] + Y_GYRO_OUT, Bits[15:8] + Y_GYRO_OUT, Bits[7:0] + Z_GYRO_LOW, Bits[15:8] + Z_GYRO_LOW, Bits[7:0] + Z_GYRO_OUT, Bits[15:8] + Z_GYRO_OUT, Bits[7:0] + X_ACCL_LOW, Bits[15:8] + X_ACCL_LOW, Bits[7:0] + X_ACCL_OUT, Bits[15:8] + X_ACCL_OUT, Bits[7:0] + Y_ACCL_LOW, Bits[15:8] + Y_ACCL_LOW, Bits[7:0] + Y_ACCL_OUT, Bits[15:8] + Y_ACCL_OUT, Bits[7:0] + Z_ACCL_LOW, Bits[15:8] + Z_ACCL_LOW, Bits[7:0] + Z_ACCL_OUT, Bits[15:8] + Z_ACCL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

32-Bit Burst Mode with BURST_SEL = 1

In 32-bit burst mode with BURST_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 32-bit format. This mode is appropriate for cases where there is averaging (decimation) and/or low-pass filtering of the data.

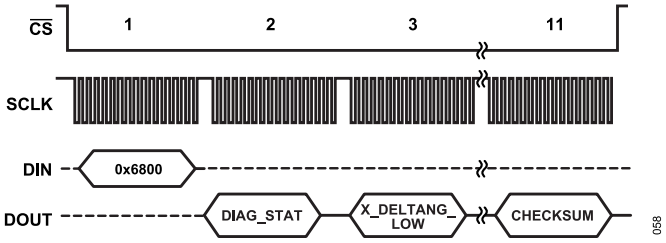

Figure 45. Burst Read Sequence with BURST_SEL = 1

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_DELTANG_LOW, X_DELTANG_OUT, Y_DELTANG_LOW, Y_DELTANG_OUT, Z_DELTANG_LOW, Z_DELTANG_OUT, X_DELTVEL_LOW, X_DELTVEL_OUT, Y_DELTVEL_LOW, Y_DELTVEL_OUT, Z_DELTVEL_LOW, Z_DELTVEL_OUT, TEMP_OUT, DATA_CNTR, and the checksum value. In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_DELTANG_LOW, Bits[15:8] + X_DELTANG_LOW, Bits[7:0] + X_DELTANG_OUT, Bits[15:8] + X_DELTANG_OUT, Bits[7:0] + Y_DELTANG_LOW, Bits[15:8] + Y_DELTANG_LOW, Bits[7:0] + Y_DELTANG_OUT, Bits[15:8] + Y_DELTANG_OUT, Bits[7:0] + Z_DELTANG_LOW, Bits[15:8] + Z_DELTANG_LOW, Bits[7:0] + Z_DELTANG_OUT, Bits[15:8] + Z_DELTANG_OUT, Bits[7:0] + X_DELTVEL_LOW, Bits[15:8] + X_DELTVEL_LOW, Bits[7:0] + X_DELTVEL_OUT, Bits[15:8] + X_DELTVEL_OUT, Bits[7:0] + Y_DELTVEL_LOW, Bits[15:8] + Y_DELTVEL_LOW, Bits[7:0] + Y_DELTVEL_OUT, Bits[15:8] + Y_DELTVEL_OUT, Bits[7:0] + Z_DELTVEL_LOW, Bits[15:8] + Z_DELTVEL_LOW, Bits[7:0] + Z_DELTVEL_OUT, Bits[15:8] + Z_DELTVEL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

LATENCY

Table 8 contains the group delay for each inertial sensor when the ADIS16501 is operating with the factory default settings for the FILT_CTRL (see Table 102) and DEC_RATE (see Table 110) registers.

Table 8. Group Delay with No Filtering, Wide Bandwidth Option, MSC_CTRL, Bit 4 = 0

Inertial Sensor	Group Delay (ms)[1]
Accelerometer	1.37
Gyroscope (X-Axis)	1.56
Gyroscope (Y-Axis)	1.56
Gyroscope (Z-Axis)	1.34

[1] In this context, latency represents the time between the motion (linear acceleration and/or angular rate of rotation) and the time that the representative data is available in the output data register.

Table 9. Group Delay with No Filtering, 370 Hz Bandwidth, MSC_CTRL, Bit 4 = 1

Inertial Sensor	Group Delay (ms)[1]
Accelerometer	2.00
Gyroscope (X-Axis)	1.80
Gyroscope (Y-Axis)	1.80

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Table 9. Group Delay with No Filtering, 370 Hz Bandwidth, MSC_CTRL, Bit 4 = 1 (Continued)

Inertial Sensor	Group Delay (ms)[1]
Gyroscope (Z-Axis)	1.54

[1] In this context, latency represents the time between the motion (linear acceleration and/or angular rate of rotation) and the time that the representative data is available in the output data register.

When the FILT_CTRL register is not equal to 0, the group delay contribution of the Bartlett window filter (in terms of sample cycles) is equal to N (see Table 103). When the DEC_RATE register is not equal to 0, the group delay contribution of the decimation filter (in terms of sample cycles) is equal D + 1, divided by 2 (see Table 111).

Data Acquisition

The total latency is equal to the sum of the group delay and the data acquisition time, which represents the time it takes the system processor to read the data from the output data registers of the ADIS16501. For example, when using the burst read function, with an SCLK rate of 1 MHz, the data acquisition time is equal to 176 µs (11 segments × 16 SCLKs/segment × 1 µs/SCLK).

DEVICE CONFIGURATION

Each configuration register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte. Each byte has its own unique address in the user register map (see Table 10). Updating the contents of a register requires writing to both of its bytes in the following sequence: low byte first, high byte second. There are three parts to coding an SPI command (see Figure 40) that write a new byte of data to a register: the write bit ($\overline{R}/W$ = 1), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 46 shows a coding example for writing 0x0004 to the FILT_CTRL register (see Table 103). In Figure 46, the 0xDC04 command writes 0x04 to Address 0x5C (lower byte), and the 0xDD00 command writes 0x00 to Address 0x5D (upper byte).

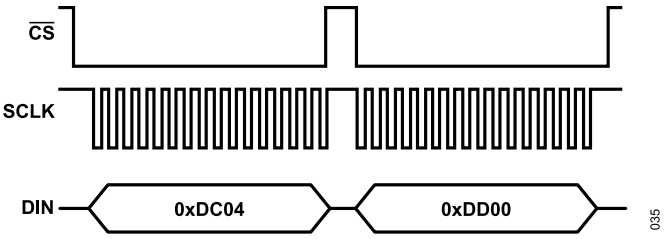

Figure 46. SPI Sequence for Writing 0x0004 to FILT_CTRL

MEMORY STRUCTURE

Figure 47 provides a functional diagram for the memory structure of the ADIS16501. The flash memory bank contains the operational code, unit specific calibration coefficients, and user configuration settings. During initialization (power application or reset recover), this information loads from the flash memory into the static random access memory (SRAM), which supports all normal operation including register access through the SPI port. Writing to a configuration register using the SPI updates the SRAM location of the register but does not automatically update its settings in the flash memory bank. The manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 113) provides a convenient method for saving all of these settings to the flash memory bank at one time. A yes in the flash backup column of Table 10 identifies the registers that have storage support in the flash memory bank.

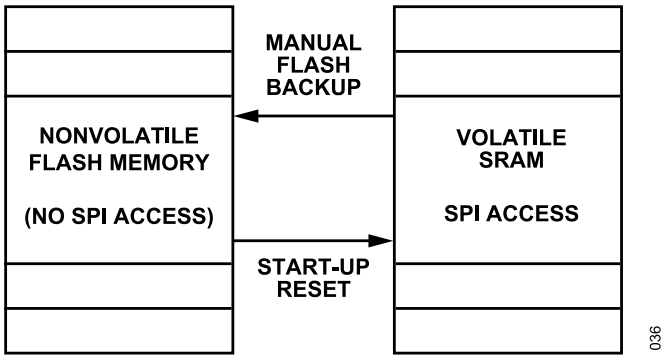

Figure 47. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	Address	Default	Register Description
Reserved	N/A	N/A	0x00, 0x01	N/A	Reserved
DIAG_STAT	R	No	0x02, 0x03	0x0000	Output, system error flags
X_GYRO_LOW	R	No	0x04, 0x05	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x06, 0x07	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x08, 0x09	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x0A, 0x0B	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x0C, 0x0D	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x0E, 0x0F	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x10, 0x11	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x12, 0x13	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x14, 0x15	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x16, 0x17	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x18, 0x19	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x1A, 0x1B	N/A	Output, z-axis accelerometer, high word
TEMP_OUT	R	No	0x1C, 0x1D	N/A	Output, temperature
TIME_STAMP	R	No	0x1E, 0x1F	N/A	Output, time stamp
Reserved	N/A	N/A	0x20, 0x21	N/A	Reserved
DATA_CNTR	R	No	0x22, 0x23	N/A	New data counter
X_DELTANG_LOW	R	No	0x24, 0x25	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x26, 0x27	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x28, 0x29	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x2A, 0x2B	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x2C, 0x2D	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x2E, 0x2F	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x30, 0x31	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x32, 0x33	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x34, 0x35	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x36, 0x37	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x38, 0x39	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x3A, 0x3B	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x3C to 0x3F	N/A	Reserved
XG_BIAS_LOW	R/W	Yes	0x40, 0x41	0x0000	Calibration, offset, gyroscope, x-axis, low word
XG_BIAS_HIGH	R/W	Yes	0x42, 0x43	0x0000	Calibration, offset, gyroscope, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x44, 0x45	0x0000	Calibration, offset, gyroscope, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x46, 0x47	0x0000	Calibration, offset, gyroscope, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x48, 0x49	0x0000	Calibration, offset, gyroscope, z-axis, low word
ZG_BIAS_HIGH	R/W	Yes	0x4A, 0x4B	0x0000	Calibration, offset, gyroscope, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x4C, 0x4D	0x0000	Calibration, offset, accelerometer, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x4E, 0x4F	0x0000	Calibration, offset, accelerometer, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x50, 0x51	0x0000	Calibration, offset, accelerometer, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x52, 0x53	0x0000	Calibration, offset, accelerometer, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x54, 0x55	0x0000	Calibration, offset, accelerometer, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x56, 0x57	0x0000	Calibration, offset, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x58 to 0x5B	N/A	Reserved

USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable) (Continued)

Name	R/W	Flash Backup	Address	Default	Register Description
FILT_CTRL	R/W	Yes	0x5C, 0x5D	0x0000	Control, Bartlett window FIR filter
RANG_MDL	R	No	0x5E, 0x5F	N/A[1]	Measurement range (model specific) identifier
MSC_CTRL	R/W	Yes	0x60, 0x61	0x00C1	Control, input/output and other miscellaneous options
UP_SCALE	R/W	Yes	0x62, 0x63	0x07D0	Control, scale factor for input clock, scaled sync mode
DEC_RATE	R/W	Yes	0x64, 0x65	0x0000	Control, decimation filter (output data rate)
Reserved	N/A	N/A	0x66, 0x67	N/A	Reserved
GLOB_CMD	W	No	0x68, 0x69	N/A	Control, global commands
Reserved	N/A	N/A	0x6A to 0x6B	N/A	Reserved
FIRM_REV	R	No	0x6C, 0x6D	0x0200	Identification, firmware revision
FIRM_DM	R	No	0x6E, 0x6F	0x0503	Identification, date code, day and month
FIRM_Y	R	No	0x70, 0x71	0x2021	Identification, date code, year
PROD_ID	R	No	0x72, 0x73	0x5FB5	Identification, device number (0x5FB5 = 24,501 decimal)
SERIAL_NUM	R	No	0x74, 0x75	N/A	Identification, serial number
USER_SCR_1	R/W	Yes	0x76, 0x77	N/A	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x78, 0x79	N/A	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x7A, 0x7B	N/A	User Scratch Register 3
FLSHCNT_LOW	R	No	0x7C, 0x7D	N/A	Output, flash memory write cycle counter, lower word
FLSHCNT_HIGH	R	No	0x7E, 0x7F	N/A	Output, flash memory write cycle counter, upper word

[1] See Table 104 for the model specific default value for this register.

USER REGISTER DEFINITIONS

STATUS/ERROR FLAG INDICATORS (DIAG_STAT)

Table 11. DIAG_STAT Register Definition

Addresses	Default	Access	Flash Backup
0x02, 0x03	0x0000	R	No

Table 12. DIAG_STAT Bit Assignments

Bits	Description
[15:8]	Reserved
7	Clock error. A 1 indicates that the internal data sampling clock (f_{SM}, see Figure 29) does not synchronize with the external clock, which only applies when using scaled sync mode (Register MSC_CTRL, Bits[3:2] = 10, see Table 107). When this error occurs, adjust the frequency of the clock signal on the SYNC pin to operate within the appropriate range.
6	Memory failure. A 1 indicates a failure in the flash memory test (Register GLOB_CMD, Bit 4, see Table 113), which involves a comparison between a cyclic redundancy check (CRC) calculation of the present flash memory and a CRC calculation from the same memory locations at the time of initial programming (during the production process). If this error occurs, repeat the same test. If this error persists, replace the ADIS16501.
5	Sensor failure. A 1 indicates failure of at least one sensor, at the conclusion of the self test (Register GLOB_CMD, Bit 2, see Table 113). If this error occurs, repeat the same test. If this error persists, replace the ADIS16501. Motion during the execution of this test can cause a false failure.
4	Standby mode. A 1 indicates that the voltage across VDD and GND is <2.8 V, which causes data processing to stop. When VDD ≥ 2.8 V for 250 ms, the ADIS16501 reinitializes itself and starts producing data again.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. When this error occurs, repeat the previous communication sequence. Persistence in this error can indicate a weakness in the SPI service that the ADIS16501 is receiving from the system it is supporting.
2	Flash memory update failure. A 1 indicates that the most recent flash memory update (Register GLOB_CMD, Bit 3, see Table 113) failed. If this error occurs, ensure that VDD ≥ 3 V and repeat the update attempt. If this error persists, replace the ADIS16501.
1	Datapath overrun. A 1 indicates that one of the data paths experienced an overrun condition. If this error occurs, initiate a reset using the $\overline{RST}$ pin (see Table 5, Pin F3) or Register GLOB_CMD, Bit 7 (see Table 113).
0	Reserved

The DIAG_STAT register (see Table 11 and Table 12) provides error flags for monitoring the integrity and operation of the ADIS16501. Reading this register resets its bits to 0. The error flags in DIAG_STAT are sticky, meaning that when they raise to a 1, they remain there until a read request clears them. If an error condition persists, the flag (bit) automatically returns to an alarm value of 1.

GYROSCOPE DATA

The gyroscopes in the ADIS16501 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 48 shows the orientation of each gyroscope axis along with the direction of rotation that produces a positive response in each of their measurements.

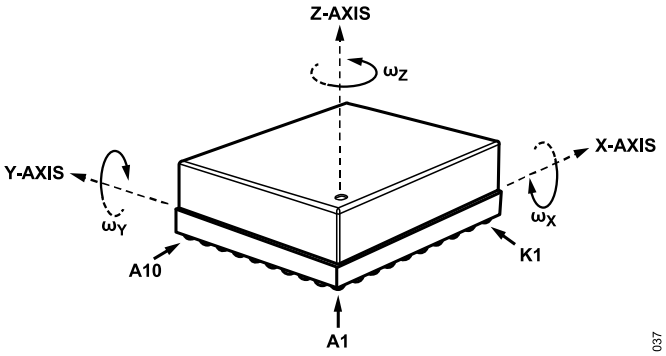

Figure 48. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 49 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and z-axes.

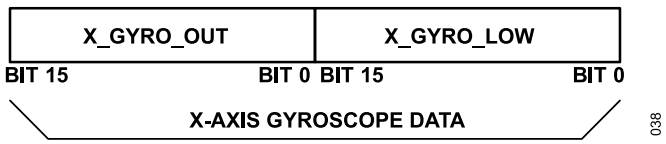

Figure 49. Gyroscope Output Data Structure

Gyroscope Measurement Range/Scale Factor

Table 13 provides the range and scale factor for the angular rate (gyroscope) measurements for the ADIS16501.

Table 13. Gyroscope Measurement Range and Scale Factors

Model	Range, $\pm\omega_{MAX}$ (°/sec)	Scale Factor, K_G (°/sec/LSB)
ADIS16501	±500	0.025

Gyroscope Data Formatting

Table 14 and Table 15 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats.

Table 14. 16-Bit Gyroscope Data Format Examples

Rotation Rate	Decimal	Hex	Binary
$+\omega_{MAX}$	+20,000	0x4E20	0100 1110 0010 0000
$+2\ K_G$	+2	0x0002	0000 0000 0000 0010
$+K_G$	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
$-K_G$	−1	0xFFFF	1111 1111 1111 1111

USER REGISTER DEFINITIONS

Table 14. 16-Bit Gyroscope Data Format Examples (Continued)

Rotation Rate	Decimal	Hex	Binary
$-2\ K_G$	−2	0xFFFE	1111 1111 1111 1110
$-\omega_{MAX}$	−20,000	0xB1E0	1011 0001 1110 0000

Table 15. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex
$+\omega_{MAX}$	+1,310,720,000	0x4E200000
$+K_G/2^{15}$	+2	0x00000002
$+K_G/2^{16}$	+1	0x00000001
0	0	0x00000000
$-K_G/2^{16}$	−1	0xFFFFFFFF
$-K_G/2^{15}$	−2	0xFFFFFFFE
$-\omega_{MAX}$	−1,310,720,000	0xB1E00000

X-Axis Gyroscope (X_GYRO_LOW and X_GYRO_OUT)

Table 16. X_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x04, 0x05	Not applicable	R	No

Table 17. X_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data, additional resolution bits

Table 18. X_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x06, 0x07	Not applicable	R	No

Table 19. X_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data, high word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 13 for K_G)

The X_GYRO_LOW (see Table 16 and Table 17) and X_GYRO_OUT (see Table 18 and Table 19) registers contain the gyroscope data for the x-axis.

Y-Axis Gyroscope (Y_GYRO_LOW and Y_GYRO_OUT)

Table 20. Y_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x08, 0x09	Not applicable	R	No

Table 21. Y_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data, additional resolution bits

Table 22. Y_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x0A, 0x0B	Not applicable	R	No

Table 23. Y_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data, high word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 13 for K_G)

The Y_GYRO_LOW (see Table 20 and Table 21) and Y_GYRO_OUT (see Table 22 and Table 23) registers contain the gyroscope data for the y-axis.

Z-Axis Gyroscope (Z_GYRO_LOW and Z_GYRO_OUT)

Table 24. Z_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x0C, 0x0D	Not applicable	R	No

Table 25. Z_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data, additional resolution bits

Table 26. Z_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x0E, 0x0F	Not applicable	R	No

Table 27. Z_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data, high word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 13 for K_G)

The Z_GYRO_LOW (see Table 24 and Table 25) and Z_GYRO_OUT (see Table 26 and Table 27) registers contain the gyroscope data for the z-axis.

USER REGISTER DEFINITIONS

ACCELERATION DATA

The accelerometers in the ADIS16501 measure both dynamic and static (response to gravity) acceleration along the same three orthogonal axes that define the axes of rotation for the gyroscopes (x, y, and z). Figure 50 shows the orientation of each accelerometer axis along with the direction of acceleration that produces a positive response in each of their measurements.

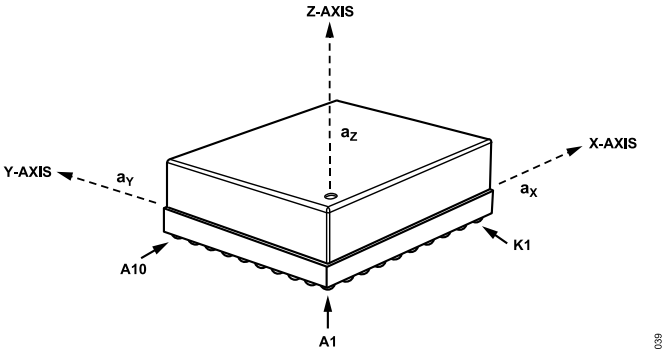

Figure 50. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 51 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes.

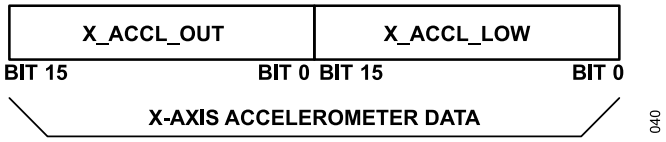

Figure 51. Accelerometer Output Data Structure

Accelerometer Resolution

Table 28 and Table 29 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 28. 16-Bit Accelerometer Data Format Examples

Acceleration	Dec	Hex	Binary
+14 *g*	+11,200	0x2BC0	0010 1011 1100 0000
+1 *g*	+800	0x0320	0000 0011 0010 0000
+1.25 m*g*	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−1.25 m*g*	−1	0xFFFF	1111 1111 1111 1111
−1 *g*	−800	0xFCE0	1111 1100 1110 0000
−14 *g*	−11,200	0xD440	1101 0100 0100 0000

Table 29. 32-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex
+14 *g*	+734,003,200	0x2BC00000
+1 *g*	+52,428,800	0x03200000

Table 29. 32-Bit Accelerometer Data Format Examples (Continued)

Acceleration	Decimal	Hex
+19.1 n*g*	+1	0x00000001
0	0	0x00000000
−19.1 n*g*	−1	0xFFFFFFFF
−1 *g*	−52,428,800	0xFCE00000
−14 *g*	−734,003,200	0xD4400000

X-Axis Accelerometer (X_ACCL_LOW and X_ACCL_OUT)

Table 30. X_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x10, 0x11	Not applicable	R	No

Table 31. X_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data, additional resolution bits

Table 32. X_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x12, 0x13	Not applicable	R	No

Table 33. X_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data, high word, twos complement, ±14 *g* range, 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

The X_ACCL_LOW (see Table 30 and Table 31) and X_ACCL_OUT (see Table 32 and Table 33) registers contain the accelerometer data for the x-axis.

Y-Axis Accelerometer (Y_ACCL_LOW and Y_ACCL_OUT)

Table 34. Y_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x14, 0x15	Not applicable	R	No

Table 35. Y_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data, additional resolution bits

Table 36. Y_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x16, 0x17	Not applicable	R	No

Table 37. Y_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data, high word, twos complement, ±14 *g* range, 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

USER REGISTER DEFINITIONS

The Y_ACCL_LOW (see Table 34 and Table 35) and Y_ACCL_OUT (see Table 36 and Table 37) registers contain the accelerometer data for the y-axis.

Z-Axis Accelerometer (Z_ACCL_LOW and Z_ACCL_OUT)

Table 38. Z_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x18, 0x19	Not applicable	R	No

Table 39. Z_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, additional resolution bits

Table 40. Z_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x1A, 0x1B	Not applicable	R	No

Table 41. Z_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, high word, twos complement, ±14 *g* range, 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

The Z_ACCL_LOW (see Table 38 and Table 39) and Z_ACCL_OUT (see Table 40 and Table 41) registers contain the accelerometer data for the z-axis.

INTERNAL TEMPERATURE (TEMP_OUT)

Table 42. TEMP_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x1C, 0x1D	Not applicable	R	No

Table 43. TEMP_OUT Bit Definitions

Bits	Description
[15:0]	Temperature data, twos complement, 1 LSB = 0.1°C, 0°C = 0x0000

The TEMP_OUT register (see Table 42 and Table 43) provides a coarse measurement of the temperature inside of the ADIS16501. This data is most useful for monitoring relative changes in the thermal environment.

Table 44. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+105	+1050	0x041A	0000 0100 0001 1010
+25	+250	0x00FA	0000 0000 1111 1010
+0.2	+2	0x0002	0000 0000 0000 0010
+0.1	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.1	−1	0xFFFF	1111 1111 1111 1111
−0.2	−2	0xFFFE	1111 1111 1111 1110
−40	−400	0xFE70	1111 1110 0111 0000

TIME STAMP (TIME_STAMP)

Table 45. TIME_STAMP Register Definition

Addresses	Default	Access	Flash Backup
0x1E, 0x1F	Not applicable	R	No

Table 46. TIME_STAMP Bit Definitions

Bits	Description
[15:0]	Time from the last pulse on the SYNC pin, offset binary format, 1 LSB = 49.02 µs

The TIME_STAMP register (see Table 45 and Table 46) works with scaled sync mode (Register MSC_CTRL, Bits[3:2] = 10, see Table 107). The 16-bit number in TIME_ STAMP contains the time associated with the last sample in each data update relative to the most recent edge of the clock signal in the SYNC pin. For example, when the value in the UP_SCALE register (see Table 109) represents a scale factor of 20, DEC_RATE = 0, and the external SYNC rate = 100 Hz, the following time stamp sequence results: 0 LSB, 10 LSB, 20 LSB, 30 LSB, 40 LSB, 50 LSB, 61 LSB, 71 LSB, … , 193 LSB for the 20th sample, which translates to 0 µs, 490 µs, … , 9460 µs, the time from the first SYNC edge.

DATA UPDATE COUNTER (DATA_CNTR)

Table 47. DATA_CNTR Register Definition

Addresses	Default	Access	Flash Backup
0x22, 0x23	Not applicable	R	No

Table 48. DATA_CNTR Bit Definitions

Bits	Description
[15:0]	Data update counter, offset binary format

When the ADIS16501 goes through its power-on sequence or when it recovers from a reset command, DATA_CNTR (see Table 47 and Table 48) starts with a value of 0x0000 and increments every time new data loads into the output registers. When the DATA_CNTR value reaches 0xFFFF, the next data update causes it to wrap back around to 0x0000 where it continues to increment every time new data loads into the output registers.

USER REGISTER DEFINITIONS

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16501 also provides delta angle measurements that represent a calculation of angular displacement between each sample update.

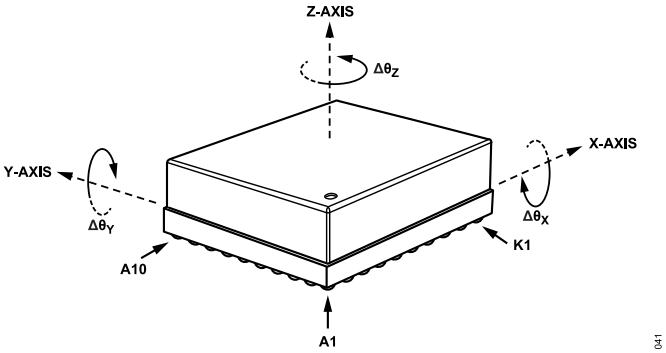

Figure 52. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(\omega_{X,nD+d} + \omega_{X,nD+d} - 1\right)$$

where:
D is the decimation rate (DEC_RATE + 1, see Table 111).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_X is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_S) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 110), divide each delta angle result (from the delta angle output registers) by the data ready frequency, and multiply it by 2000. Each axis of the delta angle measurements has two output data registers. Figure 53 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and z-axes.

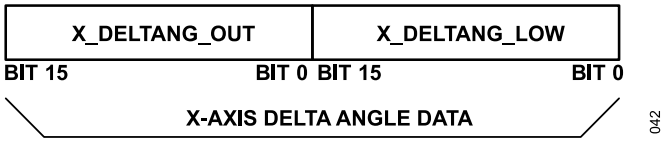

Figure 53. Delta Angle Output Data Structure

Delta Angle Measurement Range

Table 49 shows the measurement range and scale factor for the ADIS16501.

Table 49. Delta Angle Measurement Range and Scale Factor

Model	Measurement Range, $\pm\Delta\theta_{MAX}$ (°)
ADIS16501	±720

X-Axis Delta Angle (X_DELTANG_LOW and X_DELTANG_OUT)

Table 50. X_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x24, 0x25	Not applicable	R	No

Table 51. X_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data, low word

Table 52. X_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x26, 0x27	Not applicable	R	No

Table 53. X_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 49 for $\pm\Delta\theta_{MAX}$)

The X_DELTANG_LOW (see Table 50 and Table 51) and X_DELTANG_OUT (see Table 52 and Table 53) registers contain the delta angle data for the x-axis.

USER REGISTER DEFINITIONS

Y-Axis Delta Angle (Y_DELTANG_LOW and Y_DELTANG_OUT)

Table 54. Y_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x28, 0x29	Not applicable	R	No

Table 55. Y_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data, low word

Table 56. Y_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x2A, 0x2B	Not applicable	R	No

Table 57. Y_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 49 for $\pm\Delta\theta_{MAX}$)

The Y_DELTANG_LOW (see Table 54 and Table 55) and Y_DELTANG_OUT (see Table 56 and Table 57) registers contain the delta angle data for the y-axis.

Z-Axis Delta Angle (Z_DELTANG_LOW and Z_DELTANG_OUT)

Table 58. Z_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x2C, 0x2D	Not applicable	R	No

Table 59. Z_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data, low word

Table 60. Z_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x2E, 0x2F	Not applicable	R	No

Table 61. Z_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 49 for $\pm\Delta\theta_{MAX}$)

The Z_DELTANG_LOW (see Table 58 and Table 59) and Z_DELTANG_OUT (see Table 60 and Table 61) registers contain the delta angle data for the z-axis.

Delta Angle Resolution

Table 62 and Table 63 show various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 62. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
$\Delta\theta_{MAX} \times (2^{15}-1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta\theta_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta\theta_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta\theta_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta\theta_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta\theta_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 63. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
$+\Delta\theta_{MAX} \times (2^{31}-1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta\theta_{MAX}/2^{30}$	+2	0x00000002
$+\Delta\theta_{MAX}/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta\theta_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta\theta_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta\theta_{MAX}$	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16501 also provides delta velocity measurements that represent a calculation of linear velocity change between each sample update.

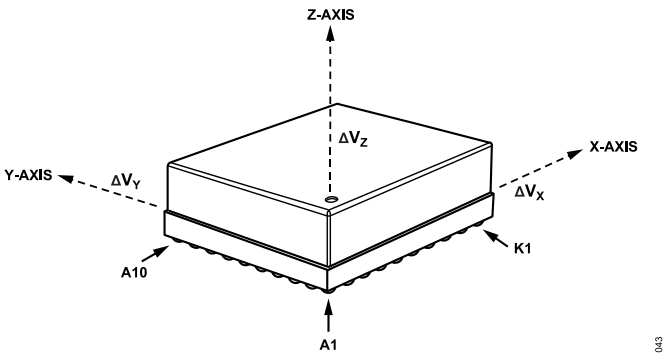

Figure 54. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(a_{X,nD+d} + a_{X,nD+d} - 1 \right)$$

USER REGISTER DEFINITIONS

where:
x is the x-axis.
n is the sample time, prior to the decimation filter.
D is the decimation rate (DEC_RATE + 1, see Table 111).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_X is the x-axis acceleration.

When using the internal sample clock, f_S is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_S) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 110), divide each delta angle result (from the delta angle output registers) by the data ready frequency, and multiply it by 2000. Each axis of the delta velocity measurements has two output data registers. Figure 55 shows how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y- and z-axes.

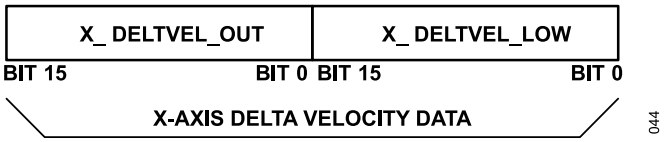

Figure 55. Delta Velocity Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW and X_DELTVEL_OUT)

Table 64. X_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x30, 0x31	Not applicable	R	No

Table 65. X_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data, additional resolution bits

Table 66. X_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x32, 0x33	Not applicable	R	No

Table 67. Table 67. X_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data, twos complement, ±125 m/sec range, 0 m/sec = 0x0000, 1 LSB = 125 m/sec ÷ 2^{15} = 0.003814697 m/sec

The X_DELTVEL_LOW (see Table 64 and Table 65) and X_DELTVEL_OUT (see Table 66 and Table 67) registers contain the delta velocity data for the x-axis.

Y-Axis Delta Velocity (Y_DELTVEL_LOW and Y_DELTVEL_OUT)

Table 68. Y_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x34, 0x35	Not applicable	R	No

Table 69. Y_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data, additional resolution bits

Table 70. Y_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x36, 0x37	Not applicable	R	No

Table 71. Y_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data, twos complement, ±125 m/sec range, 0 m/sec = 0x0000, 1 LSB = 125 m/sec ÷ 2^{15} = 0.003814697 m/sec

The Y_DELTVEL_LOW (see Table 68 and Table 69) and Y_DELTVEL_OUT (see Table 70 and Table 71) registers contain the delta velocity data for the y-axis.

Z-Axis Delta Velocity (Z_DELTVEL_LOW and Z_DELTVEL_OUT)

Table 72. Z_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x38, 0x39	Not applicable	R	No

Table 73. Z_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data, additional resolution bits

Table 74. Z_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x3A, 0x3B	Not applicable	R	No

Table 75. Z_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data, twos complement, ±125 m/sec range, 0 m/sec = 0x0000, 1 LSB = 125 m/sec ÷ 2^{15} = 0.003814697 m/sec

The Z_DELTVEL_LOW (see Table 72 and Table 73) and Z_DELTVEL_OUT (see Table 74 and Table 75) registers contain the delta velocity data for the z-axis.

USER REGISTER DEFINITIONS

Delta Velocity Resolution

Table 76 and Table 77 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 76. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
$+125 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1111 1111
$+125/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+125/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-125/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-125/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
−125	−32,768	0x8000	1000 0000 0000 0000

Table 77. 32-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex
$+125 \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+125/2^{30}$	+2	0x00000002
$+125/2^{31}$	+1	0x00000001
0	0	0x00000000
$-125/2^{31}$	−1	0xFFFFFFFF
$-125/2^{30}$	−2	0xFFFFFFFE
−125	+2,147,483,648	0x80000000

CALIBRATION

The signal chain of each inertial sensor (accelerometers and gyroscopes) includes the application of unique correction formulas, which are derived from extensive characterization of bias, sensitivity, alignment, response to linear acceleration (gyroscopes), and point of percussion (accelerometer location) over a temperature range of −40°C to +85°C, for each ADIS16501. These correction formulas are not accessible, but users do have the opportunity to adjust the bias for each sensor individually through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 2000 Hz when using the internal sample clock.

Calibration, Gyroscope Bias (XG_BIAS_LOW and XG_BIAS_HIGH)

Table 78. XG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x40, 0x41	0x0000	R/W	Yes

Table 79. XG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction, lower word

Table 80. XG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x42, 0x43	0x0000	R/W	Yes

Table 81. XG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction factor, upper word

The XG_BIAS_LOW (see Table 78 and Table 79) and XG_BIAS_HIGH (see Table 80 and Table 81) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The data format examples in Table 14 also apply to the XG_BIAS_HIGH register, and the data format examples in Table 15 apply to the 32-bit combination of the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 56 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

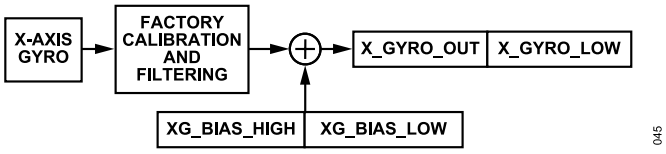

Figure 56. User Calibration Signal Path, Gyroscopes

Calibration, Gyroscope Bias (YG_BIAS_LOW and YG_BIAS_HIGH)

Table 82. YG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x44, 0x45	0x0000	R/W	Yes

Table 83. YG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, lower word

Table 84. YG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x46, 0x47	0x0000	R/W	Yes

Table 85. YG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction factor, upper word

The YG_BIAS_LOW (see Table 82 and Table 83) and YG_BIAS_HIGH (see Table 84 and Table 85) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The data format examples in Table 14 also apply to the YG_BIAS_HIGH register, and the data format examples in Table 15 apply to the 32-bit combination of the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 56).

USER REGISTER DEFINITIONS

Calibration, Gyroscope Bias (ZG_BIAS_LOW and ZG_BIAS_HIGH)

Table 86. ZG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x48, 0x49	0x0000	R/W	Yes

Table 87. ZG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, lower word

Table 88. ZG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x4A, 0x4B	0x0000	R/W	Yes

Table 89. ZG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction factor, upper word

The ZG_BIAS_LOW (see Table 86 and Table 87) and ZG_BIAS_HIGH (see Table 88 and Table 89) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The data format examples in Table 14 also apply to the ZG_BIAS_HIGH register, and the data format examples in Table 15 apply to the 32-bit combination of the ZG_BIAS_LOW and ZG_BIAS_HIGH registers.

These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 56).

Calibration, Accelerometer Bias (XA_BIAS_LOW and XA_BIAS_HIGH)

Table 90. XA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x4C, 0x4D	0x0000	R/W	Yes

Table 91. XA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, lower word

Table 92. XA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x4E, 0x4F	0x0000	R/W	Yes

Table 93. XA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, upper word

The XA_BIAS_LOW (see Table 90 and Table 91) and XA_BIAS_HIGH (see Table 92 and Table 93) registers combine to allow users to adjust the bias of the x-axis accelerometers. The data format examples in Table 28 also apply to the XA_BIAS_HIGH register, and the data format examples in Table 29 apply to the 32-bit combination of the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 57 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

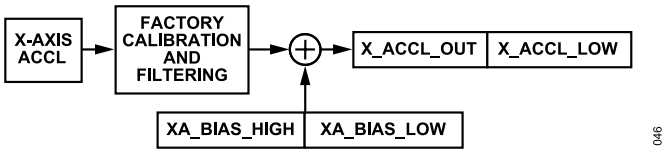

Figure 57. User Calibration Signal Path, Accelerometers

Calibration, Accelerometer Bias (YA_BIAS_LOW and YA_BIAS_HIGH)

Table 94. YA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x50, 0x51	0x0000	R/W	Yes

Table 95. YA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, lower word

Table 96. YA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x52, 0x53	0x0000	R/W	Yes

Table 97. YA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, upper word

The YA_BIAS_LOW (see Table 94 and Table 95) and YA_BIAS_HIGH (see Table 96 and Table 97) registers combine to allow users to adjust the bias of the y-axis accelerometers. The data format examples in Table 28 also apply to the YA_BIAS_HIGH register, and the data format examples in Table 29 apply to the 32-bit combination of the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 57).

Calibration, Accelerometer Bias (ZA_BIAS_LOW and ZA_BIAS_HIGH)

Table 98. ZA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x54, 0x55	0x0000	R/W	Yes

Table 99. ZA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, lower word

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Table 100. ZA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x56, 0x57	0x0000	R/W	Yes

Table 101. ZA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, upper word

The ZA_BIAS_LOW (see Table 98 and Table 99) and ZA_BIAS_HIGH (see Table 100 and Table 101) registers combine to allow users to adjust the bias of the z-axis accelerometers. The data format examples in Table 28 also apply to the ZA_BIAS_HIGH register, and the data format examples in Table 29 apply to the 32-bit combination of the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 57).

Filter Control Register (FILT_CTRL)

Table 102. FILT_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x5C, 0x5D	0x0000	R/W	Yes

Table 103. FILT_CTRL Bit Definitions

Bits	Description
[15:3]	Reserved
[2:0]	Filter Size Variable B, number of taps in each stage, N = 2^B

The FILT_CTRL register (see Table 102 and Table 103) provides user controls for the Bartlett window FIR filter (see Figure 31), which contains two cascaded averaging filters. For example, use the following sequence to set Register FILT_CTRL, Bits[2:0] = 0100, which sets each stage to have 16 taps: 0xCC04 and 0xCD00. Figure 58 provides the frequency response for several settings in the FILT_CTRL register.

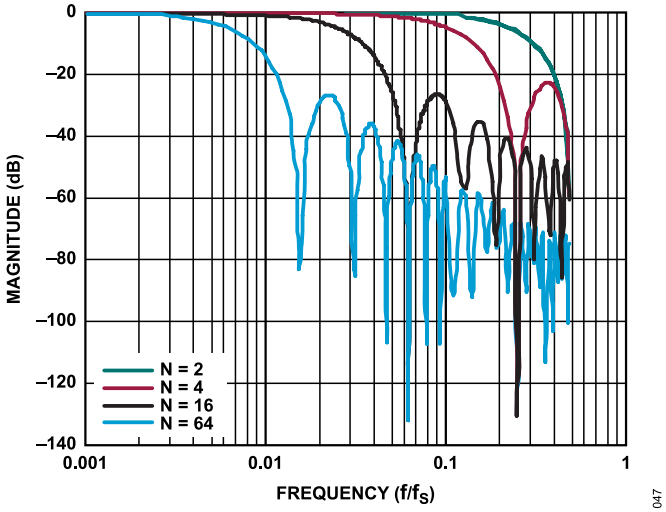

Figure 58. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

Range Identifier (RANG_MDL)

Table 104. RANG_MDL Register Definition

Addresses	Default	Access	Flash Backup
0x5E, 0x5F	Not applicable	R	No

Table 105. RANG_MDL Bit Definitions

Bits	Description
[15:3]	Reserved
[3:2]	Gyroscope measurement range 00 = not used 01 = ±500°/sec (ADIS16501) 10 = not used 11 = not used
[1:0]	Not used, binary value = 11

Miscellaneous Control Register (MSC_CTRL)

Table 106. MSC_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x60, 0x61	0x00C1	R/W	Yes

Table 107. MSC_CTRL Bit Definitions

Bits	Description
[15:10]	Reserved
9	BURST32. 32-bit burst enable bit. The user must wait until a full data ready cycle until the burst array updates with the desired data type. 1 = 32-bit burst data. 0 = 16-bit burst data (default).
8	BURST_SEL. Burst read output array selection. This bit controls what calibrated data is in a burst read. 1 = burst data has delta angle and delta velocity data (default).

USER REGISTER DEFINITIONS

Table 107. MSC_CTRL Bit Definitions (Continued)

Bits	Description
	0 = burst data has gyroscope and accelerometer data.
7	Reserved
6	Point of percussion alignment. When set, this bit allows for relocation of the acceleration sensors to a common point of percussion on the package corner by considering angular rotations. 1 = enabled (default). 0 = disabled.
5	Reserved
4	SENS_BW. Internal sensor bandwidth. 0 = wide bandwidth (default), see Table 1. 1 = 370 Hz. The gyroscope group delay increases by 0.17 ms and the accelerometer group delay increases by 0.63 ms in this mode.
[3:2]	SYNC mode select (see the Clock Control section for more information). 00 = internal SYNC (default). Internal 2 kHz clock used. 01 = direct input sync mode. The user provides an external input clock between 1900 Hz and 2100 Hz. 10 = scaled sync mode. The user provides an external input clock between 1 Hz and 128 Hz, which upscales to 1900 Hz to 2100 Hz inside the ADIS16501. 11 = output sync mode. Identical to internal sync mode, except the SYNC pin functions as an output signal, indicating when the internal clock samples sensors.
1	SYNC polarity (input or output). 1 = rising edge triggers sampling. 0 = falling edge triggers sampling (default).
0	DR polarity. This bit controls the polarity of the DR pin. 1 = active high when data is valid. 0 = active low when data is valid (default).

Point of Percussion

The MSC_CTRL register, Bit 6 (see Table 107) offers an on/off control for the point of percussion alignment function, which maps the accelerometer sensors to the corner of the package that is closest to Pin A1 (see Figure 59). The factory default setting in the MSC_CTRL register activates this function. To turn this function off while retaining the rest of the factory default settings in the MSC_CTRL register, set Register MSC_CTRL, Bit 6 = 0 using the following command sequence on the DIN pin: 0xE081, then 0xE100.

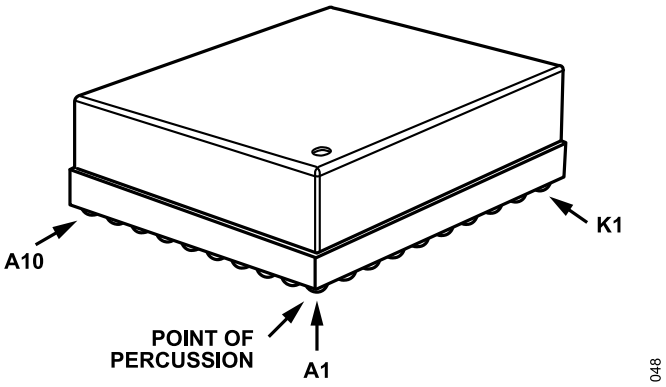

Figure 59. Point of Percussion Reference Point

Sync Mode Select

Refer to the Clock Control section for the functions of the sync mode select bits.

Sync Input Frequency Multiplier (UP_SCALE)

Table 108. UP_SCALE Register Definition

Addresses	Default	Access	Flash Backup
0x62, 0x63	0x07D0	R/W	Yes

Table 109. UP_SCALE Bit Definitions

Bits	Description
[15:0]	K_{ECSF}, binary format

Refer to the Clock Control section for the function and programming of the UP_SCALE register.

Decimation Filter (DEC_RATE)

Table 110. DEC_RATE Register Definition

Addresses	Default	Access	Flash Backup
0x64, 0x65	0x0000	R/W	Yes

Table 111. DEC_RATE Bit Definitions

Bits	Description
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 1999

The DEC_RATE register (see Table 110 and Table 111) provides user control for the averaging decimating filter, which averages and decimates the gyroscope and accelerometer data. The DEC_RATE register also extends the time that the delta angle and the delta velocity track between each update. When the ADIS16501 operates in internal clock mode (see Register MSC_CTRL, Bits[3:2], in Table 107), the nominal output data rate is equal to 2000/(DEC_RATE + 1). For example, set DEC_RATE = 0x0013 to reduce the output sample rate to 100 SPS (2000 ÷ 20) using the following DIN pin sequence: 0xE413, then 0xE500.

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Data Update Rate in External Sync Modes

When using the input sync option in scaled sync mode (Register MSC_CTRL, Bits[3:2] = 10, see Table 107), the output data rate is equal to

$$(f_{SYNC} \times K_{ECSF}) / (DEC\_RATE + 1)$$

where:
f_{SYNC} is the frequency of the clock signal on the SYNC pin.
K_{ESCF} is the value from the UP_SCALE register (see Table 109).

When using direct sync mode, K_{ESCF} = 1.

The NULL_CNFG register, Bits[3:0] establish the total average time (t_A) for the bias estimates, and the NULL_CNFG register, Bits[13:8] provide the on/off controls for each sensor. The factory default configuration for the NULL_CNFG register enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~32 sec.

Global Commands (GLOB_CMD)

Table 112. GLOB_CMD Register Definition

Addresses	Default	Access	Flash Backup
0x68, 0x69	Not applicable	W	No

Table 113. GLOB_CMD Bit Definitions

Bits	Description
[15:8]	Reserved
7	Software reset
[6:5]	Reserved
4	Flash memory test
3	Flash memory update
2	Sensor self test
1	Factory calibration restore
0	Reserved

The GLOB_CMD register (see Table 112 and Table 113) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function. During the execution of these commands, data production stops, pulsing stops on the DR pin, and the SPI does not respond to requests. Table 1 provides the execution time for each GLOB_CMD command.

Software Reset

Use the following DIN sequence to set Register GLOB_CMD, Bit 7 = 1, which triggers a reset: 0xE880, then 0xE900. This reset clears all data, and then restarts data sampling and processing. This function provides a firmware alternative to toggling the $\overline{RST}$ pin (see Table 5, Pin F3).

Flash Memory Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 4 = 1, which tests the flash memory: 0xE810, then 0xE900. The command performs a CRC computation on the flash memory (excluding user register locations) and compares it to the original CRC value, which comes from the factory configuration process. If the current CRC value does not match the original CRC value, Register DIAG_STAT, Bit 6 (see Table 12) rises to 1, indicating a failing result.

Flash Memory Update

Use the following DIN sequence to set Register GLOB_CMD, Bit 3 = 1, which triggers a backup of all user configurable registers in the flash memory: 0xE808, then 0xE900. The DIAG_STAT register, Bit 2 (see Table 12) identifies success (0) or failure (1) in completing this process.

Sensor Self Test

Use the following DIN sequence to set Register GLOB_CMD, Bit 2 = 1, which triggers the self test routine for the inertial sensors: 0xE804, then 0xE900. The self test routine uses the following steps to validate the integrity of each inertial sensor:

1. Measure the output on each sensor.
2. Activate an internal stimulus on the mechanical elements of each sensor to move them in a predictable manner and create an observable response in the sensors.
3. Measure the output response on each sensor.
4. Deactivate the internal stimulus on each sensor.
5. Calculate the difference between the sensor measurements from Step 1 (stimulus is off) and from Step 4 (stimulus is on).
6. Compare the difference with internal pass and fail criteria.
7. Report the pass and fail result to Register DIAG_STAT, Bit 5 (see Table 12).

Motion during the execution of this test can indicate a false failure.

Factory Calibration Restore

Use the following DIN sequence to set Register GLOB_CMD, Bit 1 = 1, to restore the factory default settings for the MSC_ CTRL, DEC_RATE, and FILT_CTRL registers and to clear all user configurable bias correction settings: 0xE802, then 0xE900. Executing this command results in writing 0x0000 to the following registers: XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

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Firmware Revision (FIRM_REV)

Table 114. FIRM_REV Register Definition

Addresses	Default	Access	Flash Backup
0x6C, 0x6D	Not applicable	R	No

Table 115. FIRM_REV Bit Definitions

Bits	Description
[15:0]	Firmware revision, binary coded decimal (BCD) format

The FIRM_REV register (see Table 114 and Table 115) provides the firmware revision for the internal firmware. This register uses a BCD format where each nibble represents a digit. For example, if FIRM_REV = 0x0104, the firmware revision is 1.04. At the time of this data sheet release, FIRM_REV = 0x0200.

Firmware Revision Day and Month (FIRM_DM)

Table 116. FIRM_DM Register Definition

Addresses	Default	Access	Flash Backup
0x6E, 0x6F	Not applicable	R	No

Table 117. FIRM_DM Bit Definitions

Bits	Description
[15:8]	Factory configuration month, BCD format
[7:0]	Factory configuration day, BCD format

The FIRM_DM register (see Table 116 and Table 117) contains the month and day of the factory configuration date. The FIRM_DM register, Bits[15:8] contain digits that represent the month of the factory configuration. For example, November is the 11th month in a year and is represented by Register FIRM_DM, Bits[15:8] = 0x11. The FIRM_DM register, Bits[7:0] contain the day of factory configuration. For example, the 27th day of the month is represented by Register FIRM_DM, Bits[7:0] = 0x27. At the time of this data sheet release, FIRM_DM = 0x1215.

Firmware Revision Year (FIRM_Y)

Table 118. FIRM_Y Register Definition

Addresses	Default	Access	Flash Backup
0x70, 0x71	Not applicable	R	No

Table 119. FIRM_Y Bit Definitions

Bits	Description
[15:0]	Factory configuration year, BCD format

The FIRM_Y register (see Table 118 and Table 119) contains the year of the factory configuration date. For example, the year, 2017, is represented by FIRM_Y = 0x2017. At the time of this data sheet release, FIRM_Y = 0x2023.

Product Identification (PROD_ID)

Table 120. PROD_ID Register Definition

Addresses	Default	Access	Flash Backup
0x72, 0x73	0x5FB5	R	No

Table 121. PROD_ID Bit Definitions

Bits	Description
[15:0]	Product identification = 0x5FB5

The PROD_ID register (see Table 120 and Table 121) contains the numerical portion of the device number (24,501). See Figure 41 for an example of how to use a looping read of this register to validate the integrity of the communication.

Serial Number (SERIAL_NUM)

Table 122. SERIAL_NUM Register Definition

Addresses	Default	Access	Flash Backup
0x74, 0x75	Not applicable	R	No

Table 123. SERIAL_NUM Bit Definitions

Bits	Description
[15:0]	Lot specific serial number

Scratch Registers (USER_SCR_1 to USER_SCR_3)

Table 124. USER_SCR_1 Register Definition

Addresses	Default	Access	Flash Backup
0x76, 0x77	Not applicable	R/W	Yes

Table 125. USER_SCR_1 Bit Definitions

Bits	Description
[15:0]	User defined

Table 126. USER_SCR_2 Register Definition

Addresses	Default	Access	Flash Backup
0x78, 0x79	Not applicable	R/W	Yes

Table 127. USER_SCR_2 Bit Definitions

Bits	Description
[15:0]	User defined

Table 128. USER_SCR_3 Register Definition

Addresses	Default	Access	Flash Backup
0x7A, 0x7B	Not applicable	R/W	Yes

Table 129. USER_SCR_3 Bit Definitions

Bits	Description
[15:0]	User defined

The USER_SCR_1 (see Table 124 and Table 125), USER_SCR_2 (see Table 126 and Table 127), and USER_SCR_3 (see Table 128 and Table 129) registers provide three locations for the user to store

USER REGISTER DEFINITIONS

information. For nonvolatile storage, use the manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 113) after writing information to these registers.

Flash Memory Endurance Counter (FLSHCNT_LOW and FLSHCNT_HIGH)

Table 130. FLSHCNT_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x7C, 0x7D	Not applicable	R	No

Table 131. FLSHCNT_LOW Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 132. FLSHCNT_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x7E, 0x7F	Not applicable	R	No

Table 133. FLSHCNT_HIGH Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, high word

The FLSHCNT_LOW (see Table 130 and Table 131) and FLSHCNT_HIGH (see Table 132 and Table 133) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 60 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

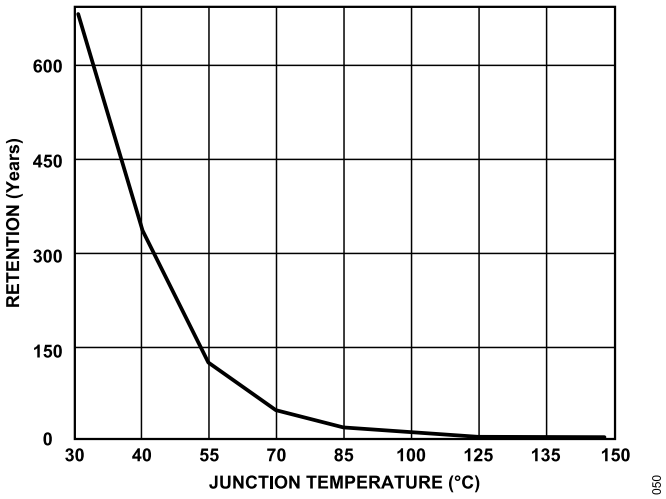

Figure 60. Flash Memory Retention

APPLICATIONS INFORMATION

ASSEMBLY AND HANDLING TIPS

Package Attributes

The ADIS16501 is a multichip module package that has a 100-ball BGA interface. This package has three basic attributes that influence its handling and assembly to the PCB of the system: the lid, the substrate, and the BGA pattern. The material of the lid is a liquid crystal polymer (LCP), and its nominal thickness is 0.5 mm. The substrate is a laminate that has a nominal thickness of 1.57 mm. The solder ball material is SAC305, and each ball has a nominal diameter of 0.75 mm (±0.15 mm). The BGA pattern is a 10 × 10 array.

All electrical and physical connections are through the 10 × 10 array shown in Figure 62. The bottom view in #unique_8/unique_8_Connect_42_F66 shows additional features from the manufacture of the ADIS16501 that are not relevant to the mounting or use of the ADIS16501.

Assembly Tips

When attaching the ADIS16501 to a PCB, follow these guidelines:

- The ADIS16501 supports solder reflow attachment processes in accordance with J-STD-020E.
- Limit device exposure to one pass through the solder reflow process (no rework).
- The hole in the top of the lid (see Figure 61) provides venting and pressure relief during the assembly process of the ADIS16501. This hole must be kept clear while attaching the ADIS16501 to a PCB. However, covering the hole in normal operation is not typically a problem.

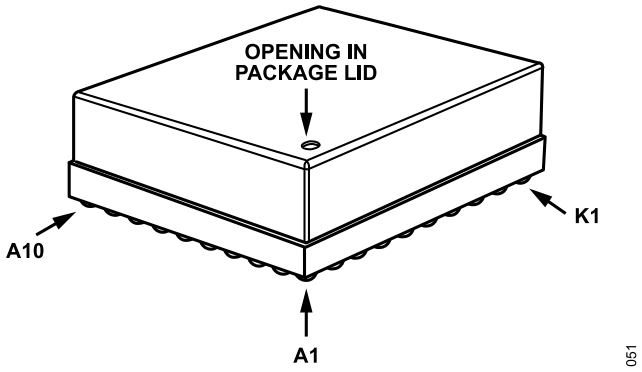

Figure 61. Pressure Relief Hole

- Use no clean flux and avoid exposing the device to cleaning solvents that can penetrate the inside of the ADIS16501 through multiple paths.
- Manage moisture exposure prior to the solder reflow processing in accordance with J-STD-033, Moisture Sensitivity Level 5.
- Avoid exposing the ADIS16501 to mechanical shock survivability that exceeds the maximum rating in Table 3. In standard PCB processing, high speed handling equipment and panel separation processes often present the most risk of introducing harmful levels of mechanical shock survivability.

PCB Layout Suggestions

Figure 62 shows an example of the pad design and layout for the ADIS16501 on a PCB. This example uses a solder mask opening with a diameter of 0.73 mm, around a metal pad that has a diameter of 0.56 mm. When using a material for the system PCB that has similar thermal expansion properties as the substrate material of the ADIS16501, the system PCB can also use the solder mask to define the pads that support attachment to the balls of the ADIS16501. The coefficient of thermal expansion (CTE) in the substrate of the ADIS16501 is approximately 14 ppm/°C.

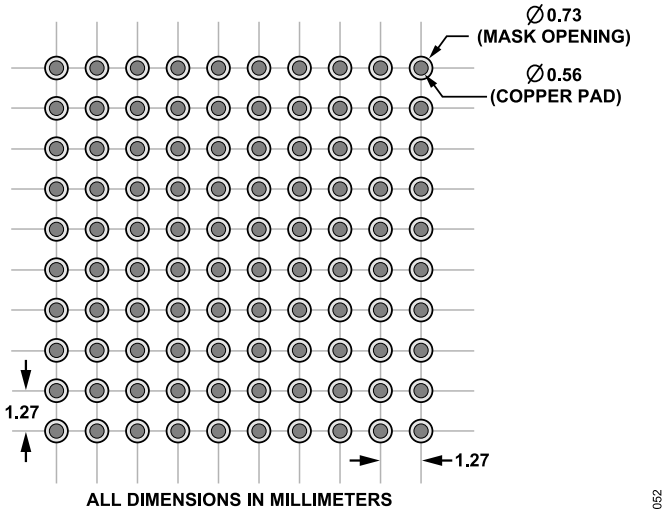

Figure 62. Recommended PCB Pattern, Solder Mask Defined Pads

Underfill

Underfill can be a useful technique in managing certain threats to the integrity of the solder joints of the ADIS16501, including peeling stress and extended exposure to vibration. When selecting underfill material and developing an application and curing process, ensure that the material fills the gap between each surface (the ADIS16501 substrate and system PCB) and adheres to both surfaces. The ADIS16501 does not require the use of underfill materials in applications that do not anticipate exposure to these types of mechanical stresses and when the CTE of the system PCB is close to the same value as the CTE of the substrate of the ADIS16501 (~14 ppm/°C).

Process Validation and Control

These guidelines provide a starting point for developing a process for attaching the ADIS16501 to a system PCB. Because each system and situation can present unique requirements for this attachment process, ensure that the process supports optimal solder joint integrity, verify that the final system meets all environmental test requirements, and establish observation and control strategies

APPLICATIONS INFORMATION

for all key process attributes (for example, peak temperatures, dwell times, and ramp rates).

POWER SUPPLY CONSIDERATIONS

The ADIS16501 contains 6 µF of decoupling capacitance across the VDD and GND pins. When the VDD voltage rises from 0 V to 3.3 V, the charging current for this capacitor bank imposes the following current profile (in amperes):

$$I_{DD}(t) = C\frac{dVDD}{dt} = 6 \times 10^{-6} \times \frac{dVDD(t)}{dt}$$

where:
$I_{DD}(t)$ is the current demand on the VDD pin during the initial power supply ramp, with respect to time.
C is the internal capacitance across the VDD and GND pins (6 µF).
$VDD(t)$ is the voltage on the VDD pin, with respect to time.

For example, if VDD follows a linear ramp from 0 V to 3.3 V, in 66 µs, the charging current is 300 mA for that timeframe. The ADIS16501 also contains embedded processing functions that present transient current demands during initialization or reset recovery operations. During these processes, the peak current demand reaches 250 mA and occurs at a time that is approximately 40 ms after VDD reaches 3.0 V (or ~40 ms after initiating a reset sequence).

EVALUATION TOOLS

Breakout Boards

The ADIS16501 has a breakout board that provides a simple way to connect an ADIS16501 model and an existing embedded processor platform. Table 134 shows the model number for the breakout board. Figure 63 shows the ADIS16505-2 board that is identical to the ADIS16501 board.

Figure 63. ADIS16501 Breakout Board (ADIS16505-2 Shown)

Table 134. Breakout Board Models

Breakout Board Model	ADIS16501 Model
ADIS16501/PCBZ	ADIS16501

The electrical interface (J1) on each breakout board comes from a dual row, 2 mm pitch, 16-pin interface, which supports standard ribbon cabling (1 mm pitch). Table 135 provides the J1 pin assignments, which support direct connection with an embedded processor board using standard ribbon cables. Although each case may present its own set of sensitivities (such as electromagnetic interference (EMI)), these boards can typically support reliable communication over ribbon cables up to 20 cm in length.

Table 135. J1 Pin Assignments, Breakout Board

J1 Pin Number	Signal	Function
1	$\overline{RST}$	Reset
2	SCLK	SPI
3	CS	SPI
4	DOUT	SPI
5	NC	No connect
6	DIN	SPI
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	VDD	Power, 3.3 V
11	VDD	Power, 3.3 V
12	VDD	Power, 3.3 V
13	DR	Data ready
14	SYNC	Input clock
15	NC	No connect
16	NC	No connect

Figure 64 provides a top view of the breakout board, including dimensional locations for all the key mechanical features, such as the mounting holes and the 16-pin header. Figure 65 provides an electrical schematic for this breakout board. For additional information, refer to the ADIS1650x-x/PCBZ Breakout Board Wiki Guide.

PC-Based Evaluation, EVAL-ADIS2

In addition to supporting quick prototype connections between the ADIS16501 and an embedded processing system, J1 on the breakout boards also connects directly to J1 on the EVAL-ADIS2 evaluation system. When used with the IMU Evaluation Software for the EVAL-ADISX Platforms, the EVAL-ADIS2 provides a simple, functional test platform that allows users to configure and collect data from the ADIS16501 IMUs.

APPLICATIONS INFORMATION

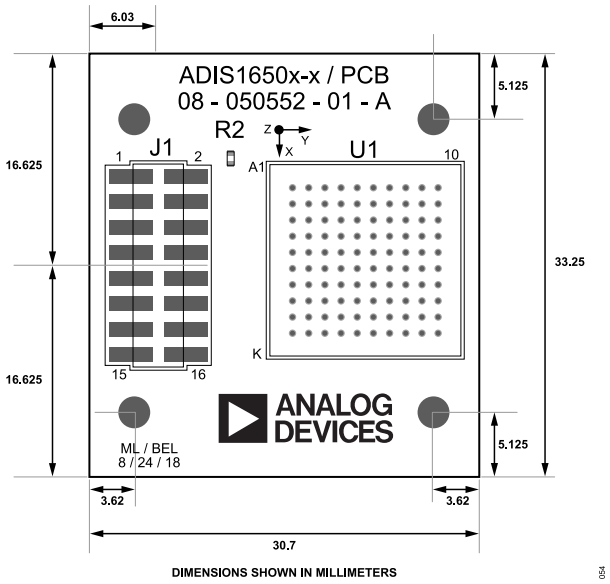

Figure 64. Top View of the ADIS16501 Breakout Board

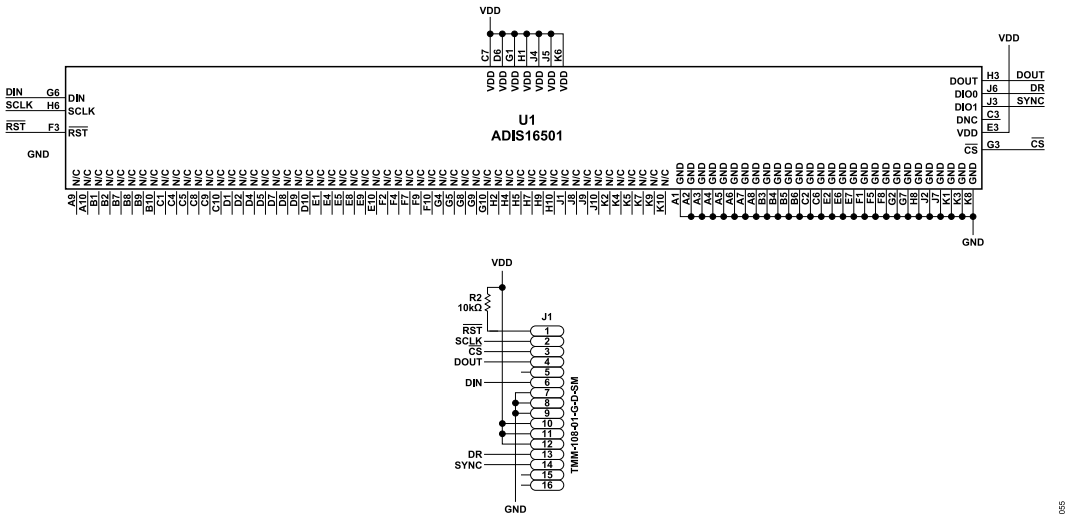

Figure 65. ADIS16501 Breakout Board Schematic

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
ML-100-1	BGA	100-Ball Ball Grid Array Module

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: March 20, 2024

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Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADIS16501-2BMLZ	-40°C to +105°C	100-Ball Ball Grid Array Module (15mm x 15mm x 5.72mm)	EACH, 1	ML-100-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADIS16501-2/PCBZ	ADIS16501-2/PCBZ Breakout Board
ADIS16501/PCBZ	Evaluation Board
EVAL-ADIS-FX3Z	EVAL-ADIS-FX3 Evaluation Board

[1] Z = RoHS Compliant Part.