ADAQ4381-4

Quad, 14-bit, 4 MSPS, Simultaneous Sampling, µModule Data Acquisition Solution

FEATURES

- Easy to use µModule® data acquisition system
  - 11× footprint reduction vs. discrete solution
  - Integrated critical passive components
  - 5 V single supply operation
- Guaranteed 14-bit no missing codes
- On-chip oversampling function
- 2-bit resolution boost
- Out of range Indicator ($\overline{\text{ALERT}}$)
- INL: ±0.5 LSB typical, ±1 LSB maximum
- SNR (typical)
  - 84 dB at Gain = 1.0, f_{IN}= 1 kHz
  - 90 dB with OSR = ×8 at Gain = 1.0, f_{IN}= 1 kHz
- Channel-to-Channel phase matching: 0.005° typical at f_{IN}= 20 kHz
- Integrated high precision reference, 3 ppm/°C typical drift
- Gain error: 0.005% typical
- Gain drift: 0.8 ppm/°C typical
- Integrated internal buffer with VCM generation
- Integrated fully differential ADC driver with signal scaling
  - Wide input common-mode voltage range
  - High common-mode rejection
- Single-ended to differential conversion
- Pin selectable input range with overrange
  - Input range: ±2 V, ±3.3 V, ±5.5 V, ±11 V
  - Gain/Attenuation: G = 0.3, 0.6, 1.0, and 1.6
- High-speed serial interface
- 8 mm x 8 mm, 0.8 mm pitch, 81-ball CSP_BGA package

APPLICATIONS

- Lab grade battery test system
- Motor control current sense
- Motor control position feedback
- Sonar
- Power quality monitoring
- Data acquisition system
- Erbium-Doped Fiber Amplifier (EDFA) applications
- I and Q demodulation

GENERAL DESCRIPTION

The ADAQ4381-4 is a quad-channel precision data acquisition (DAQ) signal chain µModule solution that reduces the development cycle of a precision measurement system by transferring the signal chain design challenges of component selection, optimization, and layout from the designer to the device.

Using system-in-package (SIP) technology, the ADAQ4381-4 reduces end system component count by combining multiple common signal processing and conditioning blocks into a single device. These blocks include a quad-channel, high resolution 14-bit, 4 MSPS simultaneous sampling SAR ADC, low noise, fully differential ADC driver amplifier, a 3.3 V precision voltage reference, low-noise buffer amplifiers, and low-dropout linear regulator.

The ADAQ4381-4 has an on-chip oversampling blocks to improve the dynamic range and reduce noise at lower bandwidths. The oversampling can boost up to two bits of added resolution. It provides the flexibility of a configurable ADC driver feedback loop to allow four gain and attenuation adjustments, and accept both fully differential or single-ended to differential input configuration.

Using Analog Devices, Inc. *i*Passives® technology, the ADAQ4381-4 incorporates critical passive components with superior matching and drift characteristics to minimize temperature dependent error sources and to offer optimized signal chain performance. Housed in a small 8 mm × 8 mm × 0.8 mm pitch, 81-ball CSP_BGA package, the ADAQ4381-4 enables compact design without sacrificing performance and simplifies end system bill of materials management. The ADAQ4381-4's optimum performance is guaranteed with a single 5 V supply operation, all the required bypass and decoupling capacitors are included inside the package. The level of ADAQ4381-4 system integration solves many design challenges, which enables a compact and simple solution for a multichannel application.

The conversion result can clock out simultaneously through 4-wire mode for faster throughput or through 1-wire serial mode when slower throughput is allowed. The ADAQ4381-4 is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using the separate logic supply. The ADAQ4381-4 is specified to operate over a temperature range of −40°C to +105°C.

Table 1. µModule® Data Acquisition Solutions

Type	500 kSPS	1 MSPS to 2 MSPS	4 MSPS
14-bit			ADAQ4381-4
16-bit	ADAQ7988	ADAQ4370-4 ADAQ7980 ADAQ4001	ADAQ4380-4
18-bit		ADAQ4003	

TABLE OF CONTENTS

TYPICAL APPLICATION DIAGRAM

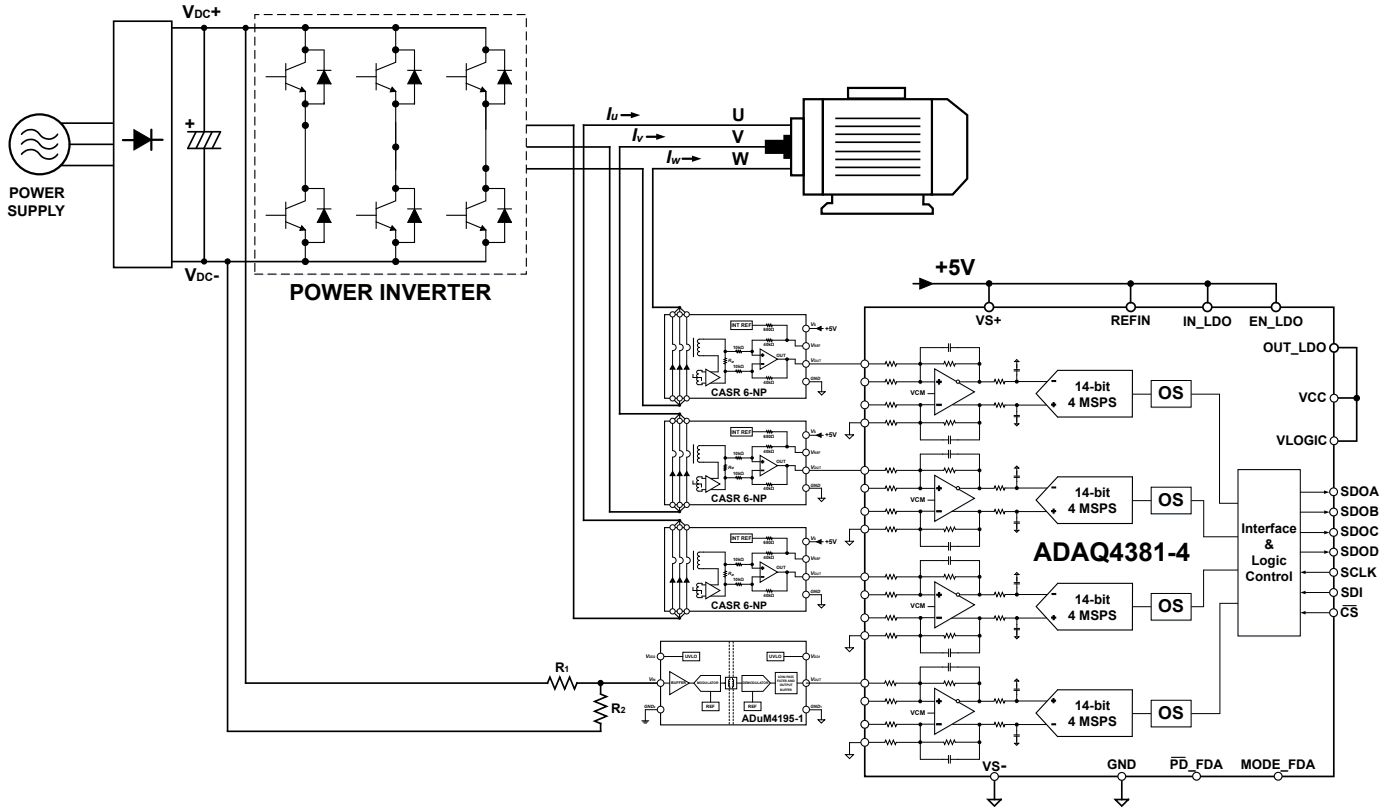

Figure 1. Precision Current and Voltage Sensing for Servo Motors Control using ADAQ4381-4

SPECIFICATIONS

V_{S+} = REFIN = IN_LDO = EN_LDO = 5 V ± 5%, V_{CC} = V_{LOGIC} = 3.45 V (OUT_LDO), V_{S-} = 0 V, reference voltage (V_{REF}) = 3.3 V internal, f_{SAMPLE} = 4 MSPS, fully differential input configuration, full power mode, T_A = 25°C , no oversampling, unless otherwise noted.

Table 2. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT CHARACTERISTICS					
Differential Input Voltage Range, V_{IN}[1]	Gain = 0.3, V_{IN} = 22 V p-p	−11		+11	V
	Gain = 0.6, V_{IN} = 11 V p-p	−5.5		+5.5	V
	Gain = 1.0, V_{IN} = 6.6 V p-p	−3.3		+3.3	V
	Gain = 1.6, V_{IN} = 4.125 V p-p	−2.0625		+2.0625	V
Input Resistance, R_{IN}	Fully differential input configuration				
	Gain = 0.3, 0.6		5.40		kΩ
	Gain = 1.0		3.24		kΩ
	Gain = 1.6		2.026		kΩ
	Single-ended input configuration				
	Gain = 0.3		3.05		kΩ
	Gain = 0.6		3.32		kΩ
	Gain = 1.0		2.16		kΩ
	Gain = 1.6		1.46		kΩ
Input Capacitance	IN_X+, IN_X−		2		pF
THROUGHPUT					
Conversion Rate (f_{SAMPLE})				4	MSPS
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Delay Match			46.8	145	ps
Aperture Jitter			20		ps
OVERALL SYSTEM DC ACCURACY					
No Missing Codes		14			Bits
Differential Nonlinearity Error (DNL)	All gains, V_{S-} = 0 V	−0.99	±0.7	+1	LSB
Integral Nonlinearity Error (INL)[2]	All gains, V_{S-} = 0 V	−2	±0.4	+2	LSB
Gain Error	Gain = 0.3	−0.08	±0.01	+0.08	%FS
	Gain = 0.6, 1.0, 1.6	−0.05	±0.01	+0.05	%FS
Gain Error Drift	All gains		0.8		ppm/°C
Offset Error, Referred to Output (RTO)	Gain = 0.3	−0.65	±0.03	+0.65	mV
	Gain = 0.6	−0.6	±0.03	+0.6	mV
	Gain = 1.0	−0.75	±0.03	+0.75	mV
	Gain = 1.6	−0.9	±0.03	+0.9	mV
Offset Error Drift	All gains	−2	±0.5	+2	µV/°C
Common-Mode Rejection Ratio (CMRR)	$\Delta V_{ICM}/\Delta V_{OSDIFF}$		80		dB
Power-Supply Rejection Ratio	V_{S+}, REFIN, IN_LDO = 4.75 V to 5.25 V, VS− = GND		95		dB
OVERALL SYSTEM AC ACCURACY[3]	Fully differential and single-ended input configuration				
Dynamic Range	V_{IN} = −60 dBFS, f_{IN} = 1 kHz				
	Gain = 0.3		TBD		dB
	Gain = 0.6		TBD		dB
	Gain = 1.0		TBD		dB
	Gain = 1.6		TBD		dB
Total RMS Noise, Referred to Output (RTO)	V_{IN} = −60 dBFS, f_{IN} = 1 kHz				
	Gain = 0.3		TBD		μV_{RMS}
	Gain = 0.6		TBD		μV_{RMS}
	Gain = 1.0		TBD		μV_{RMS}

SPECIFICATIONS

Table 2. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Gain = 1.6		TBD		μV_{RMS}
Signal-to-Noise Ratio	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz				
	Gain = 0.3		TBD		dB
	Gain = 0.6		TBD		dB
	Gain = 1.0		TBD		dB
	Gain = 1.6		TBD		dB
	Gain = 1.0, rolling average OSR = 8×, RES = 1		TBD		dB
	Gain = 1.0, low power mode		TBD		dB
	Gain = 1.0, f_{IN} = 100 kHz, full power mode		TBD		dB
	Gain = 1.0, f_{IN} = 200 kHz, full power mode		TBD		dB
Signal-to-Noise + Distortion	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz				
(SINAD)	Gain = 0.3		TBD		dB
	Gain = 0.6		TBD		dB
	Gain = 1.0		TBD		dB
	Gain = 1.6		TBD		dB
	Gain = 1.0, low power mode		TBD		dB
	Gain = 1.0, f_{IN} = 100 kHz, full power mode		TBD		dB
	Gain = 1.0, f_{IN} = 200 kHz, full power mode		TBD		dB
Total Harmonic Distortion	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz				
	All gains		−109		dB
Spurious-Free Dynamic Range	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz				
	All gains		110		dB
−3 dB Bandwidth	Gain = 0.3		12.5		MHz
	Gain = 0.6, 1.0, 1.6		5.8		MHz
Channel-to-Channel Isolation	All gains, f_{IN} = 1 kHz		−113		dB
Channel-to-Channel Phase Matching	All gains, f_{IN} = 20 kHz		0.005		Degrees
REFERENCE CHARACTERISTICS					
V_{REFIN}	Internal-reference supply voltage	4.5	5.0	5.5	V
I_{REFIN}	Internal-reference supply current		350	600	µA
$V_{REFSENSE}$	Internal-reference output voltage sense		3.3		V
	−40°C to +105°C	3.285		3.315	V
V_{REF} Temperature Coefficient	TCV_{OUT}				
	−40°C ≤ T_A ≤ +105°C		3	10	ppm/°C
V_{REF} Line Regulation			1.2	5	ppm/V
V_{REF} Load Regulation			3	8	ppm/mA
V_{REF} Noise			9		μV_{RMS}
Output Voltage Hysteresis[4]	ΔV_{OUT_HYS}				
	ΔT = 25°C to −40°C to 25°C		43		ppm
	ΔT = 25°C to 105°C to 25°C		−50		ppm
	ΔT = −40°C to +105°C		8		ppm
LDO CHARACTERISTICS					
IN_LDO Voltage Range		4.5	5.0	5.5	V
IN_LDO Supply Current	I_{OUT_LDO} = 150 mA		130	190	µA
OUT_LDO Voltage	Internal LDO Output	3.35	3.45	3.5	V
Maximum Output Current			150		mA
Shutdown Current	IN_LDO = GND		0.1	1	µA
Load Regulation	I_{OUT_LDO} = 1 mA to 150 mA		0.0005		%/mA
Start-Up Time			350		µs

SPECIFICATIONS

Table 2. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$)	Logic levels				
Input Voltage Low (V_{IL})	V_{LOGIC} < 2.3 V			0.45	V
	V_{LOGIC} ≥ 2.3 V			0.7	V
Input Voltage High (V_{IH})	V_{LOGIC} < 2.3 V	V_{LOGIC} − 0.45			V
	V_{LOGIC} ≥ 2.3 V	0.8 × V_{LOGIC}			V
Input Current Low (I_{IL})		−1		+1	µA
Input Current High (I_{IH})		−1		+1	µA
DIGITAL OUTPUTS (SDOA, SDOB, SDOC, SDOD/$\overline{ALERT}$)					
Output Coding		Twos complement			Bits
Output Low Voltage (V_{OL})	Current sink (I_{SINK}) = +300 µA			0.4	V
Output High Voltage (V_{OH})	Current source (I_{SOURCE}) = +300 µA	V_{LOGIC} − 0.3			V
Floating-State Leakage Current				±1	µA
Floating-State Output Capacitance			10		pF
POWER-DOWN/MODE SIGNALING	$\overline{PD}$_FDA/MODE_FDA				
Low	Disabled, low power mode		<1		V
High	Enabled, full power mode		>1.5		V
POWER SUPPLY REQUIREMENTS					
Operating Voltage Range					
V_{CC}		3.4		3.6	V
V_{LOGIC}		1.65		3.6	V
V_{S+}[5]		4.5	5.0	5.5	V
V_{S-}		−5		0	V
ADAQ4381-4 Current Draw	V_{CC} = V_{LOGIC} = 3.45 V, V_S = 5 V				
I_{VCC}	V_{CC} supply current				
	Normal mode (Dynamic)		38	42	mA
	Normal mode (Static)		1.7	2	mA
	Shutdown mode		101	200	µA
I_{VLOGIC}	V_{LOGIC} supply current				
	Normal mode (Dynamic)		7.3	9	mA
	Normal mode (Static)		10	200	nA
	Shutdown mode		10	200	nA
I_{VS+}/I_{VS-}	V_{S+}/V_{S-} supply current				
	Full power mode		25	28	mA
	Low power mode		15	18	mA
ADAQ4381-4 Power Dissipation	V_{CC} = V_{LOGIC} = 3.45 V, V_S = 5 V				
P_{VCC}	V_{CC} power				
	Normal mode (Dynamic)		130	155	mW
	Normal mode (Static)		6	7	mW
P_{VLOGIC}	V_{LOGIC} power				
	Normal mode (Dynamic)		25	28	mW
	Normal mode (Static)		36	720	nW
$P_{VS+/VS-}$	V_{S+}/V_{S-} power				
	Full power mode		125	135	mW
	Low power mode		75	80	mW
Total Power Dissipation	ADAQ4381-4 power dissipation				
	Dynamic, full power mode		280	318	mW

SPECIFICATIONS

Table 2. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Dynamic, low power mode		160	175	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}[6]	−40		+105	°C

[1] The absolute differential input ranges, V_{IN}, must be within the allowed input common-mode range as per Figure 22 to Figure 29. V_{IN} is dependent on the VS+ and VS− supply rails used.

[2] Limit the absolute differential input range, V_{IN}, to 95% of full scale to allow enough footroom for the ADC driver with V_S = 0 V to achieve specified performance.

[3] All AC specifications expressed in decibels are referred to full-scale input range (FSR) and are tested with an input signal of 0.5 dB below full scale, unless otherwise specified.

[4] Hysteresis in output voltage is created by package stress that differs depending on whether the IC is previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis measures the maximum output change for the averages of three hot or cold temperature cycles. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), it is usually not a dominant error source. Typical hysteresis is the worst-case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

[5] Maximum operating supply voltage, V_S (V_{S+} − V_{S-}) should not exceed 10 V.

[6] The ADAQ4381-4 is rated for performance over extended industrial temperature range, T_{CASE} = −40°C to +105°C.

SPECIFICATIONS

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 3.3 V, T_A = −40°C to +105°C, unless otherwise noted.

Table 3. Digital Interface Timing

Parameter	Min	Typ	Max	Unit	Description
t_{CYC}	250			ns	Time between conversions
t_{SCLKED}	5			ns	$\overline{CS}$ falling edge to first SCLK falling edge
t_{SCLK}	12.5			ns	SCLK period
t_{SCLKH}	5.5			ns	SCLK high time
t_{SCLKL}	5.5			ns	SCLK low time
t_{CSH}	20			ns	$\overline{CS}$ pulse width
t_{QUIET}	20			ns	Interface quiet time prior to conversion
t_{SDOEN}					$\overline{CS}$ low to SDOx enabled
			5.5	ns	$V_{LOGIC} \geq 1.75$ V
			7.4	ns	$V_{LOGIC} < 1.75$ V
t_{SDOH}	3			ns	SCLK rising edge to SDOx hold time
t_{SDOS}					SCLK rising edge to SDOx setup time
			5	ns	$V_{LOGIC} \geq 2.1$ V
			7.2	ns	$1.65 \text{ V} \leq V_{LOGIC} < 2.1$ V
t_{SDOT}			8	ns	$\overline{CS}$ rising edge to SDOx high impedance
t_{SDIS}	4			ns	SDI setup time prior to SCLK falling edge
t_{SDIH}	4			ns	SDI hold time after SCLK falling edge
t_{SCLKCS}	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$			190	ns	Conversion time
$t_{ACQUIRE}$	110			ns	Acquire time
t_{RESET}		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{POWER-UP}$					Supply active to conversion
			5	ms	First conversion allowed
			5	ms	Settled to within 1%
$t_{REGWRITE}$			5	ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting shutdown mode to conversion
			10	µs	Settled to within 1%
$t_{CONVERT0}$	6	8	10	ns	Conversion time for first sample in OS normal mode
$t_{CONVERTx}$	$t_{CONVERT0} + (250 \times (x - 1))$			ns	Conversion time for x^{th} sample in OS normal mode
t_{ALERTS}			220	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ indication
t_{ALERTC}			10	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ clear
t_{ALERTS_NOS}			20	ns	Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication

SPECIFICATIONS

Timing Diagrams

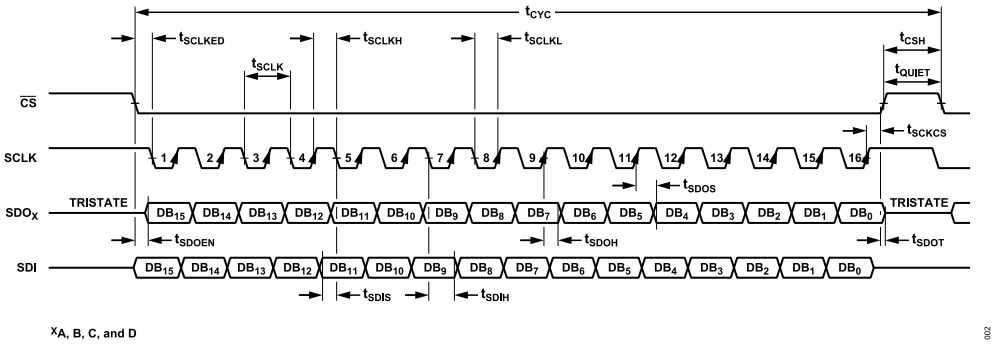

Figure 2. Serial Interface Timing Diagram

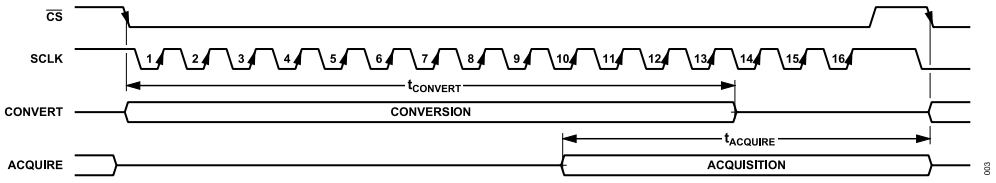

Figure 3. Internal Conversion Acquire Timing

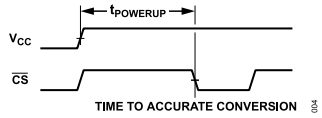

Figure 4. Power-Up Time to Conversion

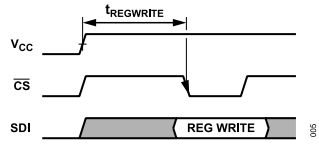

Figure 5. Power-Up Time to Register Read Write Access

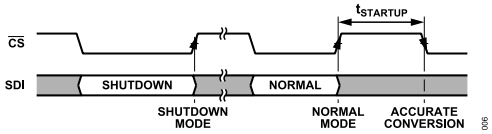

Figure 6. Shutdown Mode to Normal Mode Timing

SPECIFICATIONS

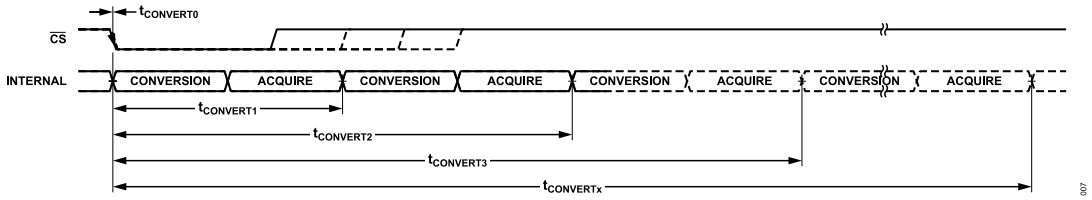

Figure 7. Conversion Timing During OS Normal Mode

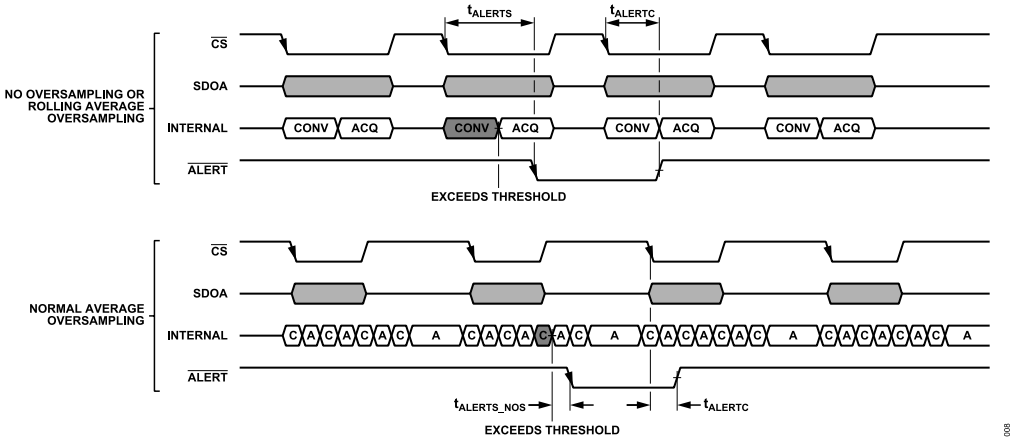

Figure 8. $\overline{\text{ALERT}}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
IN_X1+, IN_X1-, IN_X2+, IN_X2- to GND	−12.5 V to +12.5 V or ± 10 mA
Supply Voltages	
V_S	11 V
IN_LDO to GND	−0.3 V to +6.5 V
EN_LDO to GND	−0.3 V to +6.5 V
V_{LOGIC} to GND	−0.3 V to +4 V
V_{CC} to GND	−0.3 V to +4 V
REFIN to GND	−0.3 V to +38 V
Digital Inputs to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Outputs to GND	−0.3 V to V_{LOGIC} + 0.3 V
Temperature	
Storage Range	−65°C to +150°C
Junction	125°C
Lead Soldering	260°C reflow as per JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-81-7	27.2	38.1	10.4	11.9	5.7	12.0	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the θ_{JC_TOP}, which uses 1S0P JEDEC PCB.

Thermal resistance values specified in Table 5 are simulated based on JEDEC specs (unless specified otherwise) and should be used in compliance with JESD51-12.

ELECTROSTATIC DISCHARGE RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ4381-4

Table 6. ADAQ4381-4, 81-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	± 2000	2
FICDM	± 750	C2B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADAQ4380-4
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9
A	GND	INC1+	INC1–	IND2+	IND2–	IND1+	IND1–	GND	GND
B	GND	OUTC–	OUTC+	SJD+	SJD–	OUTD–	OUTD+	GND	SDOD/ ALERT
C	INC2–	SJC–	VS+	VS+	IN_LDO	EN_LDO	GND	V_{LOGIC}	SDOC
D	INC2+	SJC+	VS+	VS+	IN_LDO	OUT_LDO	OUT_LDO	GND	XX9DXX
E	GND	PD_FDA	MODE_ FDA	GND	GND	DNC	V_{CC}	GND	SDI
F	INB2+	SJB+	VS–	VS–	DNC	DNC	REFIN	GND	SDOB
G	INB2–	SJB–	VS–	VS–	GND	REFSENSE	DNC	GND	SDOA
H	GND	OUTB–	OUTB+	SJA+	SJA–	OUTA–	OUTA+	GND	$\overline{CS}$
J	GND	INB1+	INB1–	INA2+	INA2–	INA1+	INA1–	GND	GND

NOTES
1. DO NOT CONNECT. LEAVE THESE PINS FLOATING/UNCONNECTED.

600

Figure 9. Pin Configuration

Table 7. Pin Function Descriptions

Pin Number	Mnemonic	Type[1]	Description
A1, A8, A9, B1, B8, C7, D8, E1, E4, E5, E8, F8, G5, G8, H1, H8, J1, J8, J9	GND	P	Power Supply Ground.
A2	INC1+	AI	Channel C Positive Input to 1.62 kΩ Gain Resistor Network.
A3	INC1−	AI	Channel C Negative Input to 1.62 kΩ Gain Resistor Network.
A4	IND2+	AI	Channel D Positive Input to 2.70 kΩ Gain Resistor Network.
A5	IND2−	AI	Channel D Negative Input to 2.70 kΩ Gain Resistor Network.
A6	IND1+	AI	Channel D Positive Input to 1.62 kΩ Gain Resistor Network.
A7	IND1−	AI	Channel D Negative Input to 1.62 kΩ Gain Resistor Network.
B2	OUTC−	AO[2]	ADC Driver Negative Output for Channel C.
B3	OUTC+	AO[2]	ADC Driver Positive Output for Channel C.
B4	SJD+	AI	ADC Driver Positive Input Summing Node for Channel D.
B5	SJD−	AI	ADC Driver Negative Input Summing Node for Channel D.
B6	OUTD−	AO[2]	ADC Driver Negative Output for Channel D.
B7	OUTD+	AO[2]	ADC Driver Positive Output for Channel D.
B9	SDOD/$\overline{ALERT}$	DO	Serial Data Output D/$\overline{ALERT}$. This pin functions as a serial data output to or alert indication output. SDOD. This pin functions as a serial data output pin to access the conversion results. $\overline{ALERT}$. This pin operates as an alert pin going low to indicate that a conversion result has exceeded a configured threshold.
C1	INC2−	AI	Channel C Negative Input to 2.70 kΩ Gain Resistor Network.
C2	SJC−	AI	ADC Driver Negative Input Summing Node for Channel C.
C3, C4, D3, D4	VS+	P	Amplifiers Positive Supply. These pins are decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C5, D5	IN_LDO	P	Integrated LDO Input Voltage. Connect to VS+ (or 3.6 V < IN_LDO < 5.5 V). This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C6	EN_LDO	P	LDO enable. Connect to IN_LDO or VS+ to enable the internal LDO. Connect to GND if otherwise.
C8	VLOGIC	P	ADC Logic Interface Supply Voltage. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
C9	SDOC	DO	Serial Data Output C. This pin functions as a serial data output pin to access the conversion results and register contents.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
D1	INC2+	AI	Channel C Positive Input to 2.70 kΩ Gain Resistor Network.
D2	SJC+	AI	ADC Driver Positive Input Summing Node for Channel C.
D6, D7	OUT_LDO	P	Integrated LDO Output Voltage. The voltage at this pin is 3.45 V typical.
D9	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC.
E2	$\overline{\text{PD}}$_FDA	P	Active low. Connect this pin to GND to power down (disable) the ADC Drivers. Connect VS+ for normal operation.
E3	MODE_FDA	P	Power Mode for ADC Drivers. Connect to VS+ for full power mode. Connect to GND to enter low power mode.
E6, F5, F6, G7	DNC	N/A[3]	Do Not Connect. Leave these pins floating/unconnected.
E7	VCC	P	ADC Analog Supply Voltage. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
E9	SDI	DI	Serial Data Input. This input provides the data written to the on-chip control registers.
F1	INB2+	AI	Channel B Positive Input to 2.70 kΩ Gain Resistor Network.
F2	SJB+	AI	ADC Driver Positive Input Summing Node for Channel B.
F3, F4, G3, G4	VS−	P	Amplifiers Negative Supply. These pins are decoupled to ground internally. Additional decoupling capacitors may not be necessary.
F7	REFIN	P	Internal Reference Supply Voltage. Connect to VS+ for normal operation. This pin is decoupled to ground internally. Additional decoupling capacitors may not be necessary.
F9	SDOB	DO	Serial Data Output B. This pin functions as a serial data output pin to access the conversion results and register contents.
G1	INB2−	AI	Channel B Negative Input to 2.70 kΩ Gain Resistor Network.
G2	SJB−	AI	ADC Driver Negative Input Summing Node for Channel B.
G6	REFSENSE	AO[2]	Reference Output Sense pin. For accurate gain calibration, use this pin to measure the actual level of the internal 3.3 V reference. If not utilized, leave this pin floating and unconnected. Capacitive load connected to this pin should not exceed 1 µF to ensure system stability.
G9	SDOA	DO	Serial Data Output A. This pin functions as a serial data output pin to access the conversion results and register contents.
H2	OUTB−	AO[2]	ADC Driver Negative Output for Channel B.
H3	OUTB+	AO[2]	ADC Driver Positive Output for Channel B.
H4	SJA+	AI	ADC Driver Positive Input Summing Node for Channel A.
H5	SJA−	AI	ADC Driver Negative Input Summing Node for Channel A.
H6	OUTA−	AO[2]	ADC Driver Negative Output for Channel A.
H7	OUTA+	AO[2]	ADC Driver Positive Output for Channel A.
H9	$\overline{\text{CS}}$	DI	Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the ADAQ4381-4 and framing the serial data transfer.
J2	INB1+	AI	Channel B Positive Input to 1.62 kΩ Gain Resistor Network.
J3	INB1−	AI	Channel B Negative Input to 1.62 kΩ Gain Resistor Network.
J4	INA2+	AI	Channel A Positive Input to 2.70 kΩ Gain Resistor Network.
J5	INA2−	AI	Channel A Negative Input to 2.70 kΩ Gain Resistor Network.
J6	INA1+	AI	Channel A Positive Input to 1.62 kΩ Gain Resistor Network.
J7	INA1−	AI	Channel A Negative Input to 1.62 kΩ Gain Resistor Network.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

[2] Analog Output pins are for voltage monitoring/measurement, and setting the gain of ADAQ4381-4 only. These pins must not be driven externally.

[3] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = REFIN = IN_LDO = EN_LDO = 5 V, V_{CC} = V_{LOGIC} = 3.45 V, reference voltage (V_{REF}) = 3.3 V internal, f_{SAMPLE} = 4 MSPS, fully differential input configuration, full power mode, T_A = 25°C, no oversampling, unless otherwise noted.

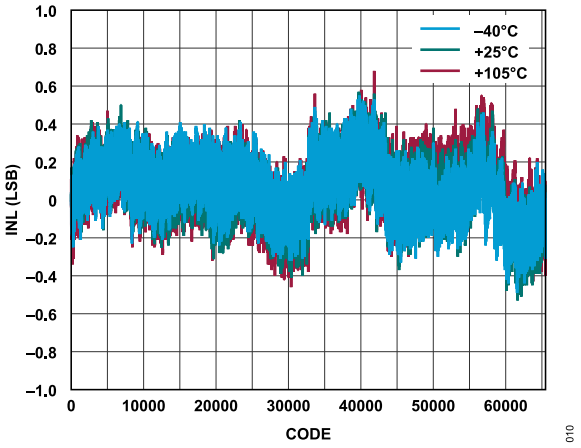

Figure 10. INL vs. Code for Various Temperature, Gain = 1.0

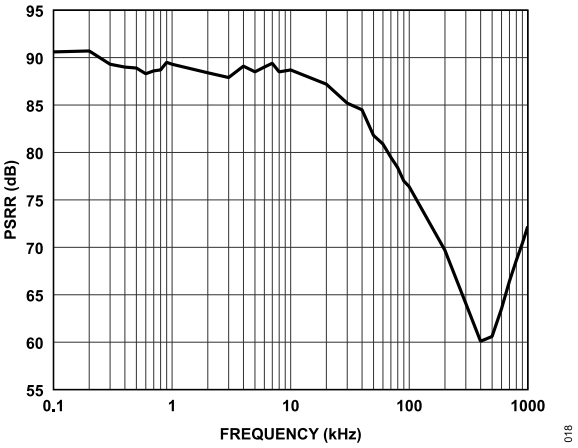

Figure 13. PSRR vs. Frequency

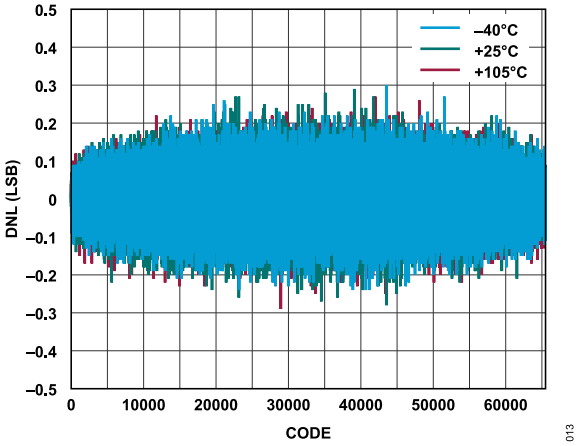

Figure 11. DNL vs. Code for Various Temperature, Gain = 1.0

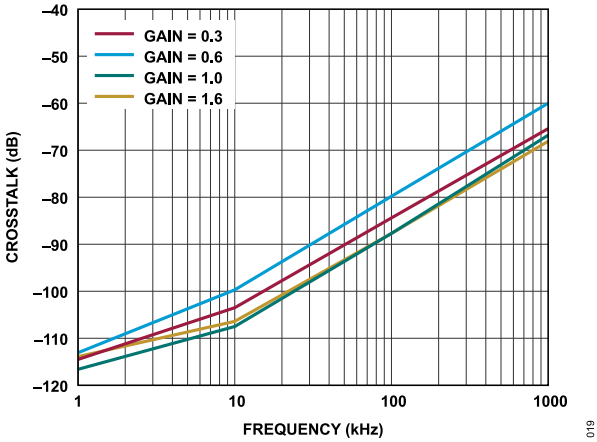

Figure 14. Channel-to-Channel Isolation vs. Frequency

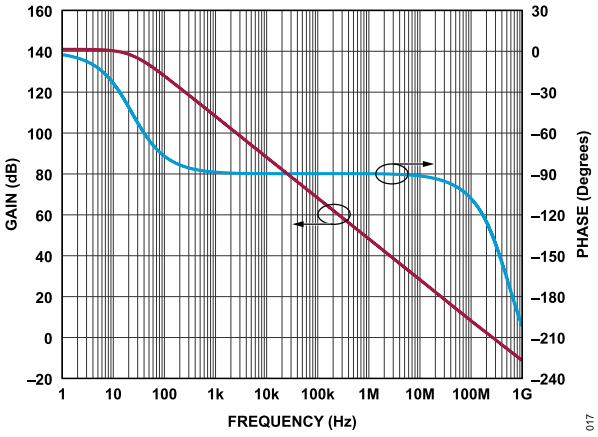

Figure 12. ADC Driver Open-Loop Gain and Phase vs. Frequency

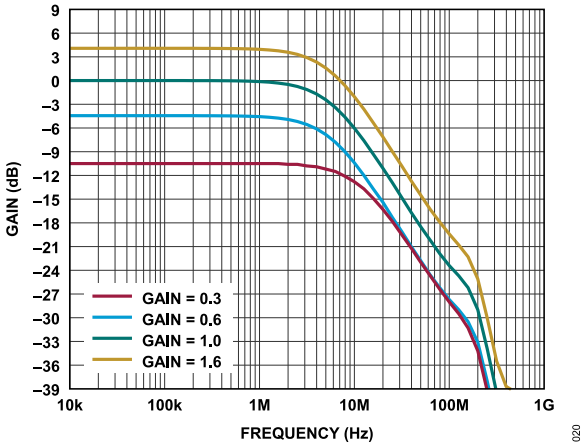

Figure 15. ADC Driver Closed-Loop Gain vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

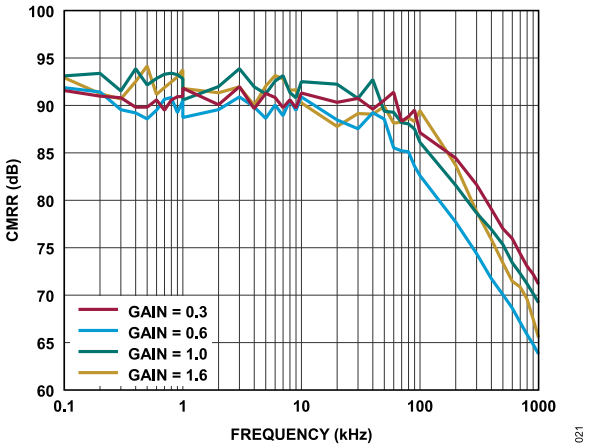

Figure 16. CMRR vs. Frequency

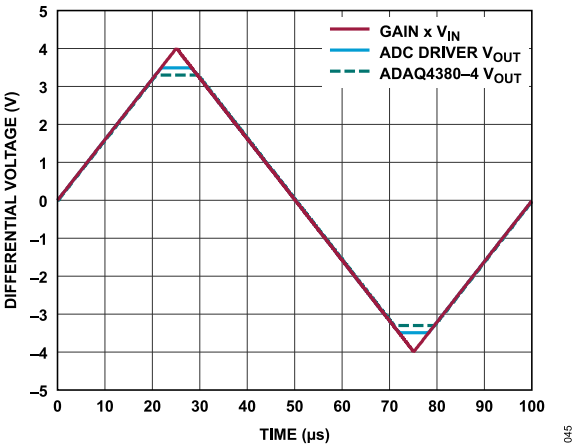

Figure 19. Output Overdrive Recovery, Gain = 0.6

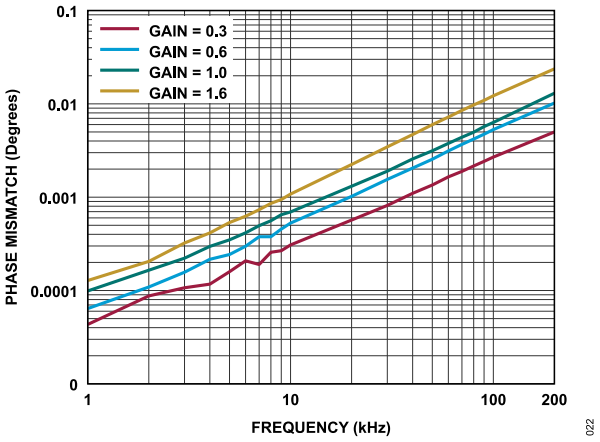

Figure 17. Channel-to-Channel Phase Matching vs. Frequency

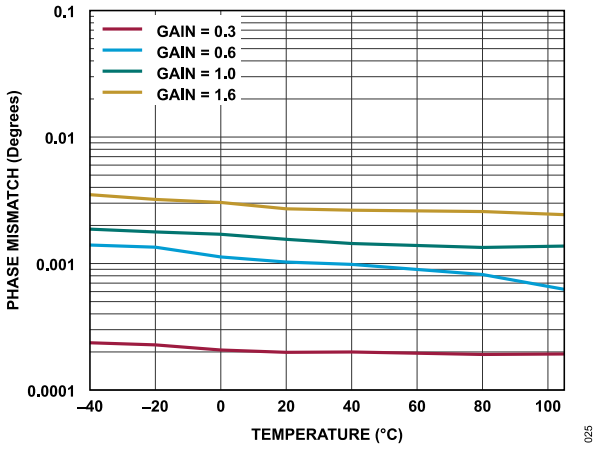

Figure 18. Channel-to-Channel Phase Matching vs. Temperature, f_{IN} = 20 kHz

TERMINOLOGY

Differential Voltage

Differential voltage is the difference between two node voltages. For example, the differential input voltage (or equivalently, input differential mode voltage) is defined as:

$$V_{IN,dm} = V_{AINA+} - V_{AINA-} \quad (1)$$

where:

V_{AINA+} and V_{AINA-} refer to the voltages at the AINA+ and AINA- terminals with respect to a common reference.

Common-Mode Voltage (CMV)

Common-Mode Voltage is the average of two node voltages. The input common-mode voltage is defined as:

$$V_{IN,cm} = (V_{AINA+} + V_{AINA-})/2 \quad (2)$$

Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The first transition occurs at a level ½ LSB above analog ground. Offset error is the difference between the ideal mid-scale input voltage (0 V), and the actual voltage producing the mid-scale output code.

Offset Error Drift

Offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full-scale code range. Offset error drift is expressed in parts per million per degree Celsius (ppm/°C) as follows:

$$Offset\ Error\ Drift(ppm/℃) = 10^6 \times (Offset\ Error\_T_{MAX} - Offset\ Error\_T_{MIN}) / (T_{MAX} - T_{MIN}) \quad (3)$$

where:

T_{MAX} = 105°C.

T_{MIN} = −40°C.

Gain Error

The first transition (from 100…000 to 100…001) should occur at a level ½ LSB above nominal negative full scale. The last transition (from 011…110 to 011…111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels. Gain error is expressed as a percentage as follows:

$$Gain\ Error(\%) = 100\times((PFS - NFS)_{ACTUAL\_CODE} - (PFS - NFS)_{IDEAL\_CODE}) /((\mathrm{PFS} - \mathrm{NFS})_{\mathrm{IDEAL\_CODE}}) \quad (4)$$

where:

PFS is positive full scale.

NFS is positive full scale.

Gain Error Drift

The gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range. Gain error drift is expressed in parts per million per degree Celsius (ppm/°C) as follows:

$$Gain\ Error\ Drift(ppm/℃) = 10^6 \times (Gain\ Error\_T_{MAX} - Gain\ Error\_T_{MIN}) / (T_{MAX} - T_{MIN}) \quad (5)$$

where:

T_{MAX} = 105°C.

T_{MIN} = −40°C.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

TERMINOLOGY

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Temperature Coefficient (TCV_{OUT})

The temperature coefficient relates the change in the output voltage to the change in the ambient temperature of the device, as normalized by the output voltage at 25°C. This parameter is specified using box method.

$$TCV_{OUT} = \left[\frac{max\{V_{OUT}\ (T_1, T_2, T_3)\} - min\{V_{OUT}\ (T_1, T_2, T_3)\}}{V_{OUT}(T_2)\ \times\ (T_3\ -\ T_1)}\right] \times 10^6 \quad (6)$$

where:

TCV_{OUT} is expressed in ppm/°C.

$V_{OUT}(T_X)$ is the output voltage at Temperature T_X.

T_1 = -40 °C.

T_2 = +25 °C.

T_3 = +105 °C.

Long-Term Drift (ΔV_{OUT_LTD})

Long-term drift refers to the shift in the output voltage versus time. This is expressed as a difference in ppm from the nominal output.

$$\Delta V_{OUT\_LTD} = \left[\frac{V_{OUT}(t_1) - V_{OUT}(t_0)}{V_{OUT}(t_0)}\right] \times 10^6 \quad (7)$$

where:

ΔV_{OUT_LTD} is expressed in ppm.

$V_{OUT}(t_0)$ is the output voltage at the starting time of the measurement.

$V_{OUT}(t_1)$ is the output voltage at the end time of the measurement.

Thermal Hysteresis (ΔV_{OUT_HYS})

Thermal hysteresis represents the change in the output voltage after the device is exposed to a specified temperature cycle. This is expressed as a difference in ppm from the nominal output.

$$\Delta V_{OUT\_HYS} = \left[\frac{V_{OUT1\_25°C} - V_{OUT2\_25°C}}{V_{OUT1\_25°C}}\right] \times 10^6 \quad (8)$$

where:

ΔV_{OUT_HYS} is expressed in ppm.

$V_{OUT1\_25°C}$ is the output voltage at 25 °C.

$V_{OUT2\_25°C}$ is the output voltage after temperature cycling.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in µModule output at the frequency, f, to the power of a 100 mV p-p sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR(dB) = 10\log\left(P_{\mu Module\_IN}/P_{\mu Module\_OUT}\right) \quad (9)$$

where:

$P_{\mu Module\_IN}$ is the common-mode power at the frequency, f, applied to the inputs.

$P_{\mu Module\_OUT}$ is the power at the frequency, f, in the µModule output.

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 500 mV p-p sine wave applied to the VS+, REFIN, and IN_LDO supply voltage centered at 5 V of frequency, f.

$$PSRR\ (dB) = 10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT}) \quad (10)$$

where:

$P_{\mu Module\_IN}$ is the power at the frequency,f, at the VS+, REFIN, and IN_LDO pins.

$P_{\mu Module\_OUT}$ is the power at the frequency,f, at the µModule output.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the input and when the input signal is held for a conversion.

Aperture Jitter

Aperture jitter is the variation in aperture delay.

THEORY OF OPERATION

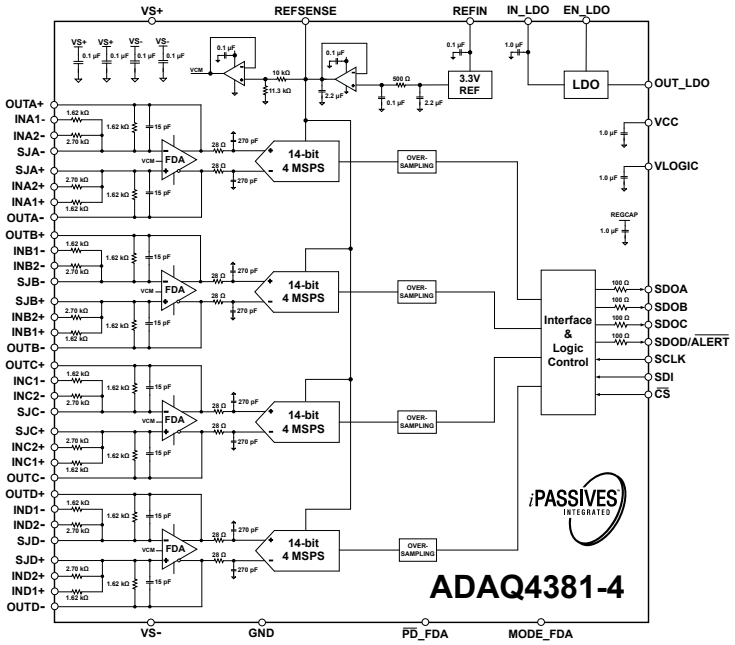

Figure 20. ADAQ4381-4 µModule® Simplified Block Diagram

CIRCUIT INFORMATION

The ADAQ4381-4 µModule® system in package (SiP) is a quad, high speed, precision data acquisition (DAQ) signal chain that uses a simultaneous sampling SAR architecture. As shown in Figure 20, the ADAQ4381-4 µModule® DAQ system is consist of a quad 14-bit SAR ADC, wide bandwidth, fully differential ADC driver, a precision low noise 3.3V reference, low noise and stable reference buffers, and a 3.4V LDO, along with critical precision passive components required to achieve optimal performance with pin selectable gain options of 0.3, 0.6, 1.0, and 1.6. All active components in the circuit, including *i*Passives® thin film resistors with ±0.005% matching, are designed by Analog Devices, Inc. and are factory calibrated to achieve a high degree of specified accuracy and minimize temperature dependent error sources.

The ADAQ4381-4 simultaneously convert all the channels with a high throughput rate of 4 MSPS. The ADAQ4381-4 has an integrated on-chip oversampling blocks to further improve the dynamic range and reduce noise at lower bandwidths. See ADC Modes of Operation section for details. All the decoupling capacitors required by the ADC's voltage pins are all included inside the BGA package. Any external capacitors won't be necessary.

Table 8. LSB Size

Resolution	3.3 V Reference	Units
14-bit	402.8	µV
16-bit	100.7	µV

TRANSFER FUNCTION

ADAQ4381-4 uses an internal 3.3 V reference. The ADAQ4381-4 converts the differential voltage of the analog inputs (IN_X+ and IN_X-) into a digital output.

The conversion result is MSB first, twos complement. The LSB size is (2 x V_{REF}) / 2^N, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen, and if resolution boost mode is enabled. Table 8 outlines the LSB size expressed in volts for different resolutions.

The ideal transfer characteristic of the ADAQ4381-4 is shown in Figure 21.

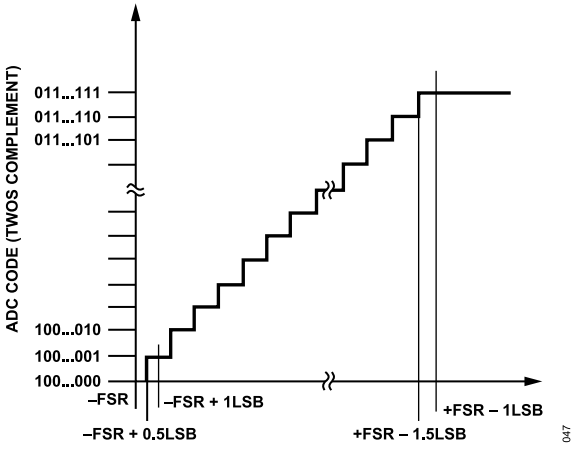

Figure 21. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAMS

Figure 22 to Figure 29 show the typical connections diagram for each channel of ADAQ4381-4 when applying differential, or single-ended input signals on four gain settings/combinations with varying common-mode voltage.

The four differential channels of the ADAQ4381-4 can accept wide input voltage range and has a wide common-mode range that allows to convert a variety of signals. Differential and Common-mode Voltage ranges are highly dependent with the gain configuration per channel.

Table 9. Gain Configurations and Input Range

Gain	Input Range	Input Signal on Pins	Test Conditions
0.3	±11 V	IN2+, IN2-	Connect IN1+ to OUT-, and IN1- to OUT+. See Figure 22 and Figure 26.
0.6	±5.5 V	IN2+, IN2-	Connect IN1+, IN1-. Leave OUT+ and OUT- floating. See Figure 23 and Figure 27.
1.0	±3.3 V	IN1+, IN1-	Leave IN2+, IN2-. OUT+ and OUT- floating. See Figure 24 and Figure 28.
1.6	±2.06 V	IN1+ or IN2+, IN1- or IN2-	Connect IN1+ to IN2+, and IN1- to IN2-. Leave OUT+ and OUT- floating. See Figure 25 and Figure 29.

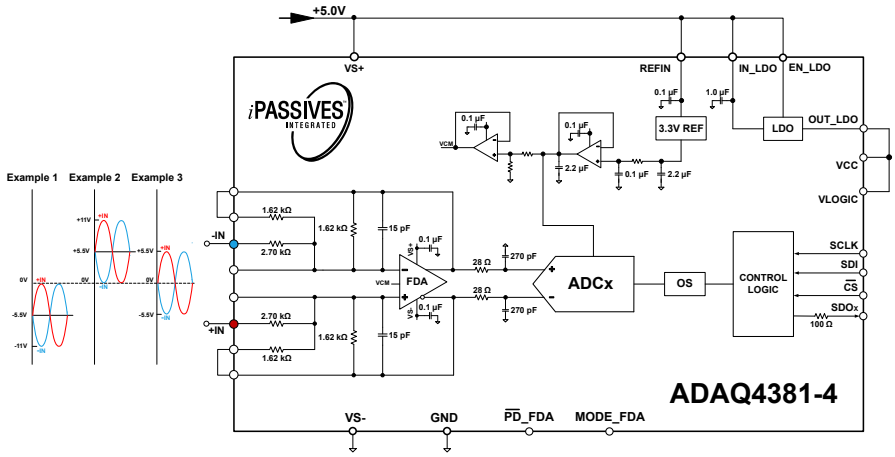

Figure 22. Fully Differential Input Configuration with Gain=0.3, ±11V Input

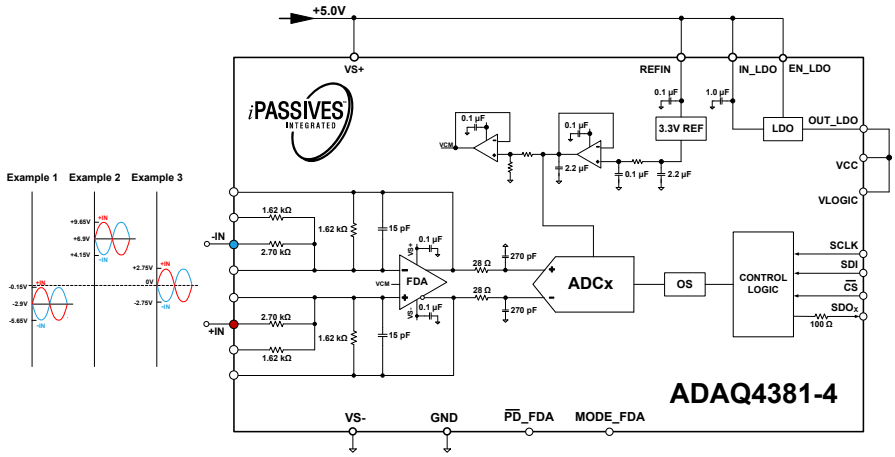

Figure 23. Fully Differential Input Configuration with Gain=0.6, ±5.5V Input

APPLICATIONS INFORMATION

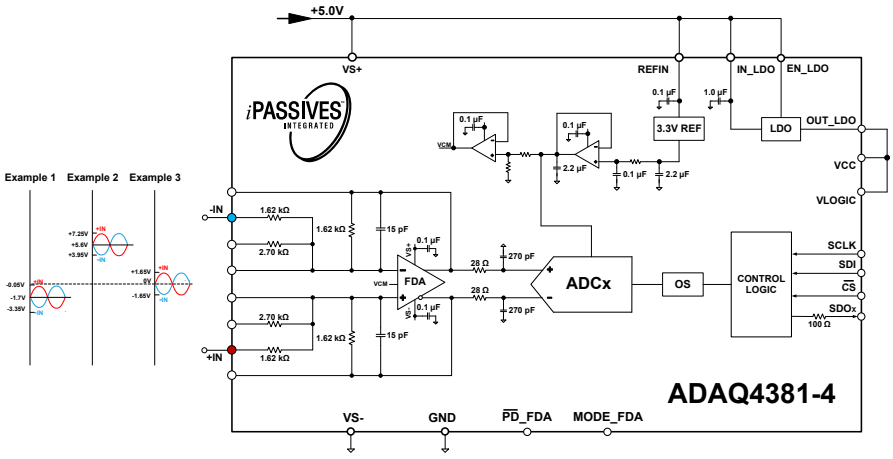

Figure 24. Fully Differential Input Configuration with Gain=1.0, ±3.3V Input

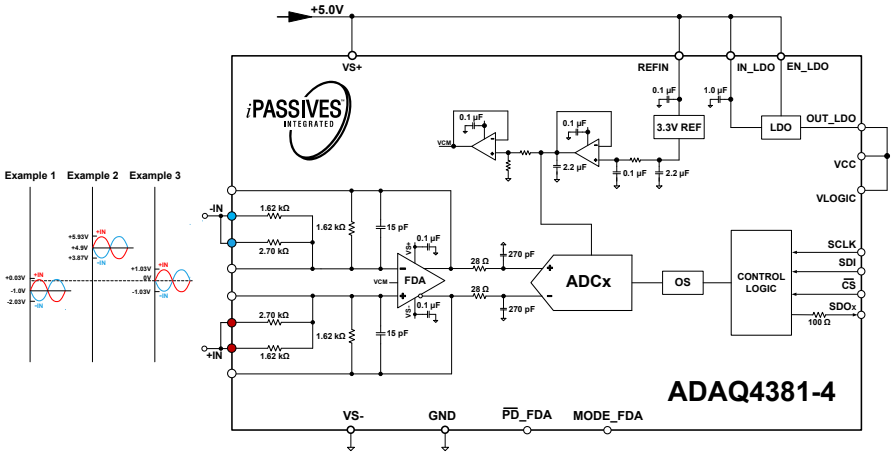

Figure 25. Fully Differential Input Configuration with Gain=1.6, ±2.06V Input

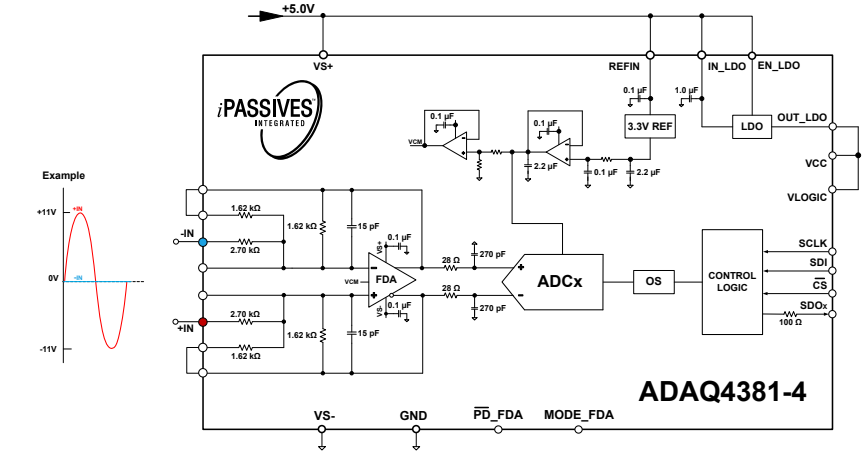

Figure 26. Single-Ended Input Configuration with Gain=0.3, ±11V Input

APPLICATIONS INFORMATION

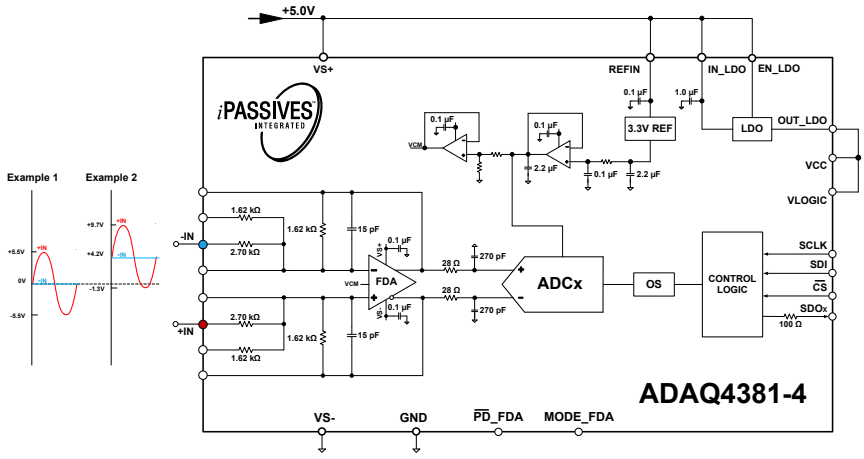

Figure 27. Single-Ended Input Configuration with Gain=0.6, ±5.5V Input

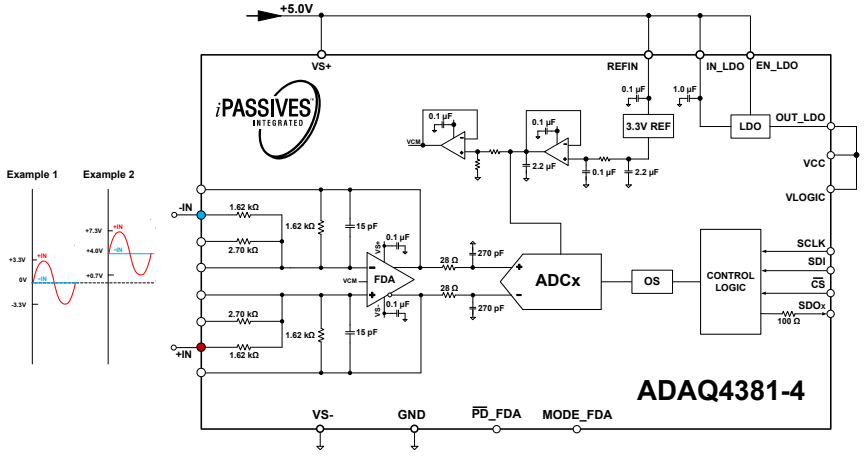

Figure 28. Single-Ended Input Configuration with Gain=1.0, ±3.3V Input

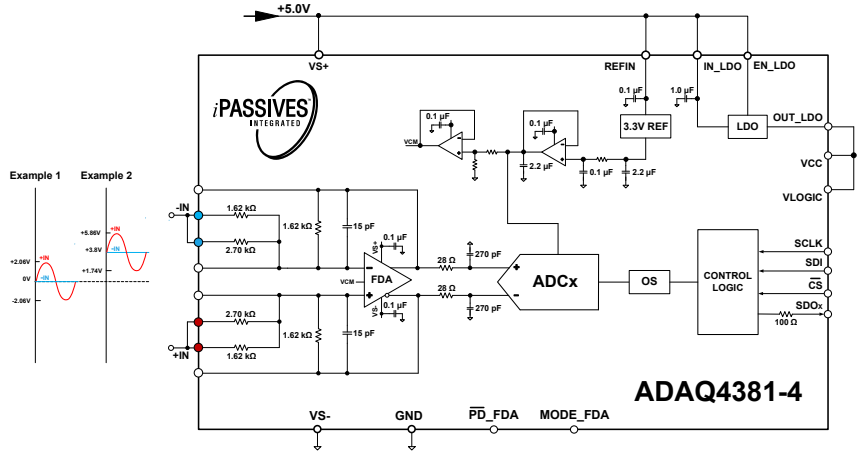

Figure 29. Single-Ended Input Configuration with Gain=1.6, ±2.06V Input

APPLICATIONS INFORMATION

ADC DRIVER

Integrated in the ADAQ4381-4 µModule are four low noise, fully differential amplifiers as ADC drivers and their respective gain network passives. These ADC drivers have two power modes, full power and low power mode. In full power mode, ADAQ4381-4 is at optimum performance with slightly higher power consumption. At low power mode, ADAQ4381-4 consumes 20% less power but with a lower SNR(~ 0.6 dB at G = 1). The power mode options allow the users to operate the ADAQ4381-4 based on the application requirements on noise and power consumption.

Input Common-Mode Voltage

The input common-mode voltage range (ICMVR) of ADAQ4381-4 is highly dependent on the gain of the ADC drivers. Gain setting and gain options are detailed in Table 9. Each gain has different ICMVR to cater a wide range of input voltage at the front-end. Aside from the absolute differential input voltage, input common-mode voltage should be taken into consideration for proper operation. Figure 30 and Figure 31 shows the ICMVR of ADAQ4381-4 for G = 0.3 and G = 1, respectively.

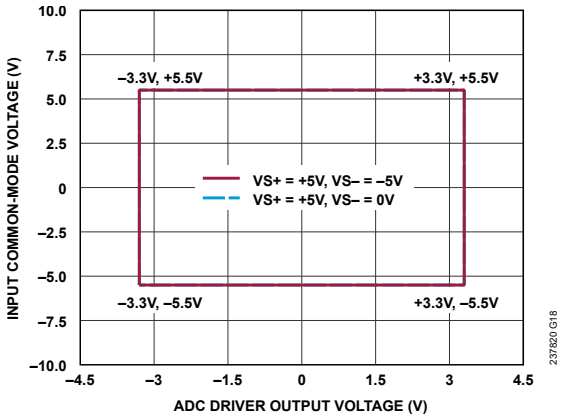

Figure 30. Input Common-Mode Voltage vs. ADC Driver Output, Gain = 0.3, ±11 V Differential Input

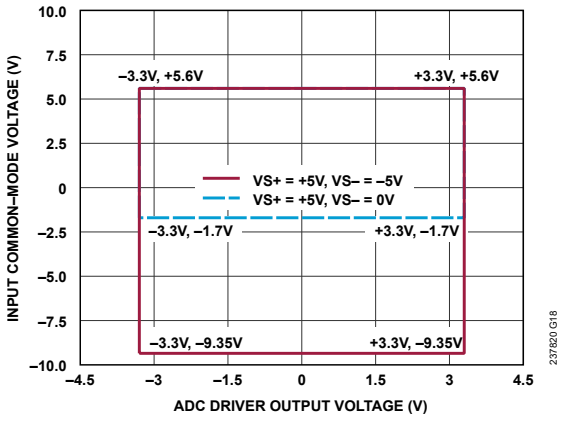

Figure 31. Input Common-Mode Voltage vs. ADC Driver Output, Gain = 1.0, ±3.3 V Differential Input

Calculating the input impedance of the application circuit

The effective input impedance depends on whether the signal source is single-ended or differential. For a balanced differential input signal, as shown in Figure 32, the input impedance ($R_{IN, dm}$) between the inputs (IN+ and IN-) is $R_{IN,dm} = 2 \times R_G$.

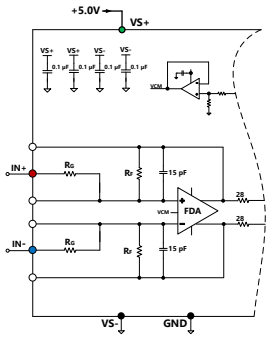

Figure 32. ADAQ4381-4 Configured at Fully Differential Inputs

For a single-ended input signal, as shown in Figure 33, the input impedance is:

$$R_{IN,SE} = \frac{R_G}{1 - \frac{R_F}{2(R_G + R_F)}} \quad (11)$$

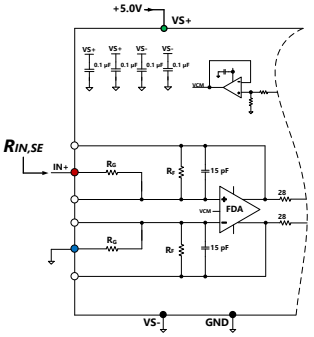

Figure 33. ADAQ4381-4 Configured at Single-Ended Inputs

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the R_G input resistor.

Terminating a Single-Ended Input

When the circuitry driving the inputs has a very low output impedance, there is no need for an additional termination on the IN+ and IN- inputs of ADAQ4381-4. However, when there is a considerable amount of resistance from the driving circuity, we recommend that a balancing network should be added on the inputs of ADAQ4381-4. Kindly refer to AN-1026 for techniques on how to properly terminate the inputs for a single-ended input operation.

APPLICATIONS INFORMATION

INTERNAL REFERENCE

The ADAQ4381-4 µModule has an internal precision voltage reference that offers high accuracy, low noise, and low drift (3 ppm/°C typical). Connect REFIN to a clean 5 V supply to ensure optimum performance. Bypass and load capacitors for stability are already included inside the µModule package, therefore external capacitors are not necessary. The 3.3 V output of this reference is utilized as the ADC reference, and VCM for ADC Drivers.

REFSENSE pin is part of the internal reference circuitry. It is connected directly to the ADC reference input and reference buffer's output. Using the REFSENSE pin as a reference or a voltage source for another part of the system is not recommended, and may degrade the ADAQ4381-4 performance. Use this pin for accurate gain calibration only, otherwise do not connect.

Long-Term Drift

To determine the long-term drift of the ADAQ4381-4 internal reference, the change in output voltage of multiple units are measured for more than 1000 hours. The drift data is taken on 19 parts that are soldered onto FR4 PCB using a standard reflow profile to replicate real-world system applications. The boards are then soaked in an ultrastable oil bath with a controlled constant temperature of 25°C, the outputs are scanned regularly and measured using a high precision measurement system.

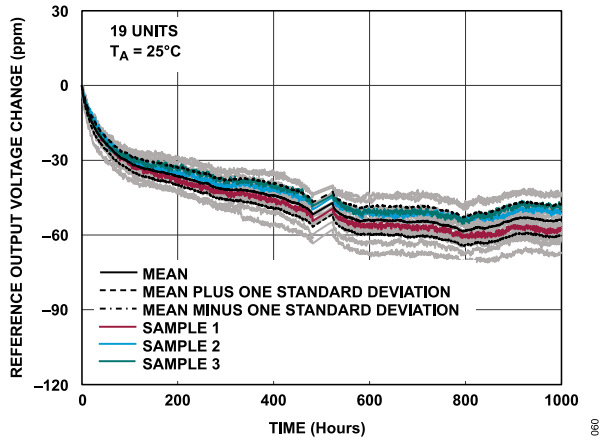

Figure 34. ADAQ4381-4 Internal Reference Long-Term Drift

Figure 34 shows the long-term drift of the ADAQ4381-4 internal 3.3 V reference, output voltage drift of 54 ppm after 800 hours. Drastic shift on the output voltage is observed from 0 hours to 250 hours, as shown in Figure 35. With a mean drift of 39 ppm, early life drift account for 72% of the total drift observed within 1000 hours.

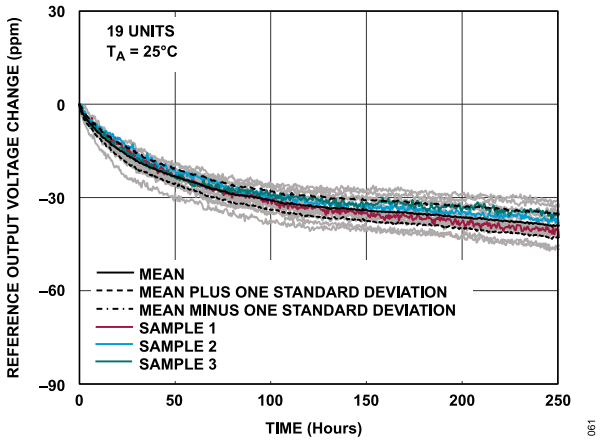

Figure 35. ADAQ4381-4 Internal Reference Early Life Drift

Thermal Hysteresis

In addition to stability over time, as described in the Long-Term Drift section, it is useful to know the thermal hysteresis, that is, the stability vs. cycling of temperature. Thermal hysteresis tells how closely the signal returns to its starting amplitude after the ambient temperature changes and the subsequent return to room temperature.

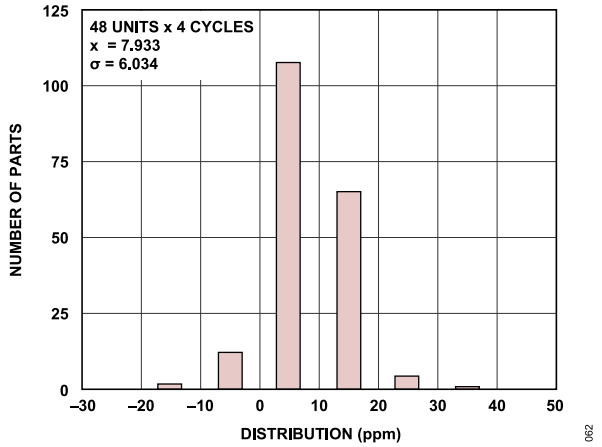

Figure 36. Reference Output Voltage Hysteresis at Four Full Cycles

Figure 36 shows the hysteresis when the part is subjected to a full temperature cycles four times from room temperature to −40°C to +105°C and back to room temperature. In four full cycles, the output hysteresis is typically 8 ppm. The histogram in Figure 37 shows that the hysteresis is larger when the device cycles through only a half cycle, from room temperature to 105°C and back to room temperature, typically −50 ppm, and from room temperature to −40°C and back to room temperature, typically 43 ppm.

APPLICATIONS INFORMATION

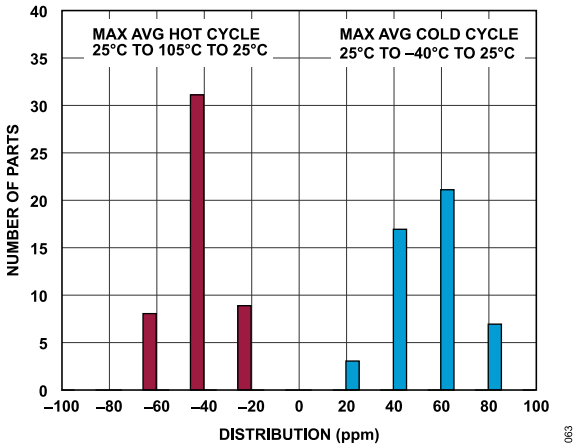

Figure 37. Reference Output Voltage Hysteresis at Half Cycles

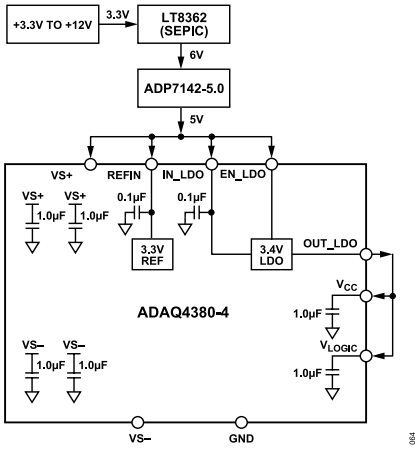

Figure 38. ADAQ4381-4 Power Supply Recommendations

INTERNAL LDO

The ADAQ4381-4 µModule has an internal LDO regulator. To use this, connect IN_LDO and EN_LDO to 5 V. Input bypass capacitors are already integrated within the µModule, external bypass capacitors are not necessary. The output of this LDO is intended to power the ADC VCC and VLOGIC supply rails. During normal operation, connect VCC and VLOGIC directly to OUT_LDO, no need for external capacitors. If applications require external supplies for VCC and VLOGIC, disable the internal LDO by connecting EN_LDO to GND.

POWER SUPPLY AND DECOUPLING

The ADAQ4381-4 has six independent power supplies, VS+, VS−, REFIN, IN_LDO, VCC, and VLOGIC that supply the analog circuitry and digital interface, respectively. For the detailed description of each supply pins, see Table 7. The ADAQ4381-4 is guaranteed to achieve its optimum performance at single, 5 V supply operation. Decoupling these supply pins may not be necessary since decoupling capacitors are already integrated in the ADAQ4381-4 internal circuitry. Additionally, the ADAQ4381-4 features an internal reference and reference buffer decoupled to ground. There is no need to add external decoupling caps on the REFSENSE pin.

Figure 38 shows the recommended power companion products for the ADAQ4381-4. For more details, refer to the ADAQ4381-4 LTPower Planner in the product website.

Power-up

Care must be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The ADAQ4381-4 is not easily damaged by power supply sequence, Figure 38 shows the recommended power supply utilizing the internal LDO to power up VCC and VLOGIC. Although the ADAQ4381-4 is robust to power supply sequencing, if applications would require an external VCC and VLOGIC, the best sequence is to power VCC and VLOGIC first, followed by VS+ and VS- and lastly with REFIN. Between VCC and VLOGIC, either can be powered up first. Analog and digital signals must be applied after the reference is applied.

The ADAQ4381-4 require a $t_{POWER-UP}$ time from applying VCC and VLOGIC until the ADC conversion results are stable. For the recommended signal condition during power-up, see Figure 4. It is recommended to pull the pin high during power-up and have a software reset after the power-up. Conversion results are not guaranteed to meet data sheet specifications during this time and must be ignored.

ADC MODES OF OPERATION

The ADAQ4381-4 have several on-chip configuration registers for controlling the operational mode of the device.

OVERSAMPLING

Oversampling is a common method used in signal processing to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC) of the ADC. The ADAQ4381-4 offer an oversampling function on-chip and have two user configurable oversampling modes: normal averaging and rolling averaging.

The oversampling functionality is configured by programming the OS_MODE bit and OSR bits in the Configuration1 Register .

Normal Average Oversampling

Normal average oversampling mode can be used in applications where slower output data rates are needed and where higher SNR or dynamic range is desirable. Normal averaging involves taking a number of samples, adding them together and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared after the process is completed.

Normal average oversampling mode is configured by setting the OS_MODE bit to logic 0 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR.

Table 10 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 14-bit resolution. If additional resolution is required, this can be achieved by configuring the resolution boost bit (RES) in the Configuration1 Register . See the Resolution Boost section for further details.

The number of samples (n), defined by the OSR bits, are taken and added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$, and the ADAQ4381-4 controls all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples at the devices maximum sampling rate is 4 MSPS. The data is ready for readback on the next serial interface access. After the averaging technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and initiates by the falling edge of $\overline{CS}$.

As the output data rate is reduced by the oversampling ratio, the SPI frequency required to transmit the data is also reduced accordingly.

Table 10. Normal Average Oversampling Overview, G = 1

OSR [2:0]	OS Ratio	SNR (dB typical) with V_{REF} = 3.3 V Internal		Data Output Rate (kSPS max)
		RES = 0	RES =1	
000	No OS	84	84	4000
001	2	84	87	1250
010	4	84	90	625
011	8	84	92	312.5
100	16	TBD	TBD	156.25
101	32	TBD	TBD	78.125
110	Invalid	Not Applicable	Not Applicable	Not Applicable
111	Invalid	Not Applicable	Not Applicable	Not Applicable

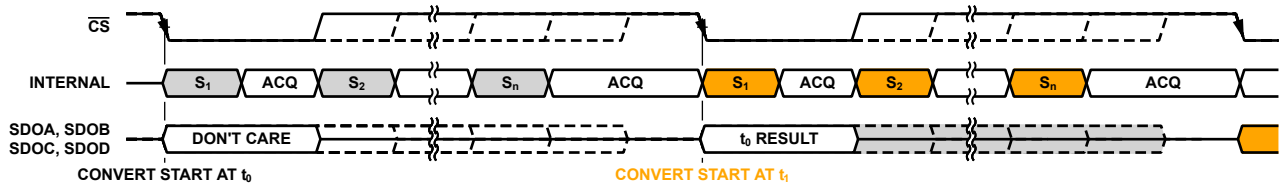

Figure 39. Normal Average Oversampling Operation

ADC MODES OF OPERATION

Rolling Average Oversampling

Rolling average oversampling mode can be used in applications where higher output data rates are required and where a higher SNR or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding them together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared when the process completes. The rolling oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling average oversampling mode is configured by setting the OS_MODE bit to logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 11).

Table 11 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the ADAQ4381-4. If additional resolution is required this can be achieved by configuring the resolution boost bit in the Configuration1 Register . See Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. When a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8 regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on-reset (POR), on the first conversion after a software controlled hard or soft reset. A new conversion result is shifted into the FIFO on completion of every ADC conversion regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, *n*, defined by the OSR bits are taken from the FIFO, added together and the result is divided by *n*.

Table 11. Rolling Average Oversampling Overview, G = 1

OSR [2:0]	OS Ratio	SNR (dB typical)		Data Output Rate (kSPS max)
		RES = 0	RES =1	
000	No OS	84	84	4000
001	2	84	87	4000
010	4	84	90	4000
011	8	84	92	4000
110	Invalid	Not Applicable	Not Applicable	Not Applicable
111	Invalid	Not Applicable	Not Applicable	Not Applicable

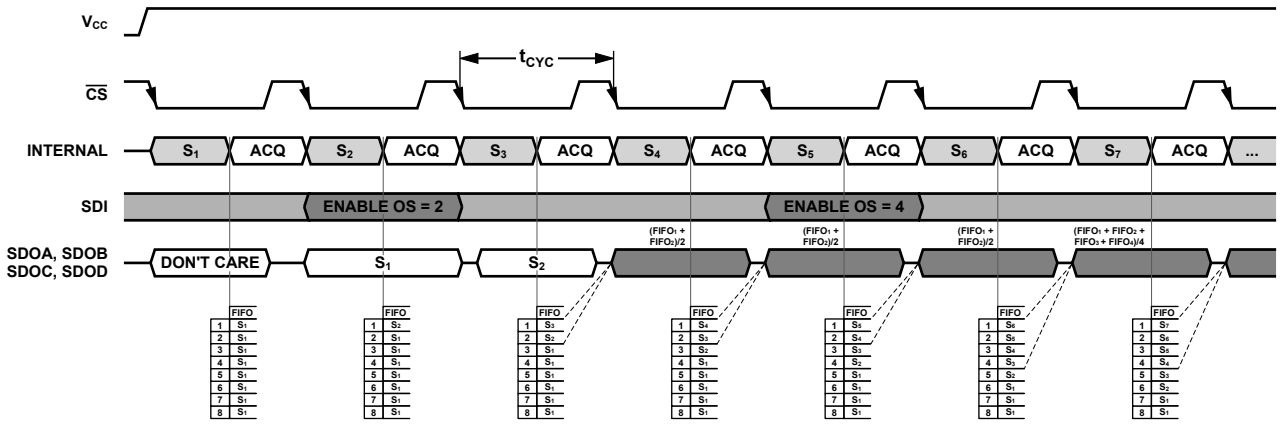

Figure 40. Rolling Average Oversampling Mode Operation

ADC MODES OF OPERATION

RESOLUTION BOOST

The default resolution and output data size for the ADAQ4381-4 is 14 bits. When the on-chip oversampling function is enabled the performance of the ADC can exceed the default resolution. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the Configuration1 Register is set to logic 1 and the ADAQ4381-4 is in a valid oversampling mode, the conversion result size for the ADAQ4381-4 is 16 bits. In this mode, 16 SCLK cycles are required to propagate the data for the ADAQ4381-4.

ALERT

The alert functionality is an out-of-range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the value in the conversion result register exceeds the alert high limit value in the Alert High Threshold Register or falls below the alert low limit value in the Alert Low Threshold Register. The Alert High Threshold Register and the Alert Low Threshold Register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the Alert Indication Register.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOD/$\overline{\text{ALERT}}$ pin. The SDOD/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the Configuration1 Register and the Configuration2 Register registers:

- Set the SDO bits to any value other than 0b10.
- Set the ALERT_EN bit to 1.
- Set a valid value in the alert high threshold register and the alert low threshold register.

The alert indication function is available in oversampling (rolling averaging, normal averaging, and in non-oversampling modes).

The alert function of the SDOD/$\overline{\text{ALERT}}$ pin updates at the end of conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register are updated as well and must be read before the end of next conversion.

Bits [7:0] in the alert indication register are cleared by reading the alert register contents. The alert function of the SDOD/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the alert indication register.

See Figure 8 for the $\overline{\text{ALERT}}$ timing diagram.

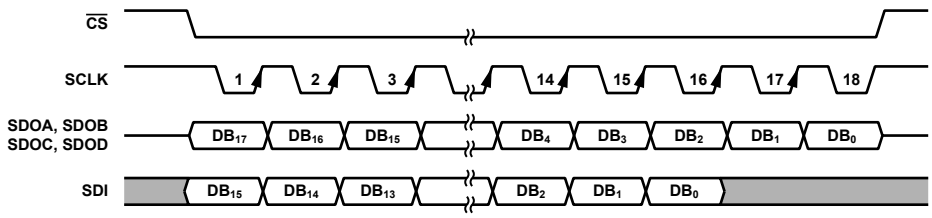

Figure 41. Resolution Boost

ADC MODES OF OPERATION

POWER MODES

The ADAQ4381-4 has two power modes that can be set in the Configuration1 Register : normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the Configuration1 Register to configure the power modes in the ADAQ4381-4. Set PMODE to logic 0 for normal mode and logic 1 for shutdown mode.

Normal Mode

Keep the ADAQ4381-4 in normal mode to achieve the fastest throughput rate. All ADC blocks always remain fully powered and an ADC conversion can be initiated by a falling edge of $\overline{CS}$ when required. When the ADAQ4381-4 is not converting, it is in static mode and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption of the ADAQ4381-4 scales with throughput.

Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the ADAQ4381-4 is in shutdown mode, all analog circuitry powers down. The serial interface remains active during shutdown mode to allow the ADAQ4381-4 to exit shutdown mode.

To enter shutdown mode, write to the power mode configuration bit, PMODE, in the Configuration1 Register .

The ADAQ4381-4 shuts down and current consumption reduces. To exit shutdown mode and return to normal mode set the PMODE bit in the Configuration1 Register to logic 0.

All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode sufficient time has to be allowed for the circuitry to turn on before starting a conversion, see Figure 42.

SOFTWARE RESET

The ADAQ4381-4 has two reset modes: a soft reset and a hard reset. A reset is initiated by writing to the reset bits in the Configuration2 Register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The register is cleared. The reference and LDO remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

DIAGNOSTIC SELF-TEST

The ADAQ4381-4 run a diagnostic self-test after a POR or after a software hard reset to ensure correct configuration is loaded into the device.

The result of the self-test is displayed in the SETUP_F bit in the Alert Indication Register. If the SETUP_F bit is set to logic 1, the diagnostic self-test has failed. If the test fails, perform a software hard reset to reset the ADAQ4381-4 registers to the default status.

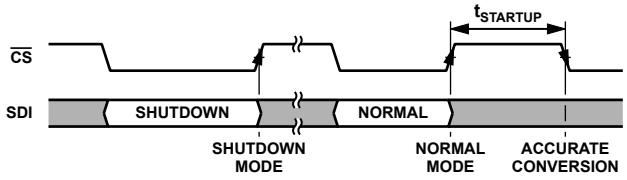

Figure 42. Shutdown Mode Operation

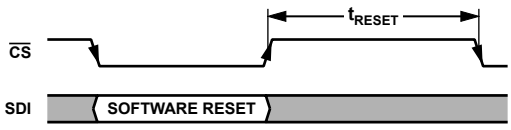

Figure 43. Software Reset Operation

INTERFACE

The interface to the ADAQ4381-4 is via a serial interface. The interface consists of a $\overline{CS}$, SCLK, SDOA, SDOB, SDOC and SDOD, and SDI. When referencing a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed, such as SDOD. For full pin names of multifunction pins, refer to the Pin Configurations and Function Descriptions section.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled and the bus is taken out of three-state. The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, SDOC, SDOD, and SDI signals. A minimum of 14 SCLK cycles are required for a write to or read from a register. The minimum numbers of SCLK cycles for a conversion read is dependent on the resolution of the device and the configuration settings, see Table 12.

The ADAQ4381-4 has four serial output signals: SDOA SDOB, SDOC, and SDOD. Programming the SDO bits in the Configuration2 Register configures 2-wire, 1-wire, or 4-wire mode. To achieve the highest throughput of the device, it is required to use either the 2-wire or 4-wire mode to read conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results.

Configuring cyclic redundancy check (CRC) operation for SPI reads, SPI writes and over sampling mode with resolution boost mode enabled will alter the operation of the interface. Refer to the CRC section to ensure correct operation.

READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the signal initiates a simultaneous conversion of the four ADCs: ADC A, ADC B, ADC C and ADC D. The ADAQ4381-4 has a one cycle read back latency. Therefore, the conversion results are available on the next SPI access. Then, take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial output pins. The next conversion is also initiated at this point.

The conversion result is shifted out of the device as a 14-bit result for the ADAQ4381-4. The MSB of the conversion result is shifted out on the $\overline{CS}$ falling edge. The remaining data is shifted out of the device under the control of the serial clock (SCLK) input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the serial data output pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDO pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled, see Figure 44 and Table 12 for details. If CRC reading is enabled, additional SCLK pulses are required to propagate the CRC information. See the CRC section for more details.

Because the $\overline{CS}$ signal initiates a conversion as well as framing the data, any data access must be completed within a single frame.

Table 12. Number of SCLK cycles (n) required for Reading Conversion Results

Interface Configuration	Resolution Boost Mode	CRC Read	No. of SCLK Cycles
4-Wire	Disabled	Disabled	14
		Enabled	22
	Enabled	Disabled	16
		Enabled	24
2-Wire	Disabled	Disabled	28
		Enabled	36
	Enabled	Disabled	32
		Enabled	40
1-Wire	Disabled	Disabled	56
		Enabled	64
	Enabled	Disabled	64
		Enabled	72

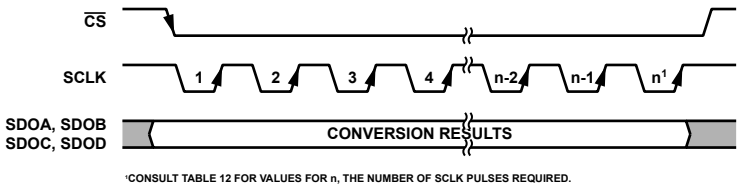

Figure 44. Reading Conversion Results

INTERFACE

Serial 4-Wire Mode

Configure 4-wire mode by setting the SDO bits to 0b10 in the Configuration2 Register. In 4-wire mode, the conversion results for ADC A is output on SDOA, ADC B on SDOB, ADC C on SDOC, and ADC D on SDOD.

Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bits to 0b00 in the Configuration2 Register. In 2-wire mode the conversion results for ADC A and ADC C are output on SDOA. The conversion result for ADC B and ADC D are output on SDOB.

Serial 1-Wire Mode

In applications where slower throughput rates are allowed or normal averaging oversampling is used the serial interface can be configured to operate in 1-wire mode. In 1-wire mode the conversion results from ADC A, ADC B, ADC C, and ADC D are output on SDOA. Additional SCLK cycles are required to propagate all the data. ADC A data is output first followed by ADC B, ADC C, and ADC D conversion results.

LOW LATENCY READBACK

The interface on the ADAQ4381-4 has a one cycle latency as shown in Figure 45. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. After the conversion time, $t_{CONVERT}$, elapses, a second $\overline{CS}$ pulse after the initial $\overline{CS}$ pulse that initiated the conversion can be used to readback the conversion result. This operation is shown in Figure 48.

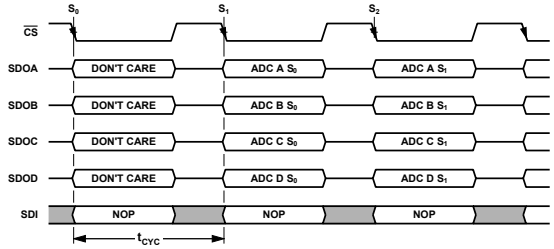

Figure 45. Read Conversion Results, 4-Wire Mode

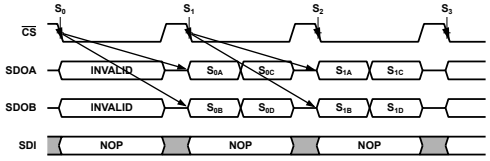

Figure 46. Reading Conversion Results, 2-Wire Mode

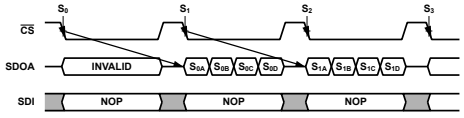

Figure 47. Read Conversion Results, 1-Wire Mode

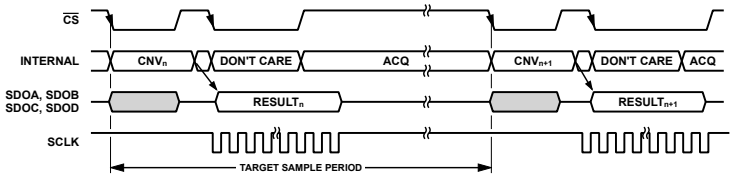

Figure 48. Low Throughput Low Latency

INTERFACE

READING FROM DEVICE REGISTERS

All registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation command (NOP). The format for a read command is shown in Table 15. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], are ignored.

WRITING TO DEVICE REGISTERS

All the read/write registers in the ADAQ4381-4 can be written to over the serial interface. The length of a SPI write access is determined by the CRC write function. An SPI access is 16 bits if CRC write is disabled and 24-bit when CRC write is enabled. The format for a write command is shown in Table 15. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register.

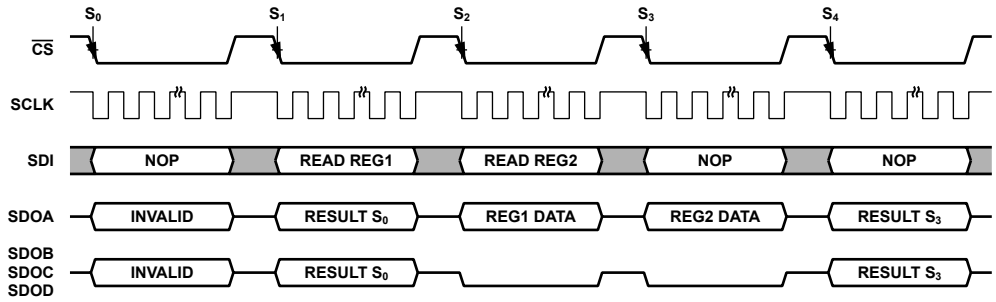

Figure 49. Register Read

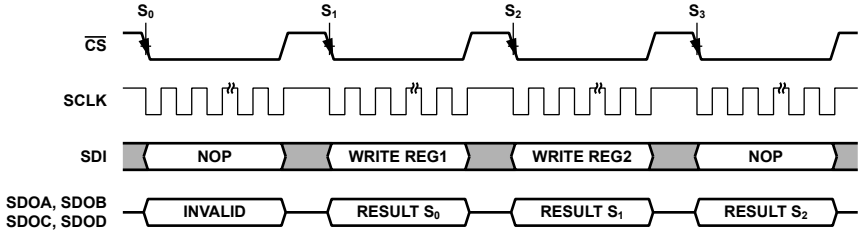

Figure 50. Register Write

INTERFACE

CRC

The ADAQ4381-4 CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and SPI interface writes. For example, enable the CRC function for SPI writes to prevent unexpected changes to the device configuration but not enable it on SPI reads to maintain a higher throughput rate. The CRC feature is controlled by programming of the CRC_W bit and CRC_R bit in the Configuration1 Register .

CRC Read

If enabled, a CRC consisting of an 8-bit word is appended to the conversion result or register reads. The CRC is calculated on the conversion result for ADC A, ADC B, ADC C, and ADC D and, is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 1-wire SPI mode, 2-wire SPI mode, 4-wire SPI mode and resolution boost mode.

CRC Write

To enable the CRC write function, the CRC_W bit in the Configuration1 Register register must be set to 1. To set the CRC_W bit to 1 to enable the CRC feature, a valid CRC must be appended to the request frame.

After the CRC feature is enabled, all register write requests are ignored unless they are accompanied by a valid CRC command. A valid CRC is required to both enable and disable the CRC write feature.

CRC Polynomial

For CRC checksum calculations, the polynomial $x^8 + x^2 + x + 1$ is always used.

To generate the checksum, the 14-bit data conversion result of the four channels are combined to produce a 64-bit data stream. The eight MSBs of the 64-bit data are inverted and the data is appended by eight bits to create a number ending in eight logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

For example, ADAQ4381-4 polynomial is 100000111. Let the original data of four channels be 0xAAAA, 0x5555, 0xAAAA and 0x5555. The eight MSBs of the data are inverted. The data is then appended to include eight 0's on right. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

Refer to Table 13 and Figure 51 for more details on ADAQ4381-4 CRC operation.

INTERFACE

Table 13. Example CRC Calculation for 4-Channel, 16-Bit Data

Data	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X[1]	X	X	X	X	X	X	X
Process Data	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
		1	0	0	0	0	0	1	1	1																														
				1	0	1	0	0	0	1	1	0																													
				1	0	0	0	0	0	0	1	1																													
						1	0	0	0	0	0	1	1	0																												
						1	0	0	0	0	0	1	1	0																												
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															1	0	0	1	0	0	1	1	0																	
															1	0	0	1	0	0	1	1	0																	
																		1	0	0	0	0	1	1	1	0	1												
																		1	0	0	0	0	1	1	1	0	1												
																							1	1	0	1	0	0	0	1	1	1								
																							1	1	0	1	0	0	0	1	1	1								
																											1	0	0	0	0	1	1	1	0					
																											1	0	0	0	0	1	1	1	0					
																																	1	0	0	0	0	1	1	1	1
																																	1	0	0	0	0	1	1	1	1
CRC																																	1	0	0	1	1	1	0	0

[1] X means don't care.

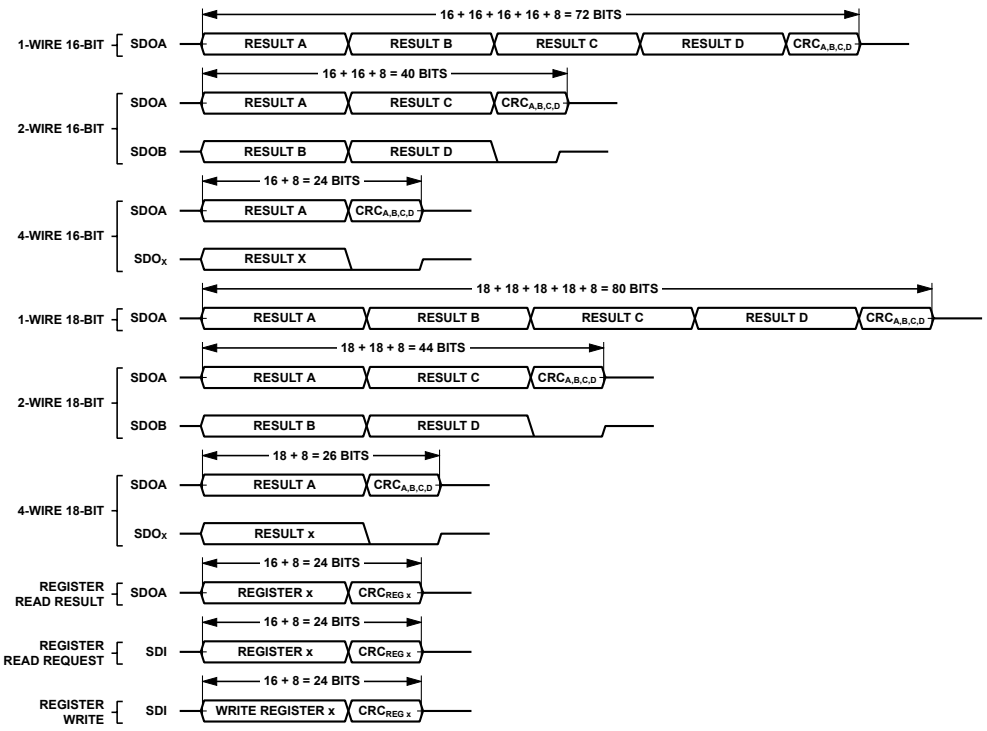

Figure 51. CRC Operation

REGISTERS

The ADAQ4381-4 has user programmable on-chip registers for configuring the device. Table 14 shows a complete overview of the registers available on the ADAQ4381-4.

The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write to a read only register is ignored. Writes to the NOP registers and the reserved register are ignored. Any read request to the NOP registers or reserved registers are considered a no operation and the data transmitted in the next SPI frame are the conversion results.

Table 14. Register Description

Reg	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Default	R/W
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x1	Configuration 1	[15:8]	WR	ADDRESSING			RESERVED		OS_MODE	OSR, Bit 2	0x0000	R/W
		[7:0]	OSR, Bits[1:0]		CRC_W	CRC_R	ALERT_EN	RES	RESERVED	PMODE		
0x2	Configuration 2	[15:8]	WR	ADDRESSING			RESERVED		SDO, Bits[1:0]		0x0000	R/W
		[7:0]	RESET, Bits[7:0]									
0x3	Alert	[15:8]	WR	ADDRESSING			RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	AI_D_HIGH	AI_D_LOW	AI_C_HIGH	AI_C_LOW	AI_B_HIGH	AI_B_LOW	AI_A_HIGH	AI_A_LOW		
0x4	Alert Low threshold	[15:8]	WR	ADDRESSING			ALERT_LOW, Bits[11:8]				0x0800	R
		[7:0]	ALERT_LOW, Bits[7:0]									
0x5	Alert high threshold	[15:8]	WR	ADDRESSING			ALERT_HIGH, Bits[11:8]				0x07FF	R/W
		[7:0]	ALERT_HIGH, Bits[7:0]									

ADDRESSING REGISTERS

A serial register transfer on the ADAQ4381-4 consists of 16 SCLK cycles. The 4 MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. If the addressed register is a valid write register, the read/write bit determines whether the remaining 12 bits of data on the SDI input are loaded into the addressed register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

Table 15. Addressing Register Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REGADDR, Bits[2:0]			Data, Bits[11:0]											

Table 16. Bit Descriptions for Addressing Registers

Bit	Mnemonic	Description
D15	WR	When a 1 is written to this bit, Bits[11:0] of this register are written to the register specified by REGADDR if it is a valid address. Alternatively, when a 0 is written, the next data sent out on the SDO pin is a read from the designated register if it is a valid address.
D14 to D12	REGADDR	When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 14. When WR = 0 and the REGADDR contains a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0 and the REGADDR contains 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access will result in the conversion results being read back.
D11 to D0	Data	These bits are written into the corresponding register specified by the REGADDR bits when the WR bit is 1 and the REGADDR bits contain a valid address

REGISTERS

CONFIGURATION1 REGISTER

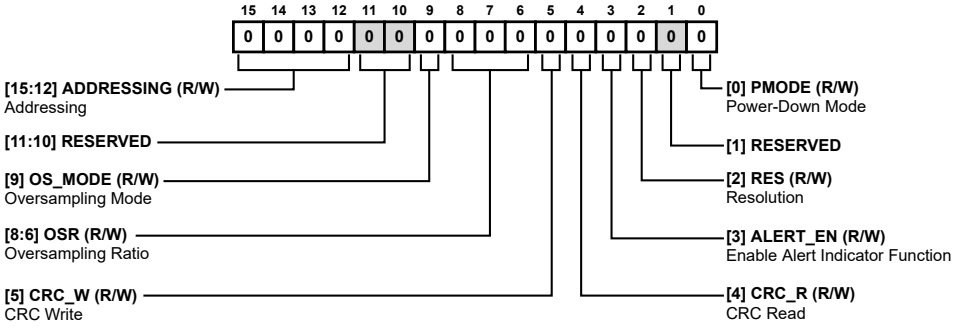

Table 17. Bit Descriptions for Configuration1 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See Addressing Registers section.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	OS_MODE	Oversampling Mode. Sets the oversampling mode of the ADC. 0: normal average. 1: rolling average.	0x0	R/W
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal averaging mode supports oversampling ratios of 2x, 4x, 8x, 16x, and 32x. Rolling average mode supports oversampling ratios of 2x, 4x, and 8x. 000: disabled. 001: 2x. 010: 4x. 011: 8x. 100: 16x. 101: 32x. 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface. When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOx interface. 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This register function when SDO bits = 01. Otherwise, the ALERT_EN bit is ignored. 0: SDOD. 1: $\overline{\text{ALERT}}$.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0, these bits are ignored and the resolution is set to default resolution. 0: normal resolution. 1: 2-bit higher resolution.	0x0	R/W
1	RESERVED	Reserved.	0x0	R/W
0	PMODE	Power-Down Mode. Sets the power modes. 0: normal Mode. 1: shutdown mode.	0x0	R/W

REGISTERS

CONFIGURATION2 REGISTER

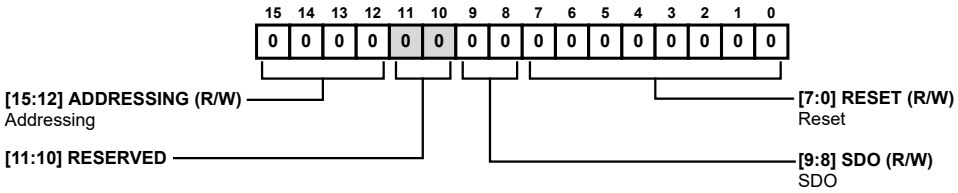

Table 18. Bit Descriptions for Configuration2 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See Addressing Registers section.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
[9:8]	SDO	SDO. Conversion Results Serial Data Output 00: 2-wire. Conversion Data are output on both SDOA and SDOB. 01: 1-wire. Conversion Data are output on SDOA only. 10: 4-wire. Conversion data are output on SDOA, SDOB, SDOC, and SDOD/$\overline{\text{ALERT}}$. 11: 1-wire. Conversion Data are output on SDOA only.	0x0	R/W
[7:0]	RESET	Reset. 0x3C: Performs a soft reset. Refreshes some blocks, Register contents remain unchanged. Clears alert indication register and flushes any oversampling stored variables or active state machine. 0xFF: Performs a hard reset. Resets all possible blocks in the device. Registers contents are set to defaults. All other values are ignored.	0x0	R/W

REGISTERS

ALERT INDICATION REGISTER

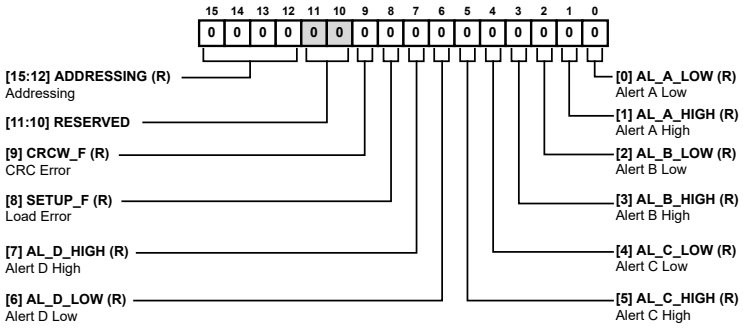

Table 19. Bit Descriptions for Alert Indication Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See Addressing Registers section.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read. 0: No CRC error. 1: CRC error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an alert indication register read. A hard reset via the Configuration2 Register is required to clear this bit and restart the device setup. 0: No setup error. 1: Setup error.	0x0	R
7	AL_D_HIGH	Alert D High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
6	AL_D_LOW	Alert D Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
5	AL_C_HIGH	Alert C High. The alert indication high bit indicate if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
4	AL_C_LOW	Alert C Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
3	AL_B_HIGH	Alert B High. The alert indication high bit indicate if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
2	AL_B_LOW	Alert B Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R

REGISTERS

Table 19. Bit Descriptions for Alert Indication Register (Continued)

Bits	Bit Name	Description	Reset	Access
1	AL_A_HIGH	Alert A High. The alert indication high bit indicate if a conversion result for the respective input channel exceeds the value set in the alert high threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the alert low threshold register. This fault bit is sticky and remains set until the register is read. 0: No alert indication. 1: Alert indication.	0x0	R

ALERT LOW THRESHOLD REGISTER

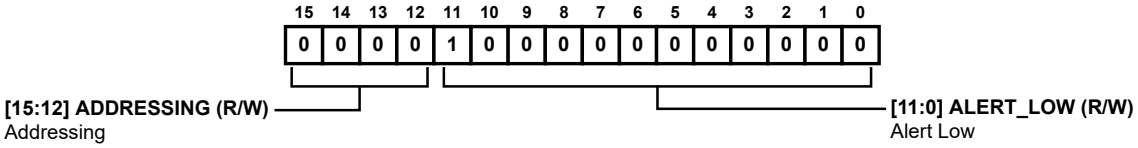

Table 20. Bit Descriptions for Alert Low Threshold Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See Addressing Registers section.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. Bits[11:0] from ALERT_LOW move to the MSBs of the internal alert low register, D[15:4]. The remaining bits, D[3:0] of the internal register are fixed at 0x0. Sets an alert when the converter result is below the value in the alert low threshold register, and the alert is disabled when it is above the value in the alert low threshold register.	0x800	R/W

ALERT HIGH THRESHOLD REGISTER

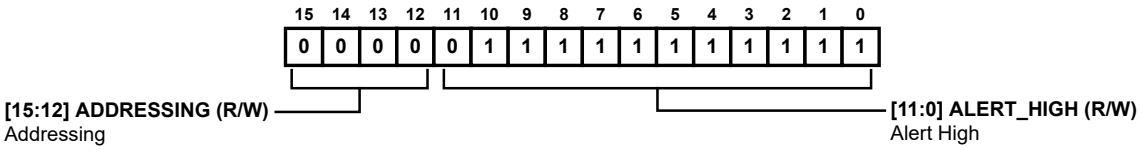

Table 21. Bit Descriptions for Alert High Threshold Register

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See Addressing Registers section.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. Bits D[11:0] from ALERT_HIGH move to the MSBs of the internal alert high register, D[15:4]. The remaining bits, D[3:0] of the internal are fixed at 0xF. Sets an alert when the converter result is above the value in the alert high threshold register, and the alert is disabled when it is below the value in the alert high threshold register.	0x7FF	R/W

LAYOUT GUIDELINES

To achieve a reliable and optimal performance of the ADAQ4381-4, there are some guidelines for the printed circuit board (PCB).

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ4381-4. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ4381-4 is recommended. Care must be taken with the placement of individual components and routing of various signals on the PCB. It is highly recommended to route the input and output signals symmetrically. Solder the ground pins of the ADAQ4381-4 directly to the ground plane of the PCB using multiple vias.

The pinouts of ADAQ4381-4 ease the layout, allowing analog and digital signals easily accessible for routing. The sensitive analog and digital sections must be separated on the PCB while keeping the power supply circuitry away from the analog signal path.

Utilize the ground pins to isolate analog signals from digital signals. Fast switching signals, such as $\overline{CS}$ or SCLK, and digital outputs, SDOA, SDOB, SDOC, and SDOD, must not run near or cross over analog signal paths to prevent noise coupling to ADAQ4381-4.

Good quality ceramic bypass capacitors of at least 2.2 µF (0402, X7R) must be placed at the output of the LDO Linear Regulator generating the ADAQ4381-4 external power supply rails (VS+, VS-, REFIN, V_{CC}, and V_{LOGIC}) to GND to minimize EMI susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ4381-4, saving extra board space and cost.

Figure 52 shows the FFT of ADAQ4381-4 sampling at 4 MSPS with shorted inputs. The recommended board layout for multiple gain options is outlined in the EV-ADAQ4380-4FMCZ user guide.

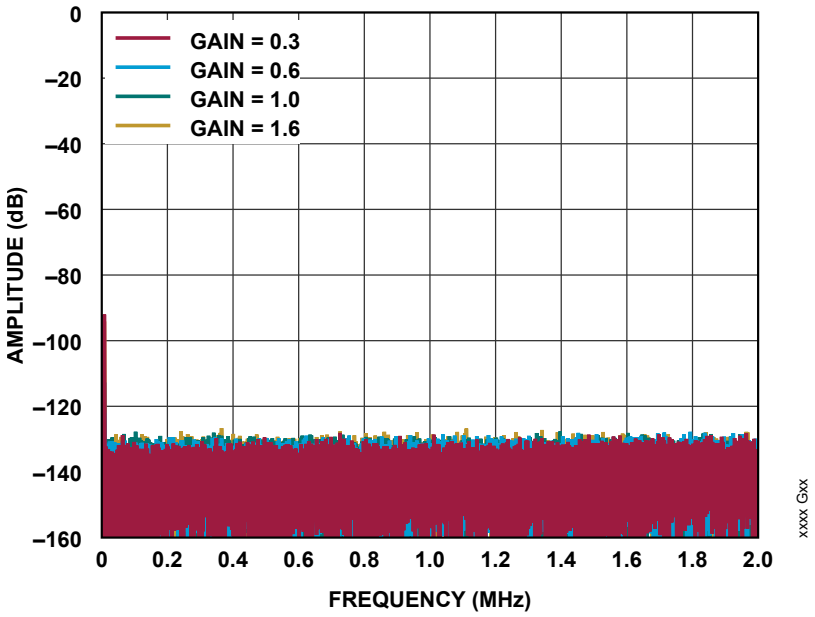

Figure 52. FFT with Shorted Inputs

OUTLINE DIMENSIONS

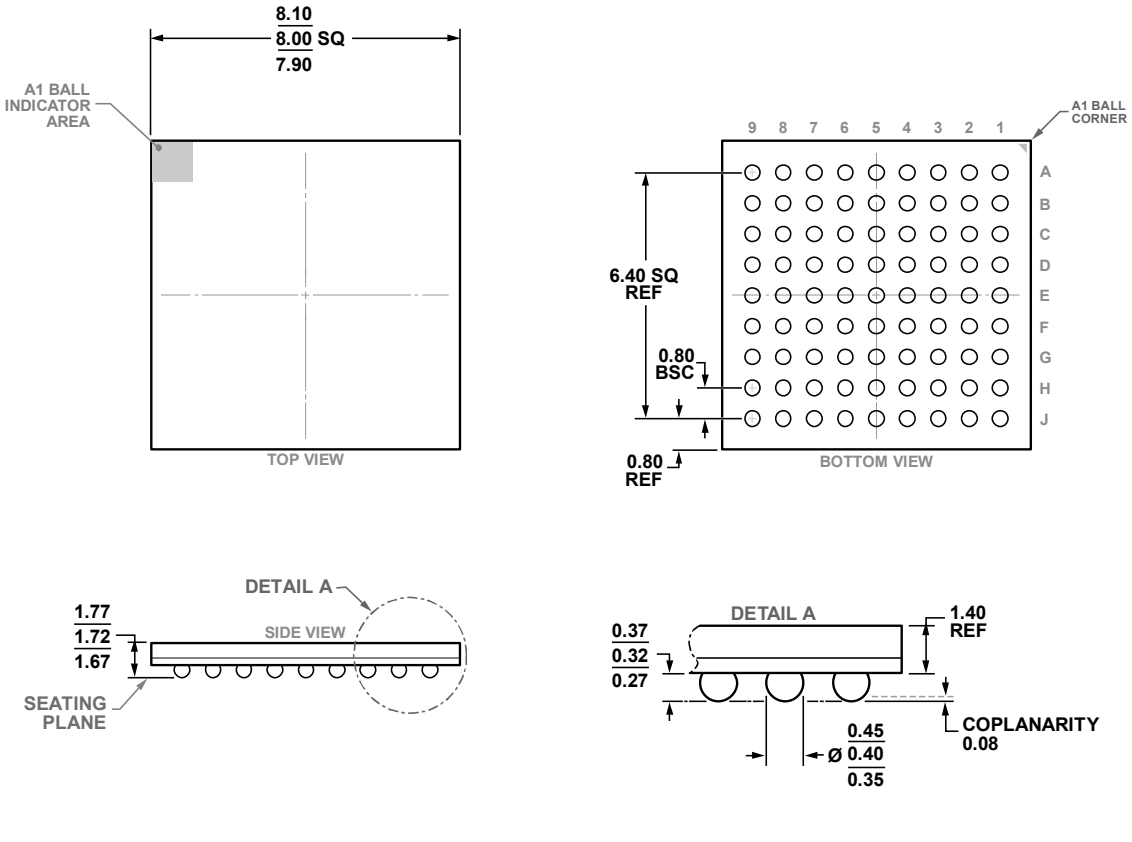

Figure 53. 81-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-81-7)